MP2459

0.5A, 55V, 480kHz Step-Down Converter in a TSOT23-6

The Future of Analog IC Technology®

DESCRIPTION

The MP2459 is a monolithic, step-down, switch-mode converter with a built-in power MOSFET. It achieves a 0.5A peak-output current over a wide input supply range with excellent load and line regulation. Current-mode operation provides a fast transient response and eases loop stabilization. Fault condition protections include cycle-by-cycle current limiting and thermal shutdown.

The MP2459 requires a minimal number of readily-available external components. The MP2459 is available in a TSOT23-6 package.

FEATURES

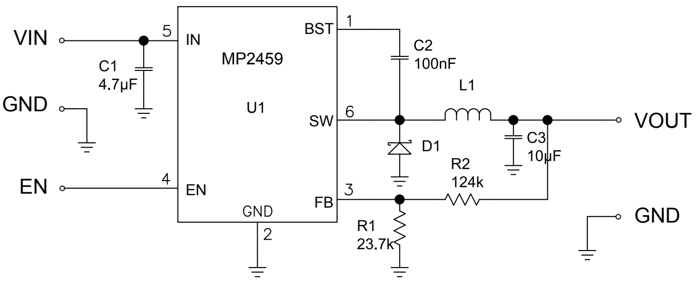
- 0.5A Peak Output Current
- 1Ω Internal Power MOSFET
- Stable with Low-ESR Ceramic Output Capacitors
- Up to 90% Efficiency
- 0.1μA Shutdown Mode
- Fixed 480kHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over-Current Protection
- Wide 4.5V-to-55V Operating Input Range
- Output Adjustable from 0.81V to 0.95*V_{IN}
- Available in a TSOT23-6 Package

APPLICATIONS

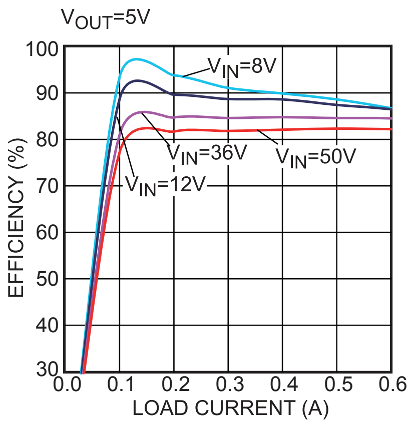
- Power Meters
- Distributed Power Systems
- Battery Chargers
- Pre-Regulator for Linear Regulators
- WLED Drivers

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

TYPICAL APPLICATION



Efficiency vs. Load Current

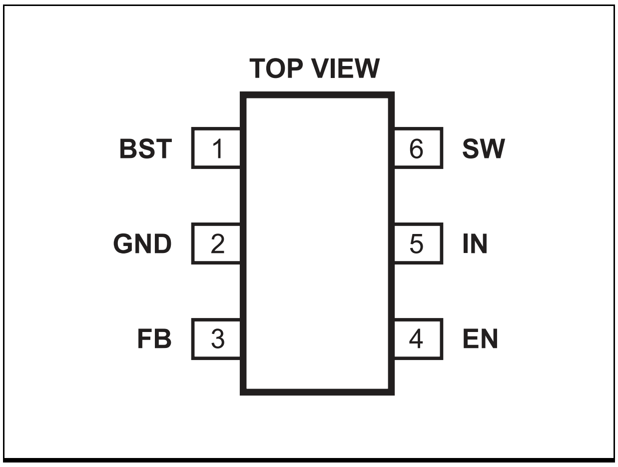


ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2459GJ	TSOT23-6	AEQ

* For Tape & Reel, add suffix –Z (eg. M2459GJ–Z);

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS [1]

Supply Voltage V_{IN} .... −0.3V to 60V
V_{SW} .... −0.3V to V_{IN}+0.3V
V_{BS} ....V_{SW} + 6V
All Other Pins .... −0.3V to +6V
Continuous Power Dissipation (T$_A$ = +25°C) [2]
TSOT23-6 ....0.568W
Junction Temperature .... 150°C
Lead Temperature .... 260°C
Storage Temperature...............−65°C to +150°C

Recommended Operating Conditions [3]

Supply Voltage V_{IN} .... 4.5V to 55V
Output Voltage V_{OUT}................0.81V to 0.95×V_{IN}
Operating Junction Temp. ....−40°C to +125°C

Thermal Resistance [4]

	θ_{JA}	θ_{JC}	
TSOT23-6	220 ...	110	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device function is not guaranteed outside of the recommended operating conditions.
4) Measured on JESD51-7, 4-layer PCB..

ELECTRICAL CHARACTERISTICS

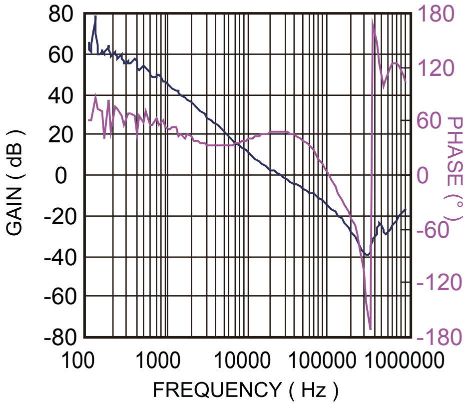
V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 55V	0.792	0.812	0.832	V
Feedback Current	I_{FB}	V_{FB} = 0.85V			0.1	μA
Switch-On Resistance	$R_{DS(ON)}$			1		Ω
Switch Leakage	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = 0V			1	μA
Current Limit	I_{LIM}		1.0	1.25	1.5	A
Oscillator Frequency	f_{SW}	V_{FB} = 0.6V	380	480	580	kHz
Foldback Frequency	f_{SW_F}	V_{FB} = 0V		150		kHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.6V	90	93.5		%
Minimum ON-Time	τ_{ON}			100		ns
Under-Voltage Lockout Threshold, Rising	V_{UVLO_R}		2.9	3.3	3.7	V
Under-Voltage Lockout Threshold, Falling	V_{UVLO_F}		2.65	3.05	3.45	V
Under-Voltage Lockout Threshold, Hysteresis	V_{UVLO_HYS}			250		mV
EN Threshold, Rising	V_{EN_R}			1.35		V
EN Threshold, Falling	V_{EN_F}			1.17		V
EN Threshold, Hysteresis	V_{EN_HYS}			180		mV
EN Input Current	I_{EN}	V_{EN} = 2V		3.1		μA
		V_{EN} = 0V		0.1		
Supply Current (Shutdown)	I_S	V_{EN} = 0V		0.1	1.0	μA
Supply Current (Quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 1V		0.73	0.85	mA
Thermal Shutdown	T_{SD}			165		°C
Thermal Shutdown Hysteresis	T_{SD_HYS}			20		°C

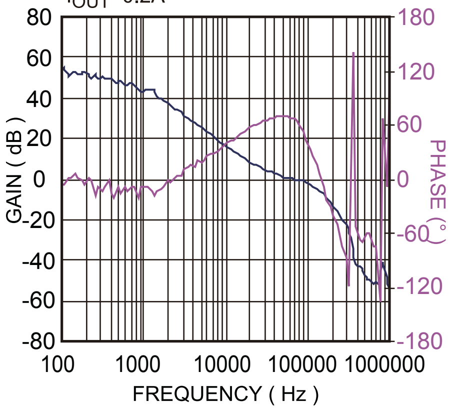
TYPICAL CHARACTERISTICS

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.5A, L=15µH, T_A=25°C, unless otherwise noted.

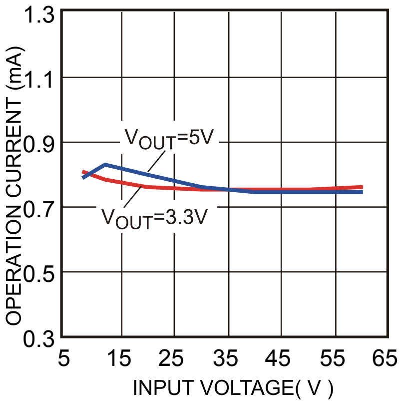
Bandwidth
I_{OUT}=0.8A



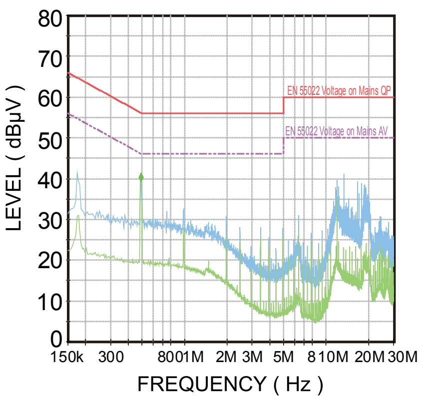
Bandwidth
V_{OUT}=3.3V,
I_{OUT}=0.2A



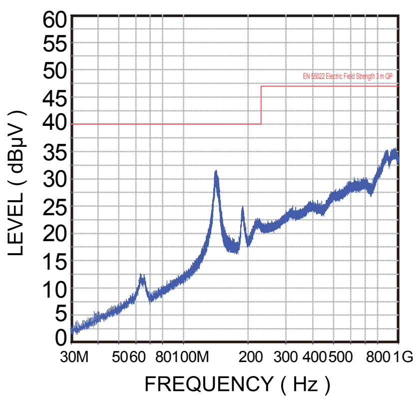
Operation Current
I_{OUT}=0A



Conduction EMI



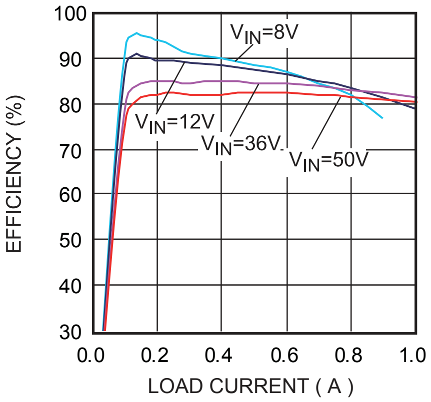
Radiation EMI



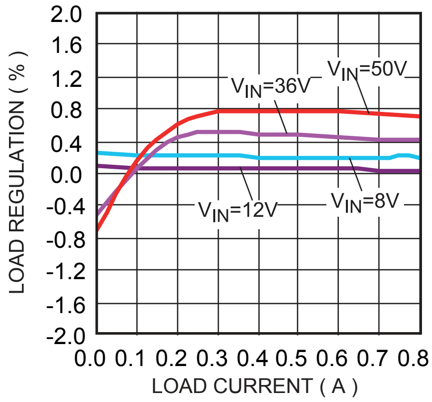
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, V_{OUT}=5V, L=22µH, T_A=25°C, unless otherwise noted.

Efficiency vs. Load

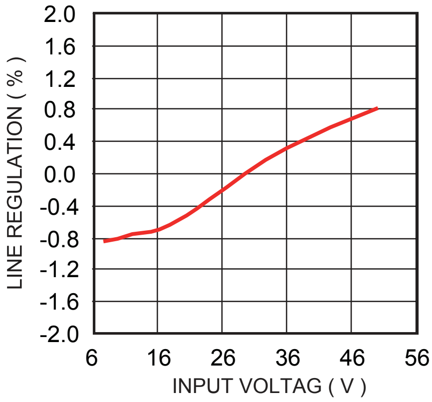


Load Regulation



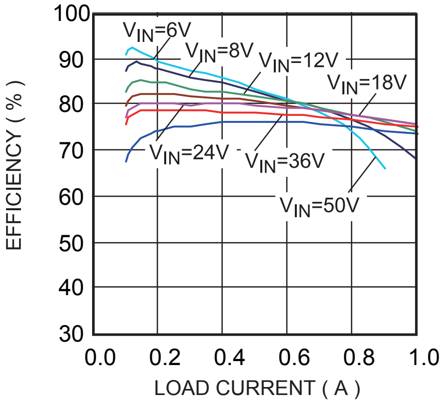
Line Regulation

I_{OUT}=0.5A



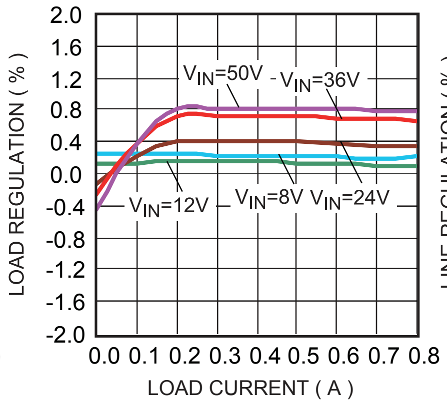
Efficiency vs. Load

V_{OUT}=3.3V



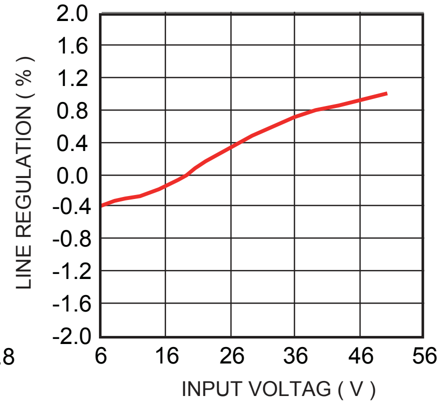
Load Regulation

V_{OUT}=3.3V

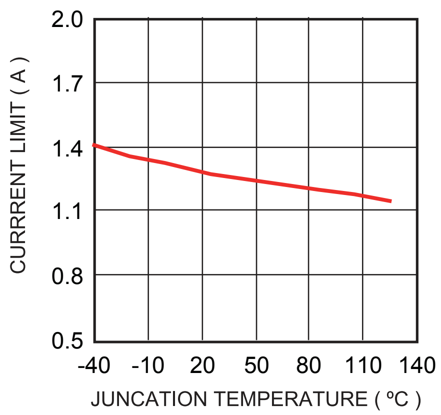


Line Regulation

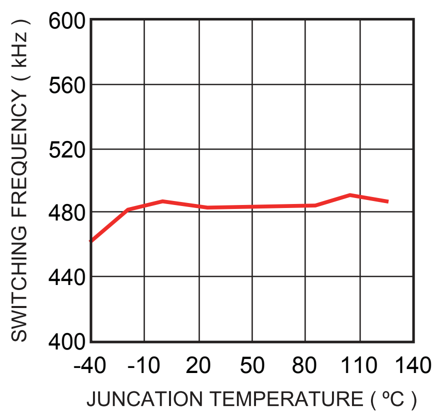
V_{OUT}=3.3V, I_{OUT}=0.5A



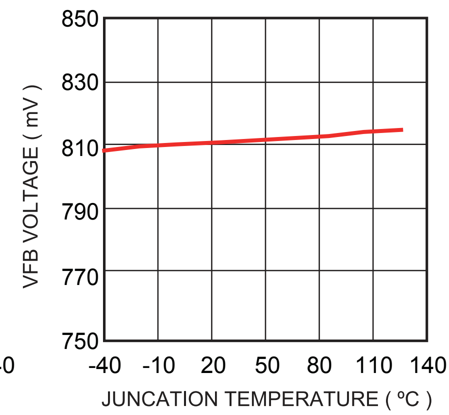
Current Limit vs. T_J



Frequency vs. T_J



Feedback Voltage vs. T_J

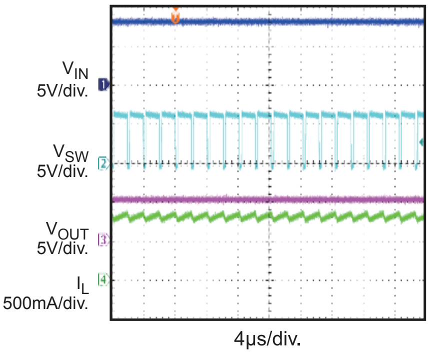


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT}=5V, L=22µH, T_A=25°C, unless otherwise noted.

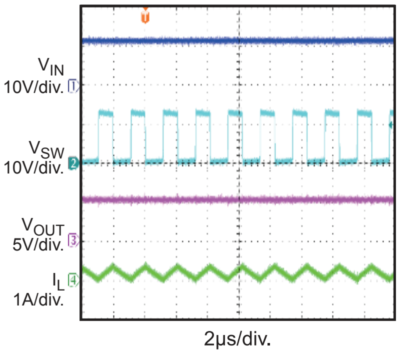
Steady State

V_{IN}=8V, I_{OUT}=0.8A



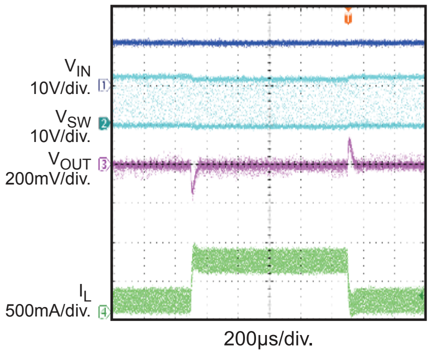
Steady State

I_{OUT}=0.15A



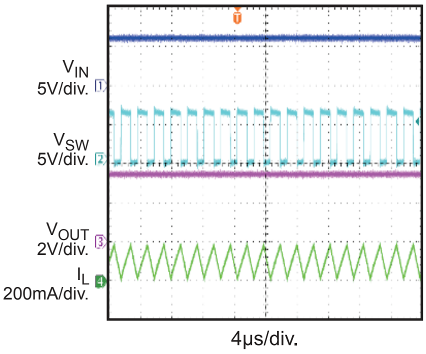
Load Transient

I_{OUT}=0.2A to 0.7A



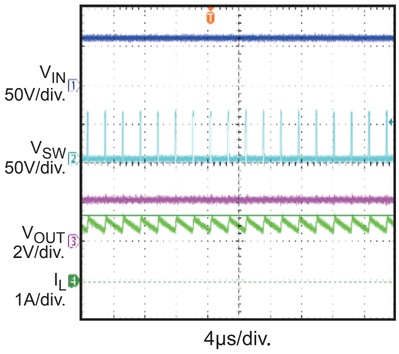
Steady State

V_{IN}=6V, V_{OUT}=3.3V, I_{OUT}=0.1A



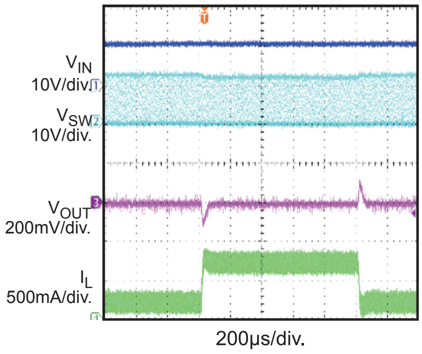
Steady State

V_{IN}=60V, V_{OUT}=3.3V, I_{OUT}=0.9A



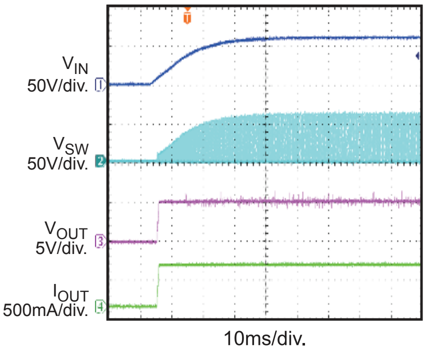
Load Transient

V_{OUT}=3.3V, I_{OUT}=0.2A to 0.7A



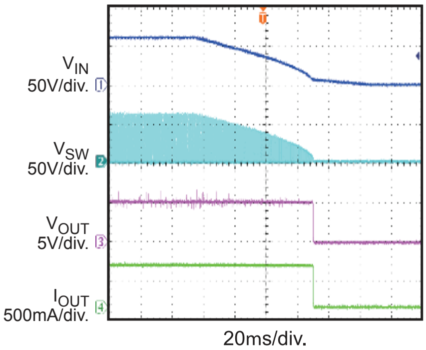
Power Ramp Up

V_{IN}=60V, I_{OUT}=0.5A



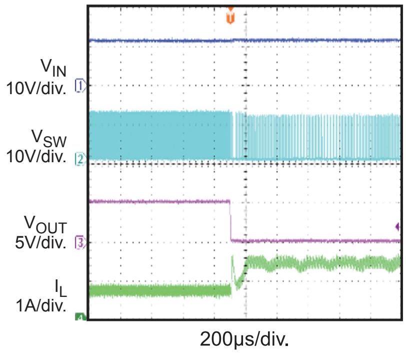
Power Ramp Down

V_{IN}=60V, I_{OUT}=0.5A



Short Output

I_{OUT}=0.65A

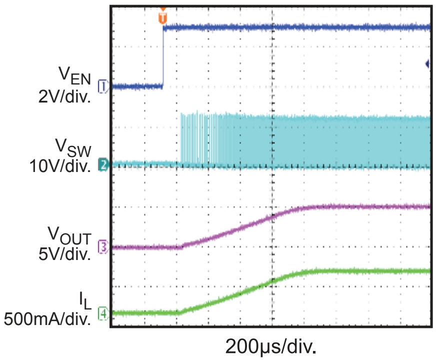


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT}=5V, L=22µH, T_A=25°C, unless otherwise noted.

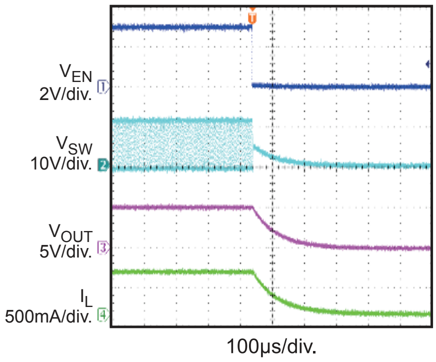
Enable On

I_{OUT}=0.5A



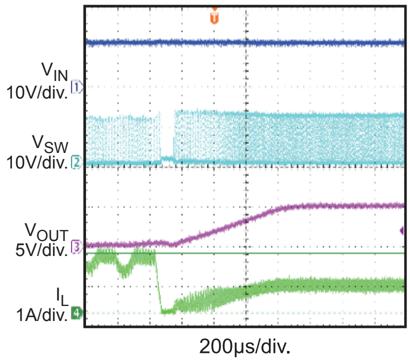
Enable Off

I_{OUT}=0.5A



Short Output Recovery

I_{OUT}=0.65A



PIN FUNCTIONS

Pin #	Name	Description
1	BST	Bootstrap. Connect a capacitor between the SW and BS pins to form a floating supply across the power switch driver. This capacitor drives the power switch's gate above the supply voltage.
2	GND	Ground. Voltage reference for the regulated output voltage. Requires special layout considerations. Isolate this node from the D1 to C1 ground path to prevent switching current spikes from inducing.
3	FB	Feedback. Sets the output voltage. Connect to the tap of an external resistor divider from the output to GND. The frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 250mV to prevent current-limit runaway during a short-circuit fault.
4	EN	On/Off. Pull EN above 1.2V to turn the device ON. For automatic enable, connect to V_{IN} using a 100kΩ resistor.
5	IN	Supply Voltage. The MP2459 operates from a 4.5V-to-55V unregulated input. Requires C1 to prevent large voltage spikes from appearing at the input.
6	SW	Switch Output.

OPERATION

The MP2459 is a current mode buck regulator. That is, the EA output voltage is proportional to the peak inductor current.

At the beginning of a cycle, M1 is off. The EA output voltage is higher than the current sense amplifier output, and the current comparator's output is low. The rising edge of the 480kHz CLK signal sets the RS Flip-Flop. Its output turns on M1 thus connecting the SW pin and inductor to the input supply.

The increasing inductor current is sensed and amplified by the Current Sense Amplifier. Ramp compensation is summed to the Current Sense Amplifier output and compared to the Error Amplifier output by the PWM Comparator. When the sum of the Current Sense Amplifier output and the Slope Compensation signal exceeds the EA output voltage, the RS Flip-Flop is reset and M1 is turned off. The external Schottky rectifier diode (D1) conducts the inductor current.

If the sum of the Current Sense Amplifier output and the Slope Compensation signal does not exceed the EA output for a whole cycle, then the falling edge of the CLK resets the Flip-Flop.

The output of the Error Amplifier integrates the voltage difference between the feedback and the 0.81V bandgap reference. The polarity is such that lower than 0.81V FB pin voltage increases the EA output voltage. Since the EA output voltage is proportional to the peak inductor current, an increase in its voltage also increases current delivered to the output.

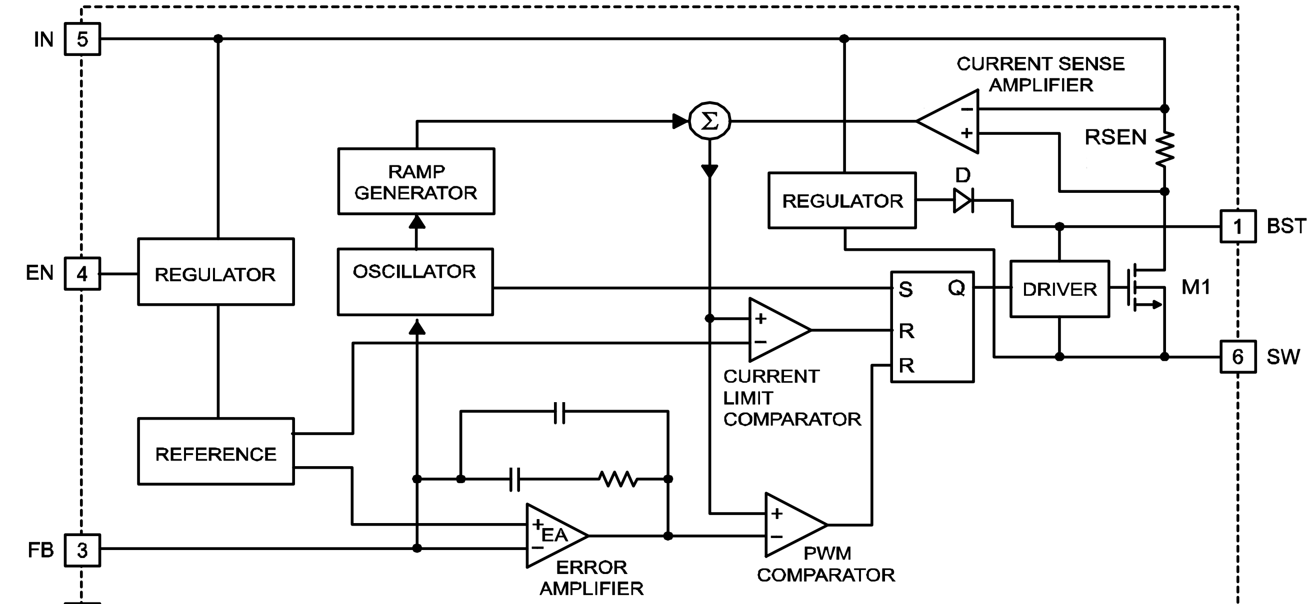


Figure 1: Functional Block Diagram

APPLICATION INFORMATION

Setting Output Voltage

The external resistor divider sets the output voltage (see the Typical Application schematic). Table 1 lists resistors for common output voltages. The feedback resistor (R2) also sets the feedback loop bandwidth with the internal compensation capacitor (see Figure 1). R1 is:

$$R1 = \frac{R2}{\frac{V_{OUT}}{0.812V} - 1}$$

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.8	102 (1%)	124 (1%)
2.5	59 (1%)	124 (1%)
3.3	40.2 (1%)	124 (1%)
5	23.7 (1%)	124 (1%)

Selecting the Inductor

Use an inductor with a DC current rating at least 25% percent higher than the maximum load current for most applications. For best efficiency, the inductor's DC resistance should be less than 200mΩ. Refer to Table 2 for suggested surface-mount inductors.

Table 2: Inductor Selection Guide

Part Number	Inductance (µH)	Max DCR (Ω)	Current Rating (A)	Dimensions L x W x H (mm^3)
Wurth				
744042100	10	0.15	1.3	4.8x4.8x1.8
744052150	15	0.19	0.95	5.8x5.8x1.8
744053220	22	0.12	1.15	5.8x5.8x2.8
ABC				
SH4018100YL	10	0.15	1.3	4.8x4.8x1.8
SH4028150YL	15	0.15	1.03	4.8x4.8x2.8
SH5028220YL	22	0.12	1.15	5.8x5.8x2.8
TDK				
VLCF5020T-100MR87	10	0.182	1.56	5x5x2.0
VLCF5024T-150MR71-2	15	0.152	1.66	5x5x2.4
VLCF5028T-220MR71-2	22	0.14	1.66	5x5x2.8
Coilcraft				
LPS5030-103MRC	10	0.127	1.5	5x5x3
LPS5030-153MRC	15	0.16	1.4	5x5x3
LPS5030-223MRC	22	0.19	1.25	5x5x3

For most designs, the required inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}}$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light-load conditions (below 100mA), use a larger inductance to improve efficiency.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high-frequency-switching current from passing through the input. Use ceramic capacitors with X5R or X7R dielectrics for their low ESRs and small temperature coefficients. For most applications, a 4.7μF capacitor will sufficient.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. The output capacitor impedance should be low at the switching frequency. Use ceramic capacitors with X5R or X7R dielectrics for their low ESR characteristics. For most applications, a 22μF ceramic capacitor will sufficient.

PCB Layout Guide

PCB layout is very important to stability. Please follow these guidelines and use Figure 2 as reference.

1) Keep the path of switching current short and minimize the loop area formed by the input capacitor, high-side MOSFET, and Schottky diode.
2) Keep the connection from the power ground→Schottky diode→SW pin as short and wide as possible.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Route SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND to large copper areas to cool the chip for improved thermal performance and long-term reliability. For single layer PCBs, avoid soldering the exposed pad

.

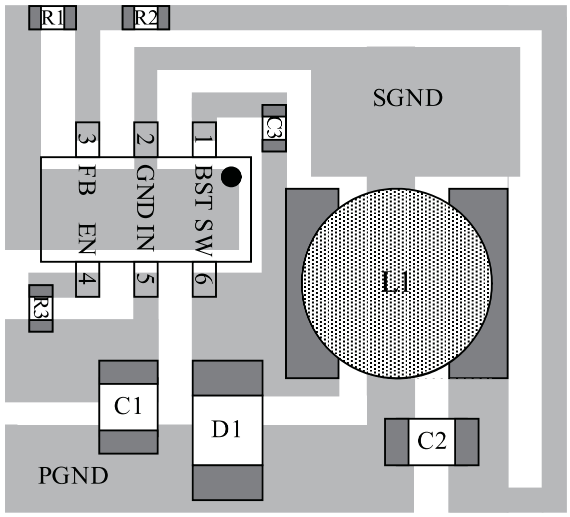


Figure 2: PCB Layout

External Bootstrap Diode

An external bootstrap diode may enhance regulator efficiency under the following conditions:

- V_{OUT}=5V or 3.3V; and
- High duty cycle: $D=\frac{V_{OUT}}{V_{IN}}>65\%$

In these cases, add an external BST diode from the output of the voltage regulator to the BST pin, as shown in Figure 3.

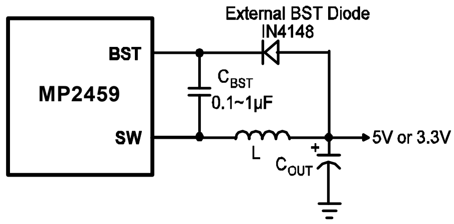
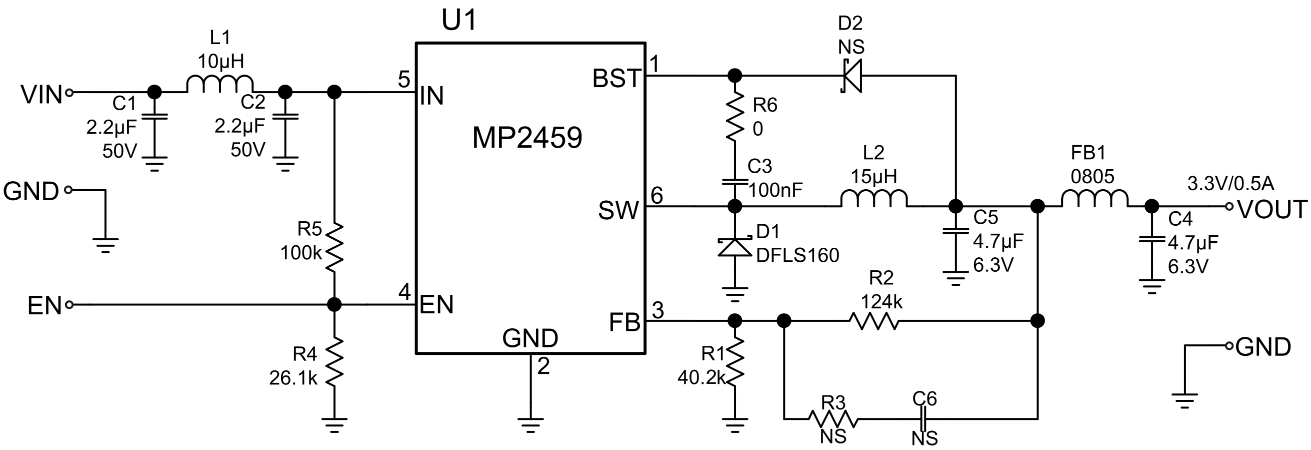


Figure 3: Optional Bootstrap Diode for Enhanced Efficiency

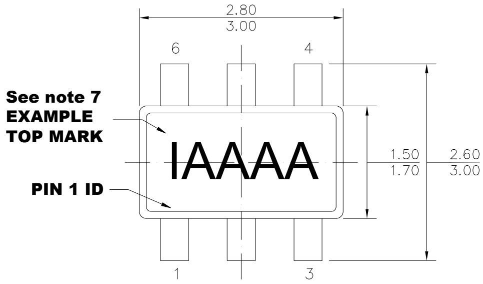
The recommended external BST diode is IN4148, and the BST capacitor is 0.1μF-1μF.

TYPICAL APPLICATION CIRCUIT

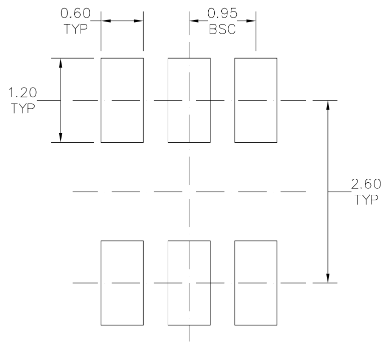


PACKAGE INFORMATION

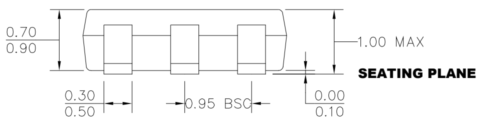
TSOT23-6



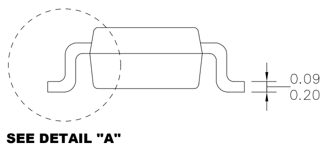
TOP VIEW



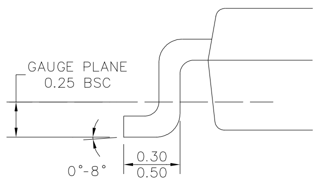
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	5/27/2014	Initial Release	-
1.1	5/21/2021	Update POD	Page 14