NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PART
ISL80015IRZ-T

October 18, 2010 FN6191.6

Monolithic 600mA Step-Down Regulator with Low Quiescent Current

The ISL8010 is a synchronous, integrated FET 600mA step-down regulator with internal compensation. It operates with an input voltage range from 2.5V to 5.5V, which accommodates supplies of 3.3V, 5V, or a Li-Ion battery source. The output can be externally set from 0.8V to V_{IN} with a resistive divider.

The ISL8010 features automatic PFM/PWM mode control, or PWM mode only. The PWM frequency is typically 1.4MHz and can be synchronized up to 12MHz. The typical no load quiescent current is only 120µA. Additional features include a Power-Good output, <1µA shutdown current, short-circuit protection, and over-temperature protection.

The ISL8010 is available in the 10 Ld MSOP package, making the entire converter occupy less than 0.18in^2 of PCB area with components on one side only. The 10 Ld MSOP package is specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

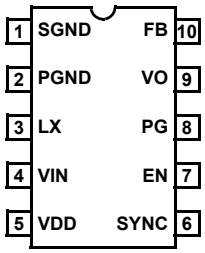
PART NUMBER (Notes 2, 3)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
ISL8010IUZ	8010Z	10 Ld MSOP	MDP0043
ISL8010IUZ-T7 (Note 1)	8010Z	10 Ld MSOP	MDP0043
ISL8010IUZ-T13 (Note 1)	8010Z	10 Ld MSOP	MDP0043

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL8010. For more information on MSL please see techbrief TB363.

Pinout

ISL8010
(10 LD MSOP)
TOP VIEW



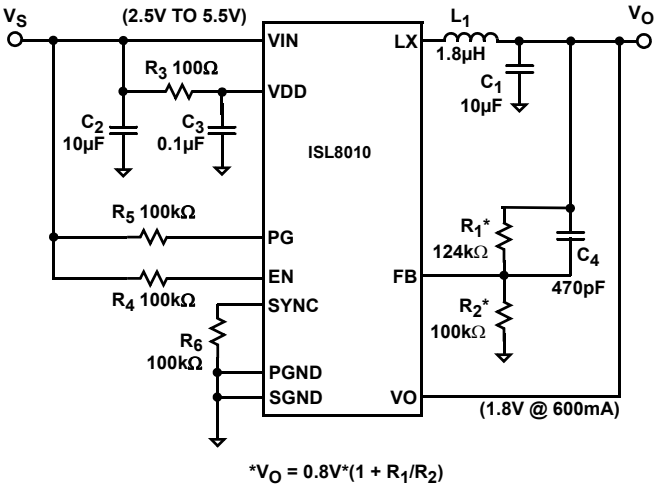
Features

- Less than 0.18in^2 footprint for the complete 600mA converter
- Components on one side of PCB
- Max height 1.1mm 10 Ld MSOP
- Power-Good (PG) output
- Internally-compensated voltage mode controller
- Up to 95% efficiency
- <1µA shutdown current
- 120µA quiescent current
- Hiccup mode overcurrent and over-temperature protection
- Externally synchronizable up to 12MHz
- Pb-free available (RoHS compliant)

Applications

- PDA and pocket PC computers
- Bar code readers
- Cellular phones
- Portable test equipment
- Li-Ion battery powered devices
- Small form factor (SFP) modules

Typical Application Diagram



Absolute Maximum Ratings (T_A = +25°C)

V_{IN}, V_{DD}, PG to SGND . . . . . -0.3V to +6.5V
LX to PGND . . . . . -0.3V to (V_{IN} + +0.3V)
SYNC, EN, V_O, FB to SGND . . . . . -0.3V to (V_{IN} + +0.3V)
PGND to SGND . . . . . -0.3V to +0.3V
Peak Output Current 800mA

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} (°C/W)
10 Ld MSOP. 130
Operating Ambient Temperature . . . . . -40°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . +125°C
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

$V_{DD} = V_{IN} = V_{EN}$ = 3.3V, $C_1 = C_2$ = 10µF, L = 1.8µH, V_O = 1.8V (as shown in "Typical Application Diagram" on page 1), T_A = -40°C to +85°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
DC CHARACTERISTICS						
V_{FB}	Feedback Input Voltage	PWM Mode	**790**	800	**810**	mV
I_{FB}	Feedback Input Current				**100**	nA
V_{IN}, V_{DD}	Input Voltage		**2.5**		**5.5**	V
$V_{IN,OFF}$	Minimum Voltage for Shutdown	V_{IN} falling, T_A = +25°C only	2		2.2	V
$V_{IN,ON}$	Maximum Voltage for Start-up	V_{IN} rising, T_A = +25°C only	2.2		2.4	V
I_S	Input Supply Quiescent Current					
	Active - PFM Mode	V_{SYNC} = 0V		120	**145**	µA
	Active - PWM Mode	V_{SYNC} = 3.3V		6.5	**7.5**	mA
I_{DD}	Supply Current	PWM, $V_{IN} = V_{DD}$ = 5V		400	**500**	µA
		EN = 0, $V_{IN} = V_{DD}$ = 5V		0.1	**3**	µA
$r_{DS(ON)-PMOS}$	PMOS FET Resistance	V_{DD} = 5V, T_A = +25°C		70	100	mΩ
$r_{DS(ON)-NMOS}$	NMOS FET Resistance	V_{DD} = 5V, T_A = +25°C		45	75	mΩ
I_{LMAX}	Current Limit			1.2		A
$T_{OT,OFF}$	Over-temperature Threshold	T rising		145		°C
$T_{OT,ON}$	Over-temperature Hysteresis	T falling		130		°C
I_{EN}, I_{SYNC}	EN, SYNC Current	V_{EN}, V_{RSI} = 0V and 3.3V	**-1**		**1**	µA
V_{EN1}, V_{SYNC1}	EN, SYNC Rising Threshold	V_{DD} = 3.3V			**2.4**	V
V_{EN2}, V_{SYNC2}	EN, SYNC Falling Threshold	V_{DD} = 3.3V	**0.8**			V
V_{PG}	Minimum V_{FB} for PG, WRT Targeted V_{FB} Value	V_{FB} rising			**95**	%
		V_{FB} falling	**86**			%
V_{OLPG}	PG Voltage Drop	I_{SINK} = 3.3mA		35	**70**	mV
AC CHARACTERISTICS						
F_{PWM}	PWM Switching Frequency		**1.25**	1.4	**1.6**	MHz
t_{SS}	Soft-start Time			650		µs

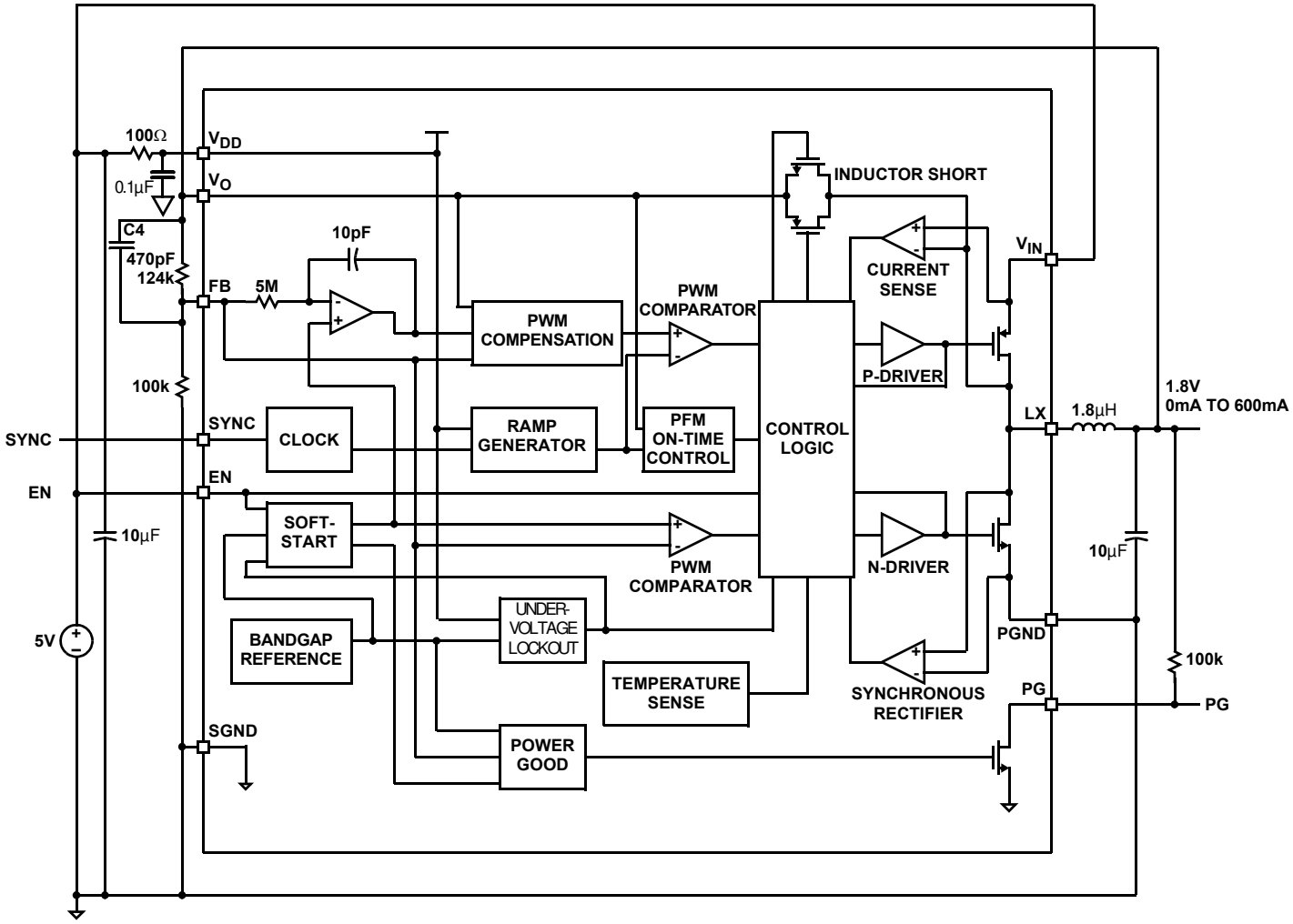
NOTE:

5. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Pin Descriptions

PIN NUMBER	PIN NAME	PIN FUNCTION
1	SGND	Negative supply for the controller stage
2	PGND	Negative supply for the power stage
3	LX	Inductor drive pin; high current digital output with average voltage equal to the regulator output voltage
4	VIN	Positive supply for the power stage
5	VDD	Power supply for the controller stage
6	SYNC	SYNC input pin; when connected to HI, regulator runs at forced PWM mode; when connected to Low, auto PFM/PWM mode; when connected to external sync signal, at external PWM frequency up to 12MHz
7	EN	Enable
8	PG	Power-Good open drain output
9	VO	Output voltage sense
10	FB	Voltage feedback input; connected to an external resistor divider between V_O and SGND for variable output

Block Diagram



Typical Performance Curves

All waveforms are taken at V_{IN} = 3.3V, V_O = 1.8V, I_O = 600mA with component values shown on page 1 at room ambient temperature, unless otherwise noted.

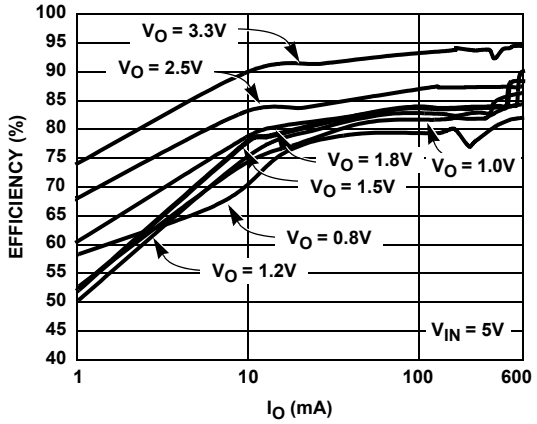


FIGURE 1. EFFICIENCY vs I_O (PFM/PWM MODE)

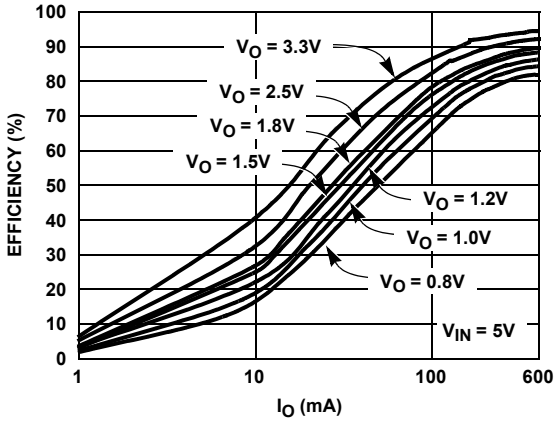


FIGURE 2. EFFICIENCY vs I_O (PWM MODE)

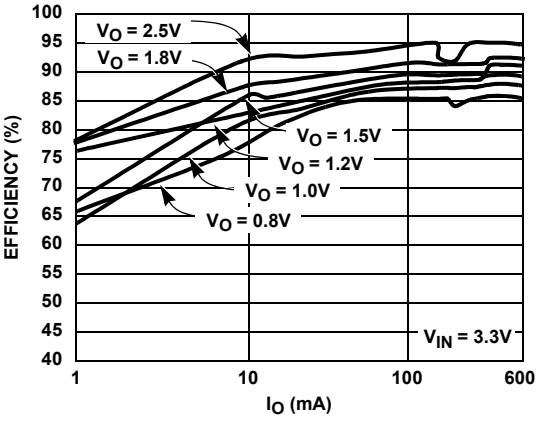


FIGURE 3. EFFICIENCY vs I_O (PFM/FWM MODE)

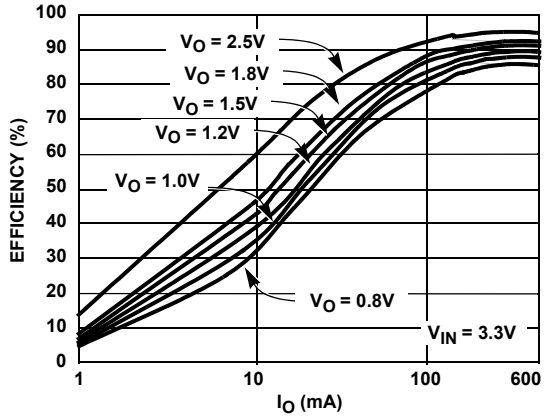


FIGURE 4. EFFICIENCY vs I_O (PWM MODE)

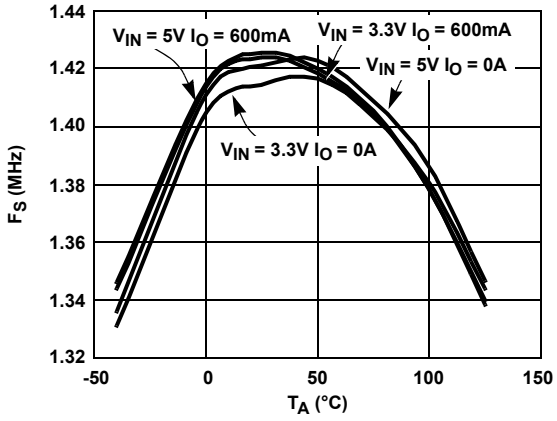


FIGURE 5. F_S vs JUNCTION TEMPERATURE (PWM MODE)

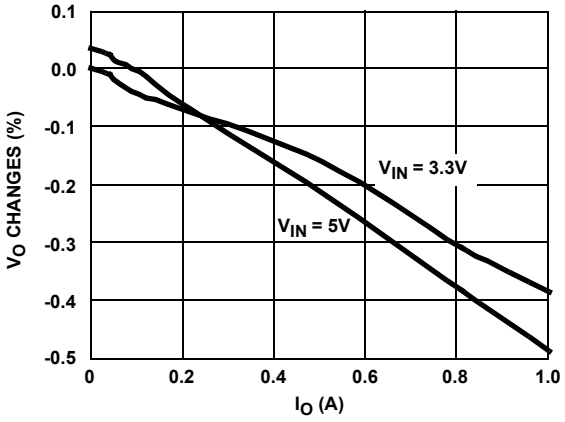


FIGURE 6. LOAD REGULATIONS (PWM MODE)

Typical Performance Curves

All waveforms are taken at V_{IN} = 3.3V, V_O = 1.8V, I_O = 600mA with component values shown on page 1 at room ambient temperature, unless otherwise noted. **(Continued)**

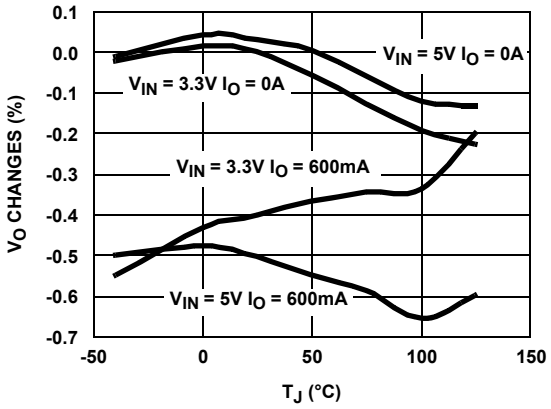


FIGURE 7. PWM MODE LOAD/LINE REGULATIONS vs JUNCTION TEMPERATURE

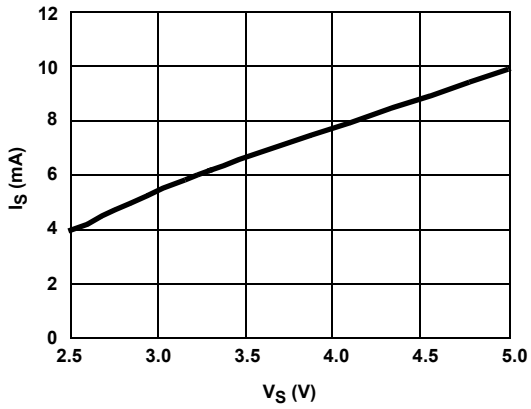


FIGURE 8. NO LOAD QUIESCENT CURRENT (PWM MODE)

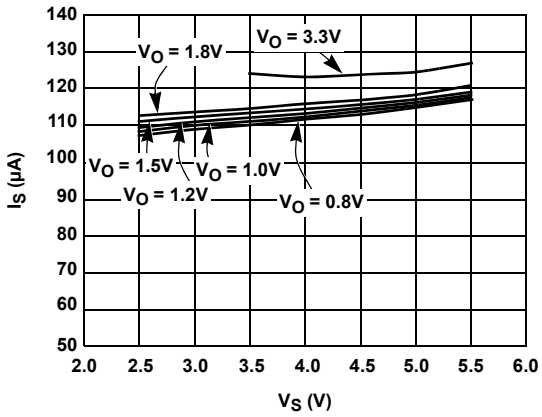


FIGURE 9. NO LOAD QUIESCENT CURRENT (PFM MODE)

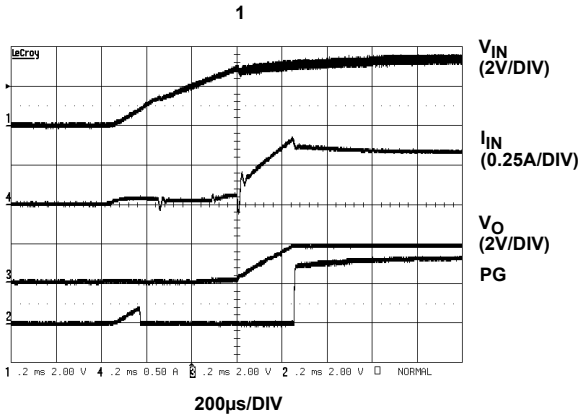


FIGURE 10. START-UP AT I_O = 600mA

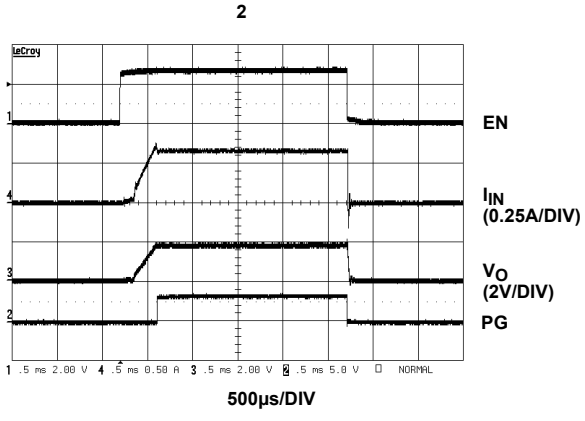


FIGURE 11. ENABLE AND SHUTDOWN

Typical Performance Curves

All waveforms are taken at V_{IN} = 3.3V, V_O = 1.8V, I_O = 600mA with component values shown on page 1 at room ambient temperature, unless otherwise noted. **(Continued)**

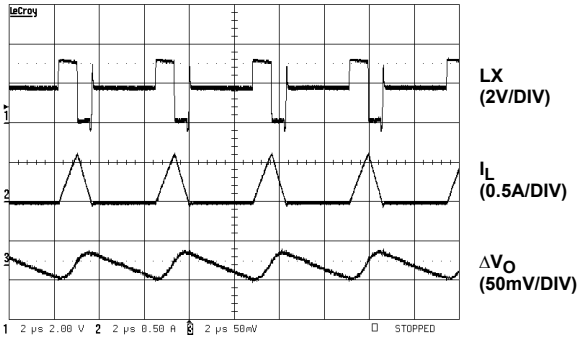


FIGURE 12. PFM STEADY-STATE OPERATION WAVEFORM (I_O = 100mA)

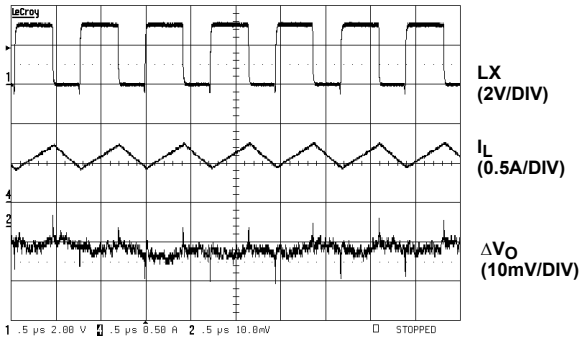


FIGURE 13. PWM STEADY-STATE OPERATION (I_O = 600mA)

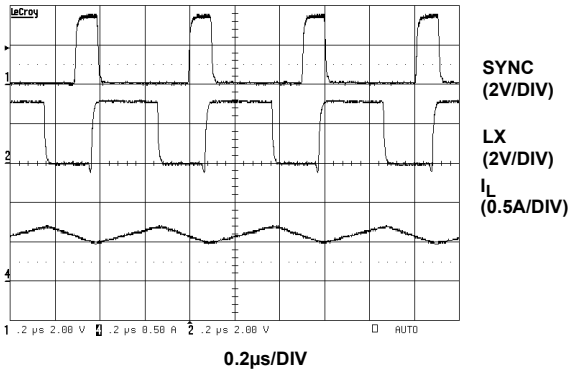


FIGURE 14. EXTERNAL SYNCHRONIZATION TO 2MHz

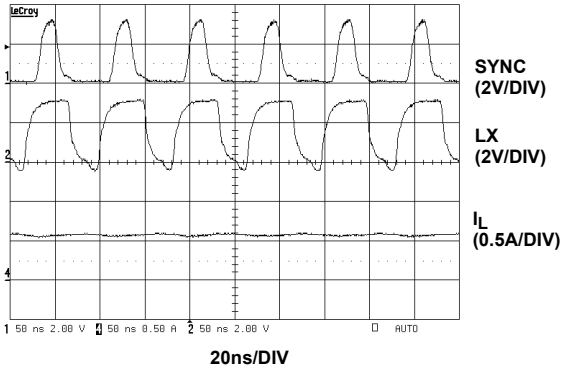


FIGURE 15. EXTERNAL SYNCHRONIZATION TO 12MHz

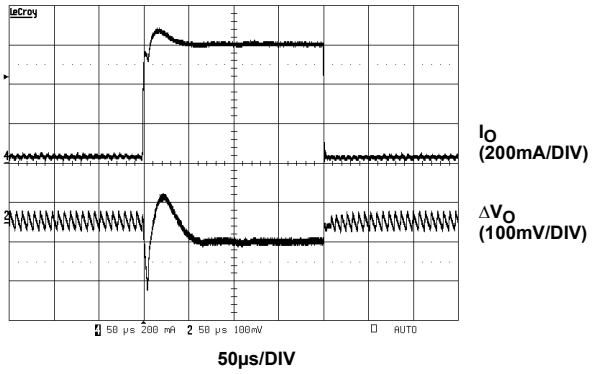


FIGURE 16. LOAD TRANSIENT RESPONSE (22mA TO 600mA)

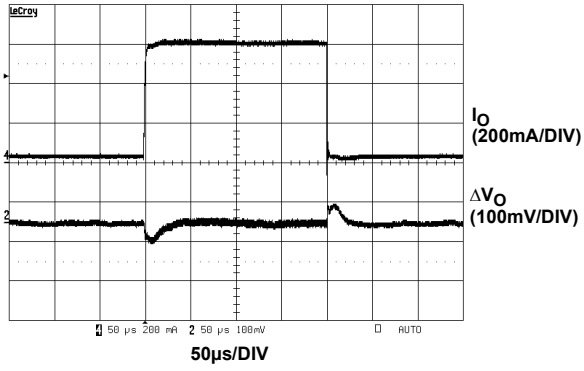


FIGURE 17. PWM LOAD TRANSIENT RESPONSE (30mA TO 600mA)

Typical Performance Curves

All waveforms are taken at V_{IN} = 3.3V, V_O = 1.8V, I_O = 600mA with component values shown on page 1 at room ambient temperature, unless otherwise noted. **(Continued)**

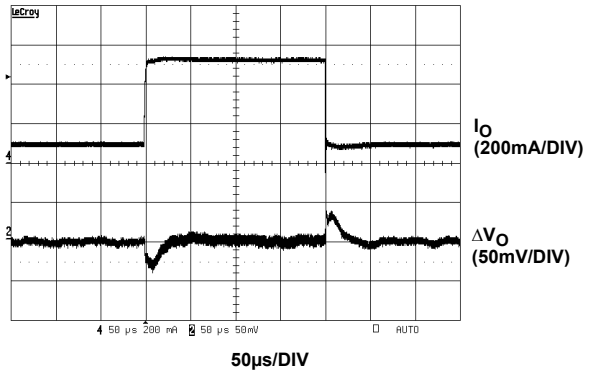


FIGURE 18. PWM LOAD TRANSIENT RESPONSE (100mA TO 500mA)

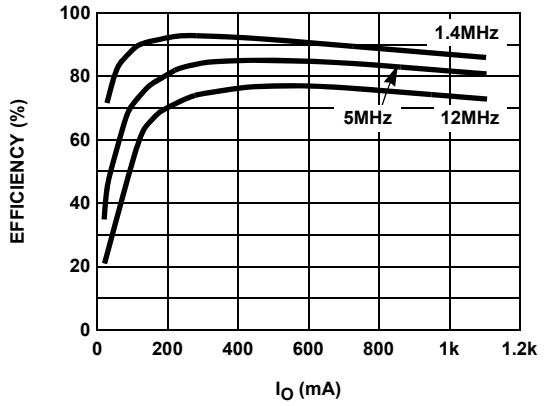


FIGURE 19. EFFICIENCY vs I_O (PWM MODE)

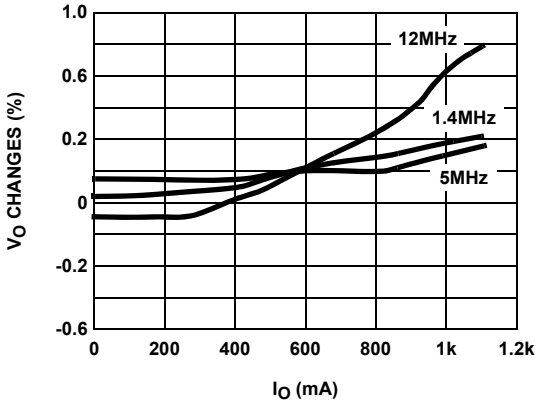


FIGURE 20. LOAD REGULATION (PWM MODE)

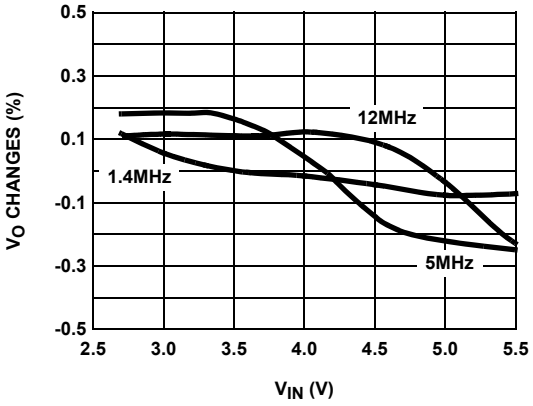


FIGURE 21. LINE REGULATION @ 500mA (PWM MODE)

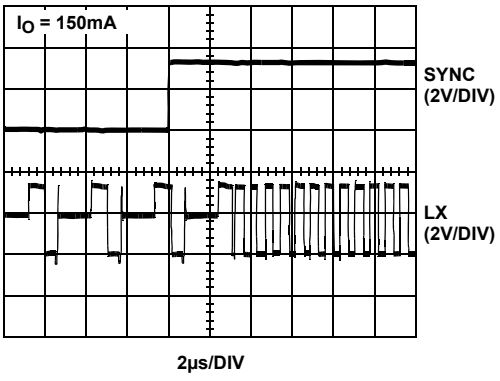


FIGURE 22. PFM-PWM TRANSITION TIME

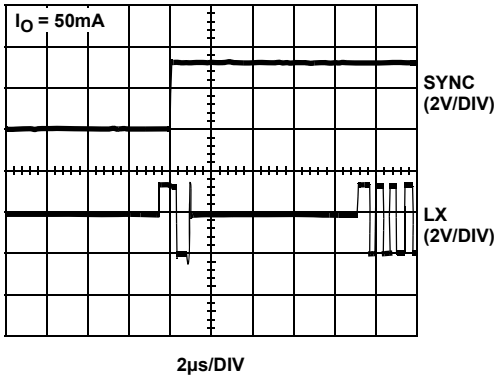


FIGURE 23. PFM-PWM TRANSITION TIME

Typical Performance Curves

All waveforms are taken at V_{IN} = 3.3V, V_O = 1.8V, I_O = 600mA with component values shown on page 1 at room ambient temperature, unless otherwise noted. **(Continued)**

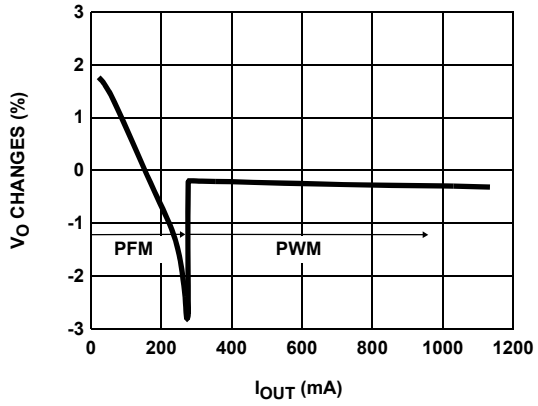


FIGURE 24. PFM-PWM TRANSITION

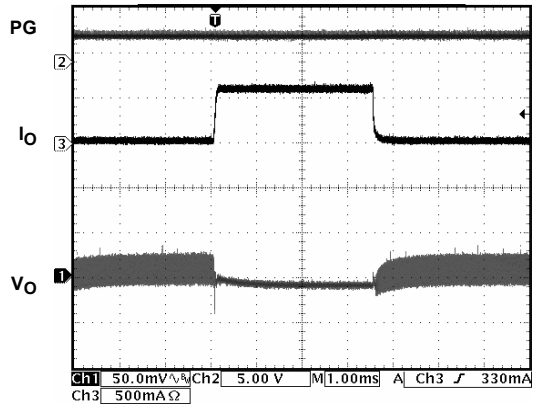


FIGURE 25. PFM-PWM LOAD TRANSIENT

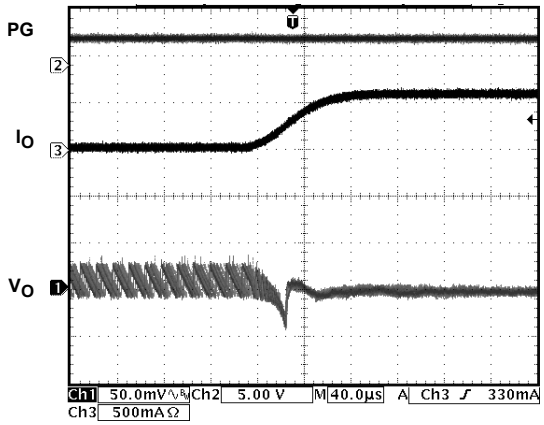


FIGURE 26. PFM TO PWM TRANSITION

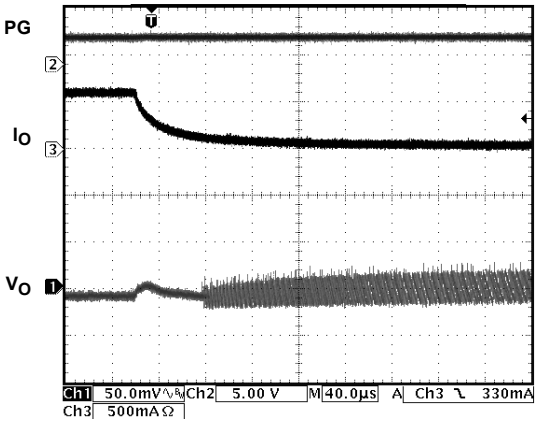


FIGURE 27. PWM TO PFM TRANSITION

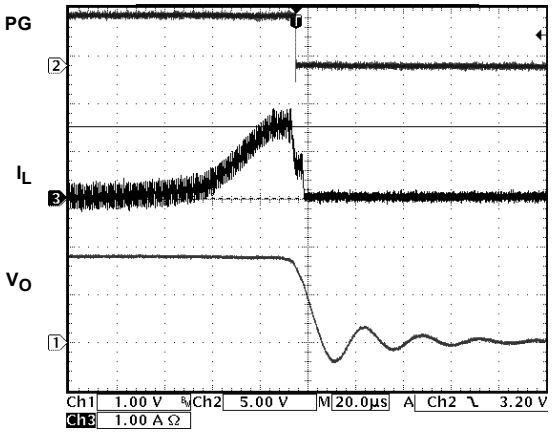


FIGURE 28. OVERCURRENT SHUTDOWN

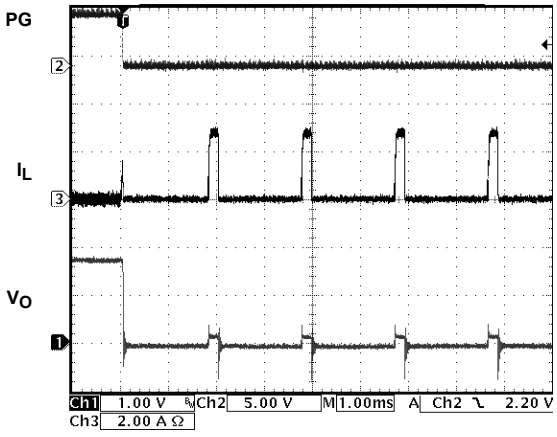


FIGURE 29. OVERCURRENT HICCUP MODE

Applications Information

Product Description

The ISL8010 is a synchronous, integrated FET 600mA step-down regulator, which operates from an input of 2.5V to 5.5V. The output voltage is user-adjustable with a pair of external resistors.

When the load is very light, the regulator automatically operates in the PFM mode, thus achieving high efficiency at light load (>70% for 1mA load). When the load increases, the regulator automatically switches over to a voltage-mode PWM operating at nominal 1.4MHz switching frequency. The efficiency is up to 95%.

It can also operate in a fixed PWM mode or be synchronized to an external clock up to 12MHz for improved EMI performance.

PFM Operation

The heart of the ISL8010 regulator is the automatic PFM/PWM controller.

If the SYNC pin is connected to ground, the regulator operates automatically in either the PFM or PWM mode, depending on load. When the SYNC pin is connected to V_{IN}, the regulator operates in the fixed PWM mode. When the pin is connected to an external clock ranging from 1.6MHz to 12MHz, the regulator is in the fixed PWM mode and synchronized to the external clock frequency.

In the automatic PFM/PWM operation, when the load is light, the regulator operates in the PFM mode to achieve high efficiency. The top P-Channel MOSFET is turned on first. The inductor current increases linearly to a preset value before it is turned off. Then the bottom N-Channel MOSFET turns on, and the inductor current linearly decreases to zero current. The N-Channel MOSFET is then turned off, and an anti-ringing MOSFET is turned on to clamp the LX pin to VO. Both MOSFETs remain off until VFB drops below the internal reference voltage of 0.8V. The inductor current looks like triangular pulses. The frequency of the pulses is mainly a function of output current. The higher the load, the higher the frequency of the pulses until the inductor current becomes continuous. At this point, the controller automatically changes to PWM operation.

When the controller transitions to PWM mode, there can be a perturbation to the output voltage. This perturbation is due to the inherent behavior of switching converters when transitioning between two control loops. To reduce this effect, it is recommended to use the phase-lead capacitor (C_4) shown in the “Typical Application Diagram” on page 1. This capacitor allows the PWM loop to respond more quickly to this type of perturbation. To properly size C_4, refer to “Component Selection” on page 10.

PWM Operation

The regulator operates the same way in the forced PWM or synchronized PWM mode. In this mode, the inductor current is always continuous and does not stay at zero.

In this mode, the P-Channel MOSFET and N-Channel MOSFET always operate complementary. When the P-Channel MOSFET is on and the N-Channel MOSFET off, the inductor current increases linearly. The input energy is transferred to the output and also stored in the inductor. When the P-Channel MOSFET is off and the N-Channel MOSFET on, the inductor current decreases linearly, and energy is transferred from the inductor to the output. Hence, the average current through the inductor is the output current. Since the inductor and the output capacitor act as a low pass filter, the duty cycle ratio is approximately equal to V_O divided by V_{IN}.

The output LC filter has a second order effect. To maintain the stability of the converter, the overall controller must be compensated. This is done with the fixed internally compensated error amplifier and the PWM compensator. Because the compensations are fixed, the values of input and output capacitors are 10µF to 22µF ceramic and inductor is 1.5µH to 2.2µH.

Forced PWM Mode/SYNC Input

Pulling the SYNC pin HI (>2.5V) forces the converter into PWM mode in the next switching cycle regardless of output current. The duration of the transition varies depending on the output current. Figures 22 and 23 (under two different loading conditions) show the device goes from PFM to PWM mode.

Note: In forced PWM mode, the IC will continue to start-up in PFM mode to support pre-biased load applications.

Start-Up and Shutdown

When the EN pin is tied to V_{IN} and V_{IN} reaches approximately 2.4V, the regulator begins to switch. The inductor current limit is gradually increased to ensure proper soft-start operation.

When the EN pin is connected to a logic low, the ISL8010 is in the shutdown mode. All the control circuitry and both MOSFETs are off, and V_{OUT} falls to zero. In this mode, the total input current is less than 1µA.

When the EN reaches logic HI, the regulator repeats the start-up procedure, including the soft-start function.

Current Limit and Short-Circuit Protection

The current limit is set at about 1.2A for the PMOS. When a short-circuit occurs in the load, the preset current limit restricts the amount of current available to the output, which causes the output voltage to drop as load demand increases. When the output voltage drops 30mV below the reference voltage, the converter will shutdown for a period of time (approximated by Equation 1) and then restart. If the overcurrent condition still exists, it will repeat the shutdown-wait-restart event. This

is called a “hiccup” event. The average power dissipation is reduced, thereby reducing the likelihood of damaged current and thermal conditions in the IC.

$$tHICCUP \approx \left(\frac{700\mu \cdot V_{IN}}{3} + 216\mu\right) \quad \text{(EQ. 1)}$$

Thermal Shutdown

Once the junction reaches about +145°C, the regulator shuts down. Both the P-Channel and the N-Channel MOSFETs turn off. The output voltage will drop to zero. With the output MOSFETs turned off, the regulator will cool down. Once the junction temperature drops to about +130°C, the regulator will perform a normal restart.

Thermal Performance

The ISL8010 is available in a fused-lead 10 Ld MSOP package. Compared with regular 10 Ld MSOP package, the fused-lead package provides lower thermal resistance. The θ_{JA} is +100°C/W on a 4-layer board and +125°C/W on 2-layer board. Maximizing the copper area around the pins will further improve the thermal performance.

Power Good Output

The PG (pin 8) output is used to indicate when the output voltage is properly regulating at the desired set point. It is an open-drain output that should be tied to VIN or VCC through a 100kΩ resistor. If no faults are detected, EN is high, and the output voltage is within ~5% of regulation, the PG pin will be allowed to go high. Otherwise, the open-drain NMOS will pull PG low.

Output Voltage Selection

Users can set the output voltage of the variable version with a resistor divider, which can be chosen based on Equation 2:

$$V_O = 0.8 \times \left(1 + \frac{R_1}{R_2}\right) \quad \text{(EQ. 2)}$$

Component Selection

Because of the fixed internal compensation, the component choice is relatively narrow. For a regulator with fixed output voltage, only two capacitors and one inductor are required. It is recommended to use between 10µF and 22µF multilayer ceramic capacitors with X5R or X7R rating for both the input and output capacitors, and 1.5µH to 2.2µH for the inductor.

The RMS current present at the input capacitor is decided by Equation 3:

$$I_{INRMS} = \frac{\sqrt{V_O \times (V_{IN} - V_O)}}{V_{IN}} \times I_O \quad \text{(EQ. 3)}$$

This is about half of the output current I_O for all the V_O. This input capacitor must be able to handle this current.

The inductor peak-to-peak ripple current is given as Equation 4:

$$\Delta I_{IL} = \frac{(V_{IN} - V_O) \times V_O}{L \times V_{IN} \times f_S} \quad \text{(EQ. 4)}$$

L is the inductance

f_S is the switching frequency (nominally 1.4MHz)

The inductor must be able to handle I_O for the RMS load current, and to assure that the inductor is reliable, it must handle the 2A surge current that can occur during a current limit condition.

In addition to decoupling capacitors and inductor value, it is important to properly size the phase-lead capacitor C_4 (Refer to “Typical Application Diagram” on page 1). The phase-lead capacitor creates additional phase margin in the control loop by generating a zero and a pole in the transfer function. As a general rule of thumb, C_4 should be sized to start the phase-lead at a frequency of ~2.5kHz. The zero will always appear at lower frequency than the pole and follow Equation 5:

$$f_Z = \frac{1}{2\pi R_2 C_4} \quad \text{(EQ. 5)}$$

Over a normal range of R_2 (~10kΩ to 100kΩ), C_4 will range from ~470pF to 4700pF. The pole frequency cannot be set once the zero frequency is chosen as it is dictated by the ratio of R_1 and R_2, which is solely determined by the desired output set point. Equation 6 shows the pole frequency relationship:

$$f_P = \frac{1}{2\pi (R_1 \| R_2) C_4} \quad \text{(EQ. 6)}$$

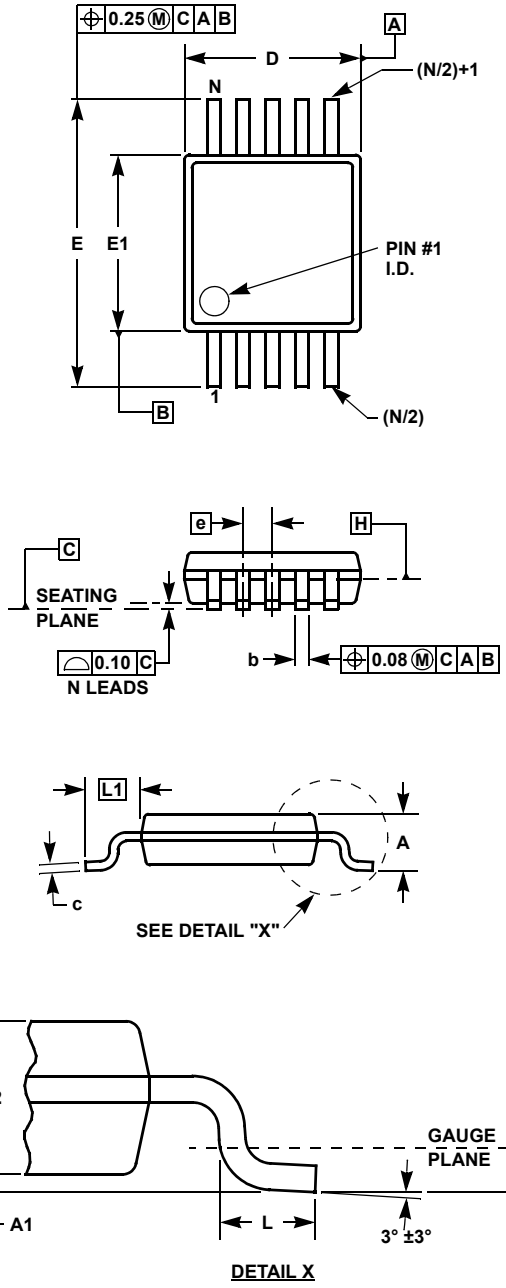
Layout Considerations

The layout is very important for the converter to function properly. The following PC layout guidelines should be followed:

1. Separate the Power Ground (⏚) and Signal Ground (⏚); connect them only at one point right at the pins
2. Place the input capacitor as close to VIN and PGND pins as possible
3. Make the following PC traces as small as possible:
   - from LX pin to L
   - from C_O to PGND
4. If used, connect the trace from the FB pin to R_1 and R_2 as close as possible
5. Maximize the copper area around the PGND pin
6. Place several via holes under the chip to additional ground plane to improve heat dissipation

The demo board is a good example of layout based on this outline. Please refer to the ISL8010 Application Note.

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

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NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.