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Evaluating the ADG5462F User Defined Fault Protection and Detection, 10 Ω R_{ON}, Quad Channel Protector

FEATURES

- Supply voltages
  - Dual supply: ±5 V to ±22 V
  - Single supply: 8 V to 44 V
- Protected against overvoltage on source pins
  - Signal voltages up to −55 V and +55 V
- LEDs for visual overvoltage indication
- Parallel interface compatible with 3 V logic
- On-board low dropout (LDO) regulator for digital supply and control, if required

EVALUATION KIT CONTENTS

- EVAL-ADG5462FEBZ evaluation board

DOCUMENTS NEEDED

- ADG5462F data sheet
- EVAL-ADG5462FEBZ user guide

EQUIPMENT NEEDED

- DC voltage source
  - ±22 V for dual supply
  - 44 V for single supply
- Optional digital logic supply: 3 V to 5 V
- Analog signal source
- Method to measure voltage, such as a digital multimeter (DMM)

GENERAL DESCRIPTION

The EVAL-ADG5462FEBZ is the evaluation board for the ADG5462F, which features an overvoltage protected quad channel protector. The ADG5462F has overvoltage detection and protection circuitry on the source pins and is protected against signals up to −55 V and +55 V in both the powered and unpowered states.

Figure 1 shows the EVAL-ADG5462FEBZ in a typical evaluation setup. The ADG5462F is soldered to the center of the evaluation board, and wire screw terminals are provided to connect to each of the source and drain pins. Three screw terminals power the device and a fourth terminal provides a user defined digital logic supply voltage, if required. Alternatively, a LDO regulator is provided for 5 V digital logic supply and to supply the LEDs, which are mounted to provide visual indication of the fault status of the switch.

Full specifications on the ADG5462F are available in the product data sheet, which should be consulted in conjunction with this user guide when using the evaluation board.

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REVISION HISTORY

11/15—Revision 0: Initial Version

TYPICAL EVALUATION BOARD SETUP

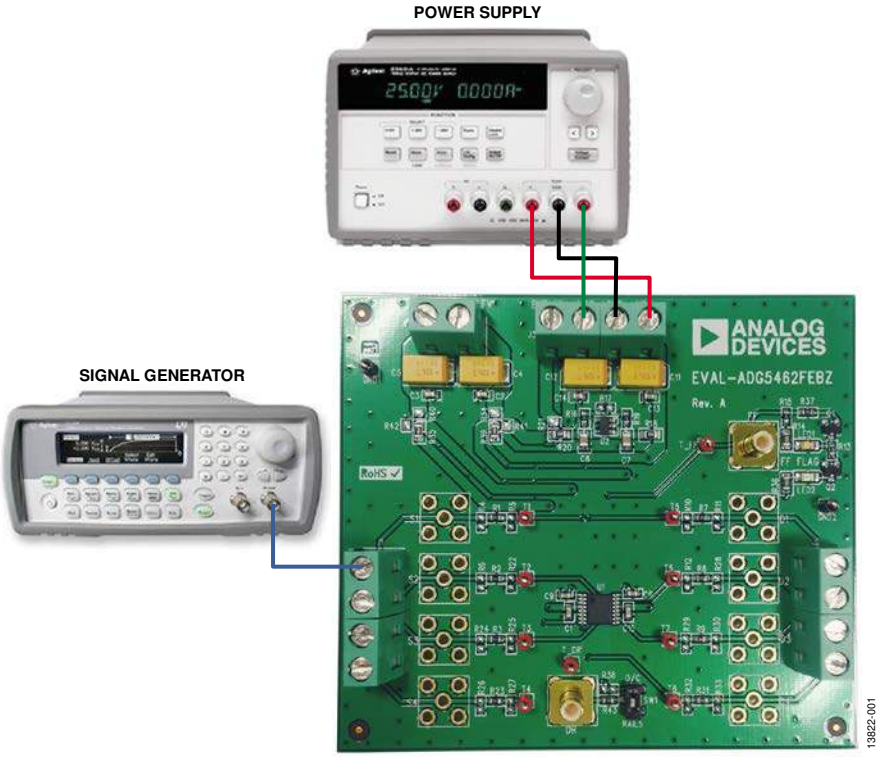

Figure 1.

GETTING STARTED

EVALUATION BOARD SETUP PROCEDURE

The EVAL-ADG5462FEBZ operates independently and does not require any additional evaluation boards or software to operate. An on-board LDO regulator is the digital power supply for the LEDs and manually controls the ADG5462F.

Supply the EVAL-ADG5462FEBZ with a dual power source of up to ±22 V or a single supply of up to +44 V by connecting VSS and GND together.

Follow these steps to conduct a functionality test:

1. Connect a power supply to J3. Connect VSS and GND together if a single supply is required.
2. Ensure that a 0 Ω resistor is inserted in R18 to use the on-board LDO regulator and that a 0 Ω resistor is inserted in R20.
3. Control the digital signals for the ADG5462F by using SW1.
4. Verify that LED1 is green; this indicates that the mux is operating normally.

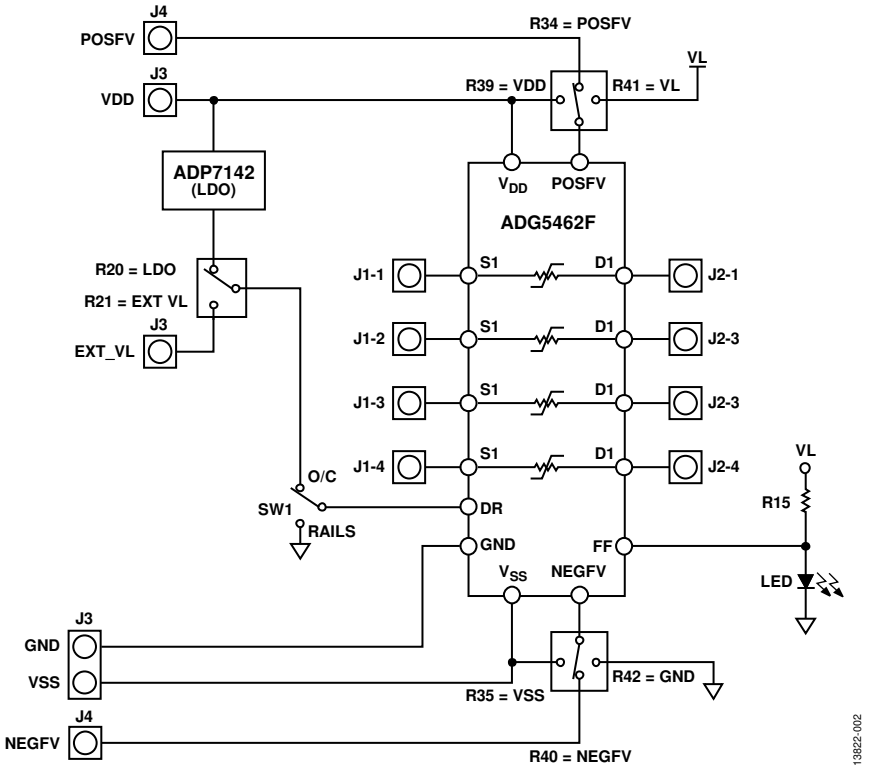

Figure 2. EVAL-ADG5462FEBZ Block Diagram

EVALUATION BOARD HARDWARE

To evaluate the ADG5462F use the EVAL-ADG5462FEBZ. Figure 1 shows a typical evaluation setup where only a power supply and signal generator are required. Figure 2 shows the block diagram of the main components of the evaluation board.

In this evaluation board, the ADG5462F passes signals from either the source or drain connectors. The source pins have fault detection circuitry that react to an overvoltage event. During an overvoltage event, the channel on which the fault occurs turns off, and the FF pin pulls low. See the ADG5462F data sheet for more details.

POWER SUPPLY

Connector J3 provides access to the supply pins of the ADG5462F. VDD, GND, and VSS link to the appropriate pins on the ADG5462F. For dual-supply voltages, the EVAL-ADG5462FEBZ is powered from ±5 V to ±22 V. For single-supply voltages, the GND and VSS terminals are connected together to power the EVAL-ADG5462FEBZ from 8 V to 44 V. Additionally, an on-board LDO regulator provides the digital control voltage. If necessary, connect a secondary voltage source to EXT_VL and use it to control the digital voltages. To use EXT_VL, move the 0 Ω resistor from R20 to R21. Do not expose the on-board LDO regulator to voltages greater than 28 V; remove R18 and supply an alternative digital voltage via EXT_VL, if required.

INPUT SIGNALS

Two screw connectors connect to both the source and drain pins of the ADG5462F. Additional subminiature Version B (SMB) connector pads are available if extra connections are required. The ADG5462F is overvoltage protected on the source side, and each source terminal (S1 to S4) can be presented with a voltage of up to +55 V or to −55 V. See the ADG5462F data sheet for more details.

Each trace on the source and drain side includes two sets of 0603 pads, which place a load on the signal path to ground. A 0 Ω resistor is placed in the signal path and can be replaced with a user defined value. The resistor combined with the 0603 pads creates a simple resistor capacitor (RC) filter.

OUTPUT SIGNALS

The FF pin indicates when the device is operating normally or whether there is an overvoltage fault on one of the source pins.

For visual indication, LEDs are mounted on the EVAL-ADG5462FEBZ. When the device operates normally, the FF pin remains high, and LED1 illuminates green. If an overvoltage occurs at any of the source pins, the FF pin pulls low, and LED2 illuminates red.

JUMPER SETTINGS

SWITCHES AND 0 Ω RESITORS

The switches manually control the ADG5462F, and 0 Ω resistors configure the digital control voltage, the voltage present on POSFV and NEGFV, to isolate the LED from the rest of the system.

Use SW1 to configure the DR pin. The RAILS position is tied to GND and enables the drain to pull to POSFV or NEGFV during an overvoltage fault condition. The O/C position is tied to VL, and the drain is open-circuit condition.

R18 connects the on-board LDO regulator to the VDD supply. Remove this resistor to protect the LDO regulator from voltages higher than 28 V. Move the 0 Ω resistor R20 to R21 to use an alternative digital voltage connected to EXT_VL.

Resistors R14 and R36 connect the LEDs to the digital power supply, and Resistors R37 and R13 connect the FF pin of the ADG5462F to the LED controls.

Resistors R34, R39, and R41 configure POSFV to either the voltage present on POSFV on J4 (VDD) or VL. Resistors R35, R40, and R42 configure NEGFV to either VSS, the voltage present on NEGFV on J4, or GND.

SMB CONNECTORS

The DR SMB connector can allow control via the external control signals.

The FF SMB connector can access the FF digital output from the ADG5462F.

Table 1. Switch and 0 Ω Resistor Descriptions

Label	Position	Description
SW1	O/C	Logic 1 on DR pin
	RAILS	Logic 0 on DR pin
R35, R40, R42	R35	NEGFV set to VSS
	R40	NEGFV set to voltage on J4 NEGFV screw terminal
	R42	NEGFV set to GND
R34, R39, R41	R34	POSFV set to voltage on J4 POSFV screw terminal
	R39	POSFV set to VDD
	R41	POSFV set to VL
R20, R21	R20	On-board LDO regulator digital voltage
	R21	EXT_VL digital voltage
R18	Inserted	LDO regulator powered up
	Removed	LDO regulator unpowered
R37, R13	Inserted	FF pin connected to LED
	Removed	FF pin disconnected from LED
R14, R36	Inserted	LED connected to digital supply
	Removed	LED isolated
R15	Inserted	1 kΩ pull-up resistor at FF pin
	Removed	No external pull-up resistor at FF pin

EVALUATION BOARD SCHEMATICS AND ARTWORK

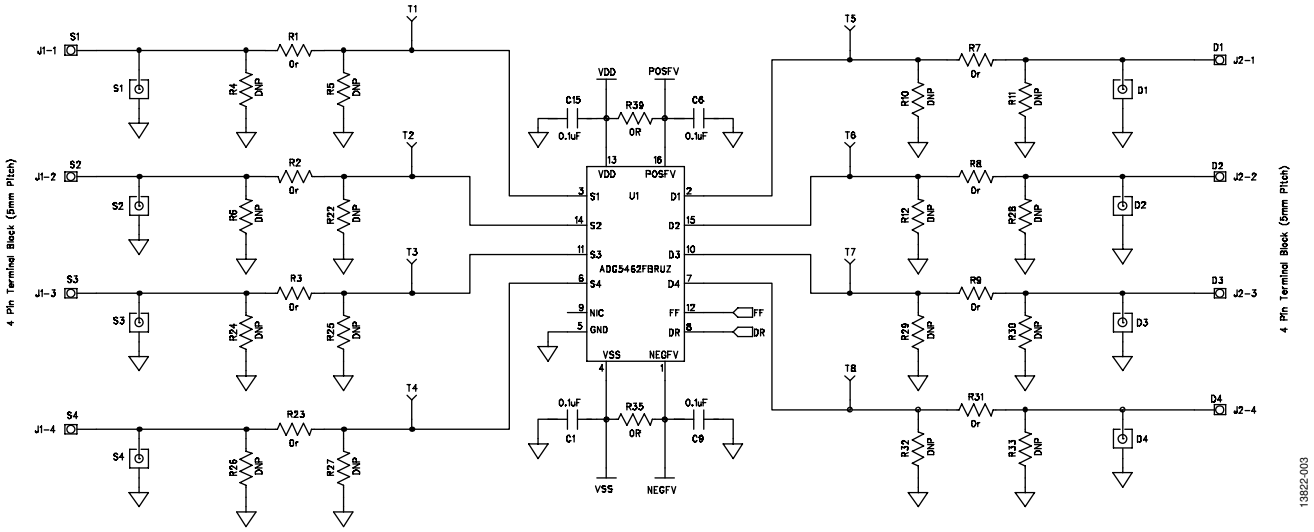

Figure 3. EVAL-ADG5462FEBZ Evaluation Board Schematic (Part 1)

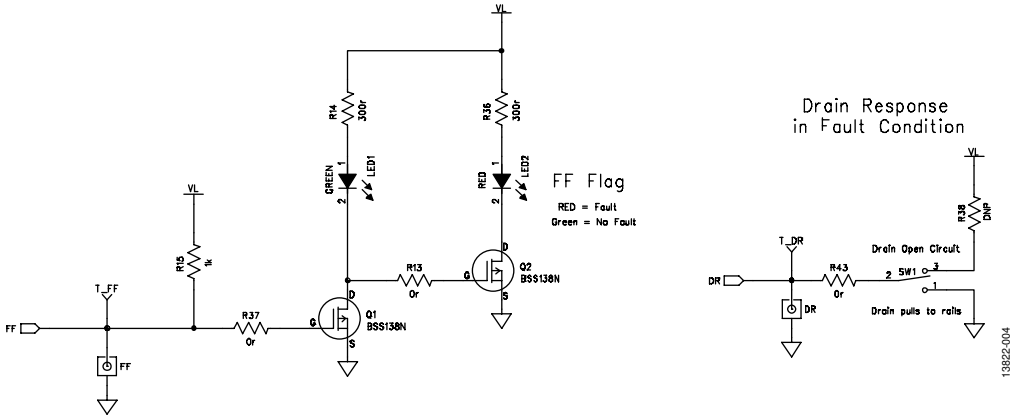

Figure 4. EVAL-ADG5462FEBZ Evaluation Board Schematic (Part 2)

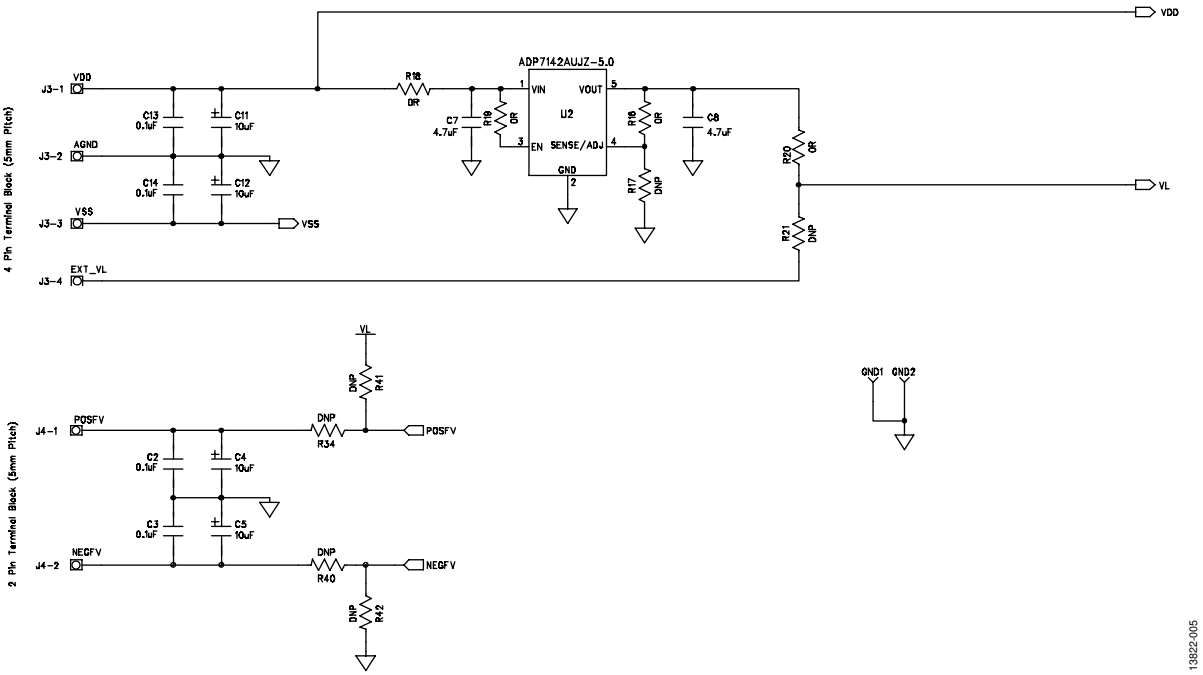

Figure 5. EVAL-ADG5462FEBZ Evaluation Board Schematic (Part 3)

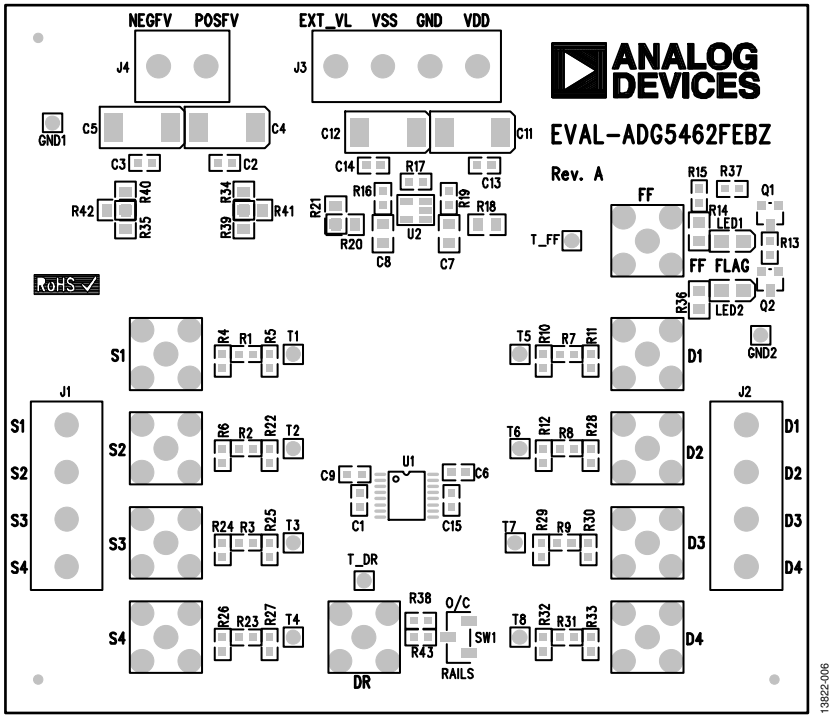

Figure 6. EVAL-ADG5462FEBZ Silk Screen

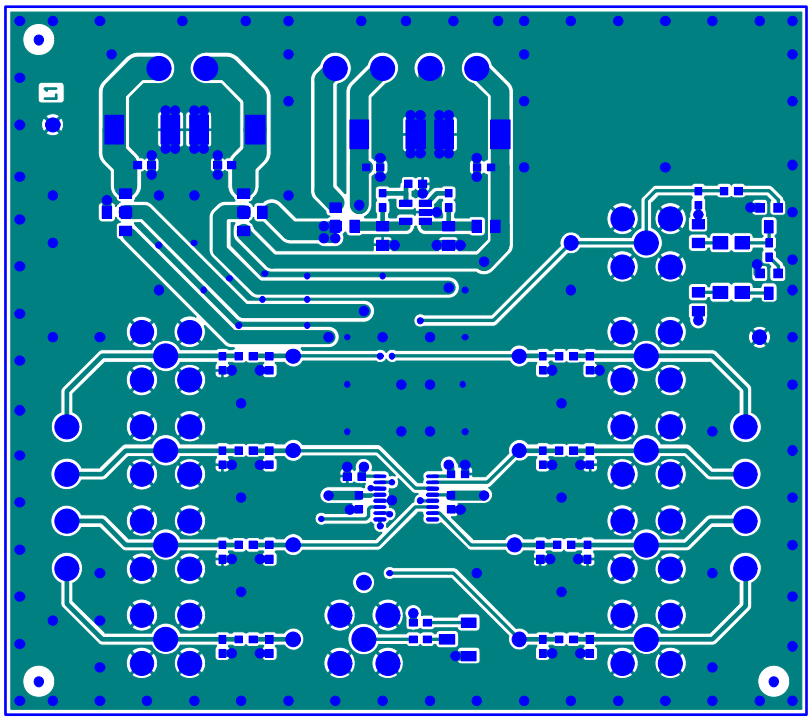

Figure 7. EVAL-ADG5462FEBZ Top Layer

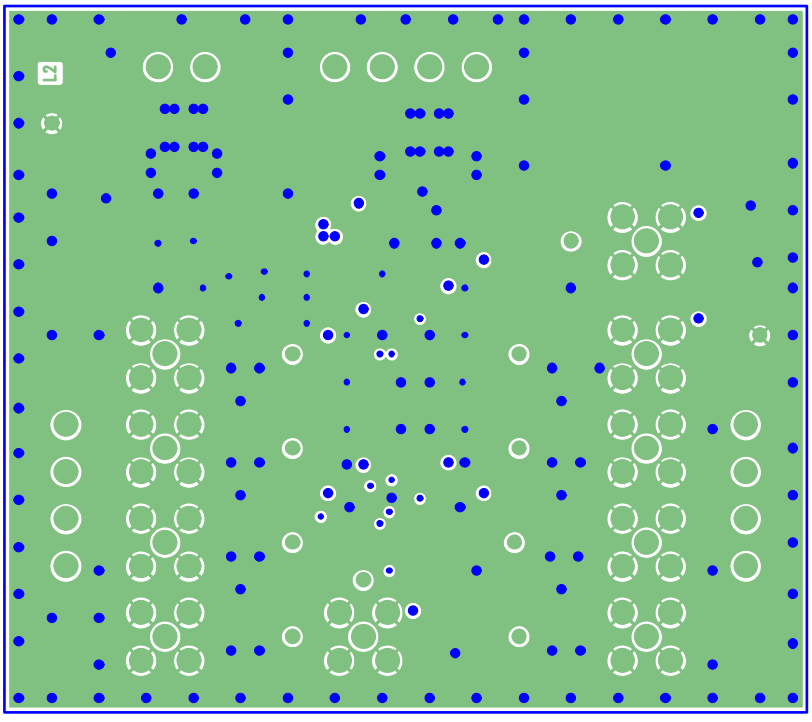

Figure 8. EVAL-ADG5462FEBZ Layer 2

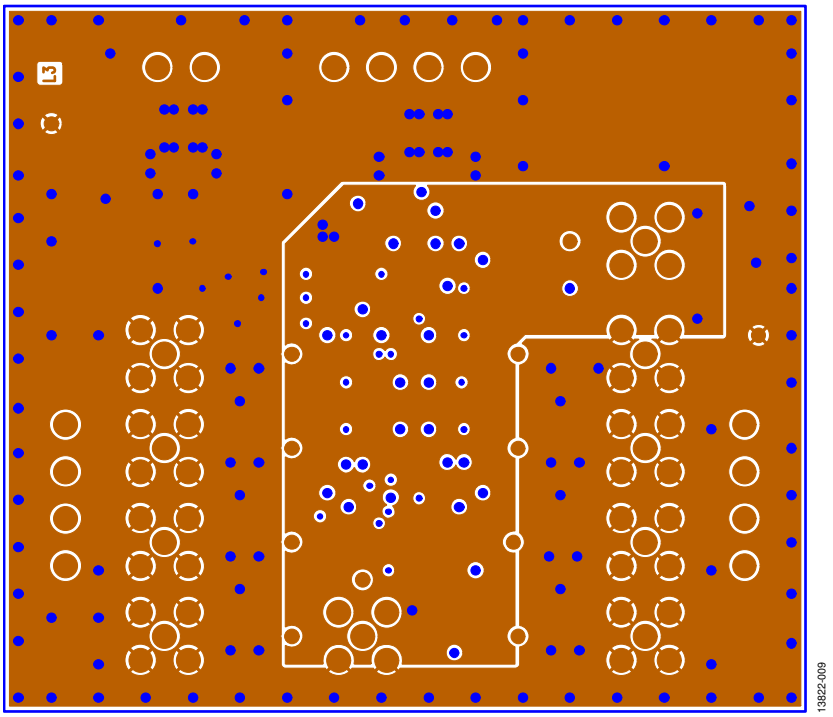

Figure 9. EVAL-ADG5462FEBZ Layer 3

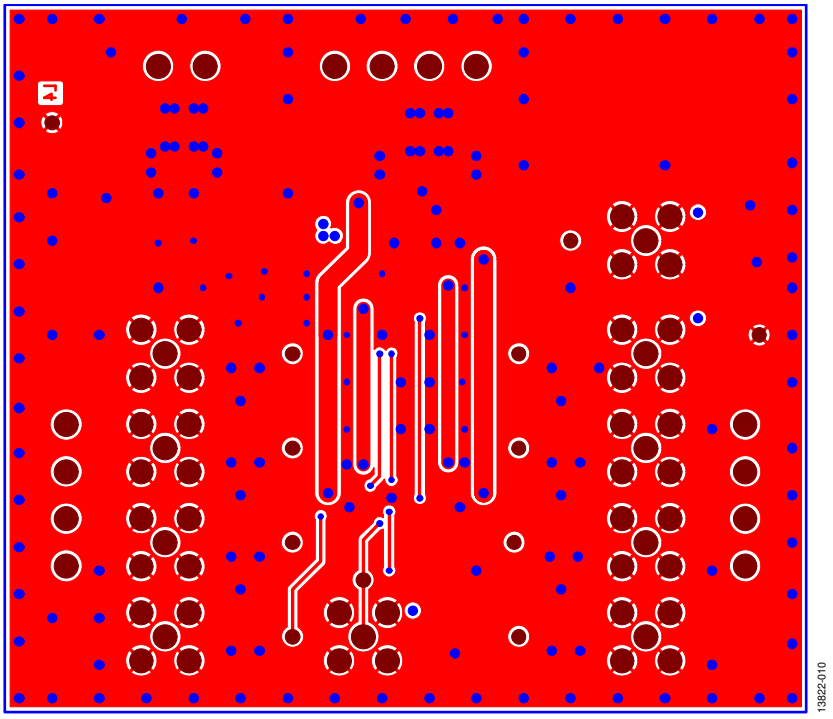

Figure 10. EVAL-ADG5462FEBZ Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Reference Designator	Description	Manufacturer Part No.	Stock Code
C1 to C3, C6, C9, C13 to C15	50 V, X7R, 0.1 µF multilayer ceramic capacitors, 0603	GRM188R71H104KA93D	FEC 882-0023
C4, C5, C11, C12	50 V, 10 µF tantalum capacitors, D size	TAJD106K050RNJ	FEC 143-2387
C7, C8	4.7 µF ceramic multilayer capacitors	C2012X5R1H475K125AB	FEC 2346932
D1 to D4, S1 to S4	50 Ω SMB sockets	Not applicable	Do not insert
DR, FF	50 Ω straight SMB jacks	SMB1251B1-3GT30G-50	FEC 1111349
GND1, GND2	Black test points	20-2137	FEC 873-1128
J1 to J3	4-pin terminal blocks (5 mm pitch)	CTB5000/4	FEC 151791
J4	2-pin terminal block (5 mm pitch)	CTB5000/2	FEC 151789
LED1	LED, SMD green, 0805	KP-2012SGC	FEC 1318243
LED2	LED, SMD red, 0805	KP-2012SRC-PRV	FEC 1318244
Q1, Q2	Transistors, N-MOSFET, 60 V, 0.23 A, SOT-23	BSS138N	FEC 115-6434
R1 to R3, R7 to R9, R13, R16, R19, R23, R31, R37, R43	Resistors, 0603, 1%, 0 Ω	MC0063W06030R	FEC 9331662
R4 to R6, R10 to R12, R17, R22, R24 to R30, R32, R33, R38	SMD resistors, 0603	Not applicable	Do not insert
R14, R36	Resistors, 300 Ω, 0.1 W, 1%, 0805	MC01W08051300R	FEC 9332987
R15	Resistor, 1 kΩ, 0.063 W, 1%, 0603	MC0063W060311K	FEC 9330380
R18, R20, R35, R39	Resistors, 0805, 1%, 0 Ω	MC01W08050R	FEC 9333681
R21, R34, R40 to R42	SMD resistors, 0805	Not applicable	Do not insert
SW1	SPDT, SMT slide switch	Digi-Key CAS-120TA	CAS120JCT-ND
T1 to T8, T_DR, T_FF	Red test points	20-313137	FEC 873-1144
U1	User defined fault protection and detection, 10 Ω R_{ON}, quad channel protector	ADG5462F	ADG5462FBRUZ
U2	40 V, 200 mA, low noise, CMOS LDO linear regulator	ADP7142AUJZ-5.0	ADP7142AUJZ-5.0-R7

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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