



iCEstick Evaluation Kit

User's Guide

Introduction

Thank you for choosing the Lattice Semiconductor iCEstick™ Evaluation Kit.

This guide describes how to start using the iCEstick Evaluation Kit, an easy-to-use USB form factor board for rapidly prototyping designs using the iCE40 FPGA. Along with the evaluation board, this kit includes a pre-loaded design that demonstrates basic board functionality.

The contents of this user's guide include demo operations, descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, a complete set of schematics and bill of materials for the iCEstick Evaluation Board.

Features

The iCEstick Evaluation Kit includes:

- iCEstick Evaluation Board – features the following on-board components
 - High-performance, low-power iCE40HX1K FPGA
 - FTDI 2232H USB device allows iCE device programming and UART interface to a PC
 - Vishay TFDU4101 IrDA transceiver
 - Five user LEDs
 - 2 x 6 position Diligent Pmod™ compatible connector enables many other peripheral connections
 - Discera 12Mhz MEMS oscillator
 - Micron 32Mbit N25Q32 SPI flash
 - Supported by Lattice iCEcube2™ design software
 - USB connector provides the power supply
 - 16 LVCMOS/LVTTL (3.3V) digital I/O connections on 0.1" through-hole connections
- Pre-loaded demo design – the kit includes the pre-loaded demo design that flashes the on-board LEDs in a clockwise pattern.
- USB connector – provides a communication and debug port via a USB-to-RS-232 physical channel and programming interface to the PC.

Figure 1. iCEstick Evaluation Board

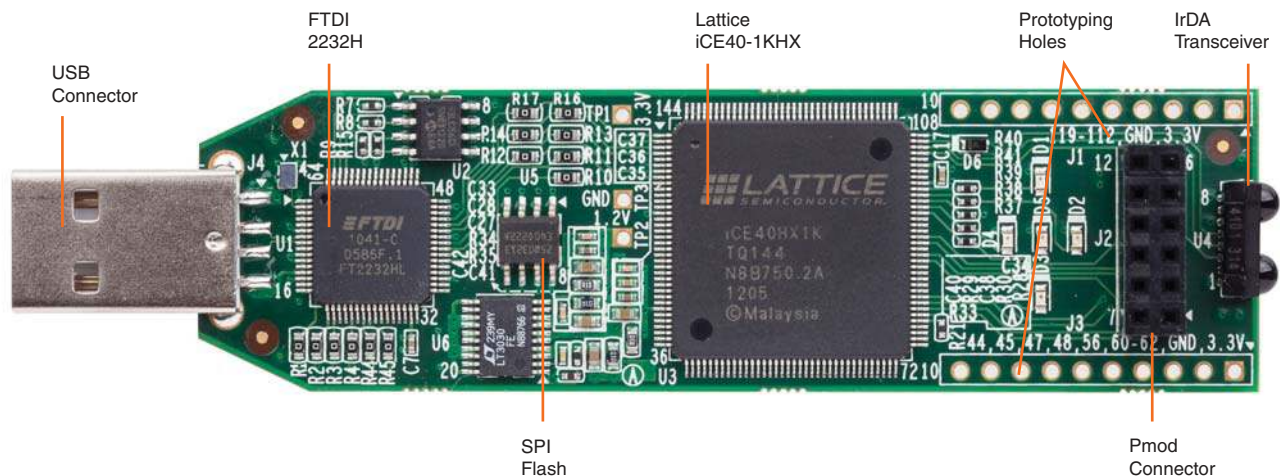
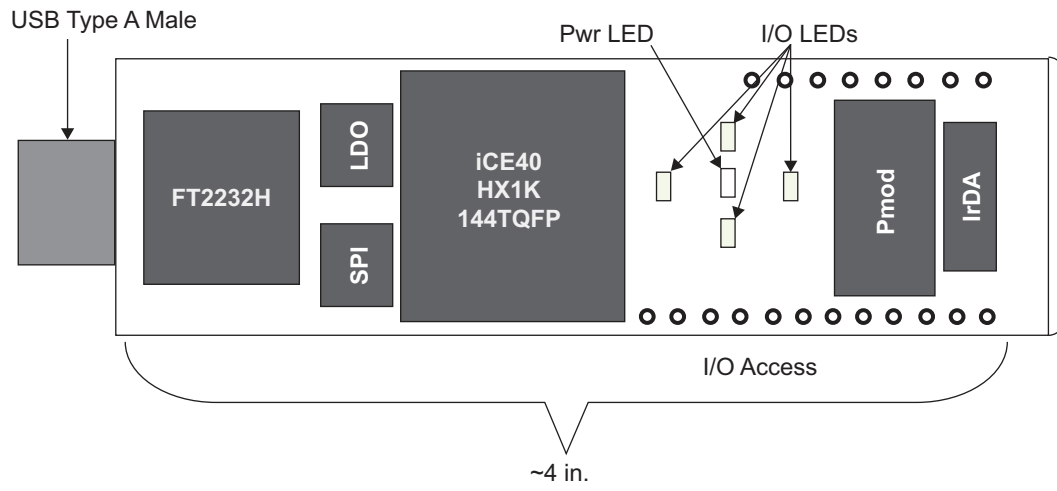


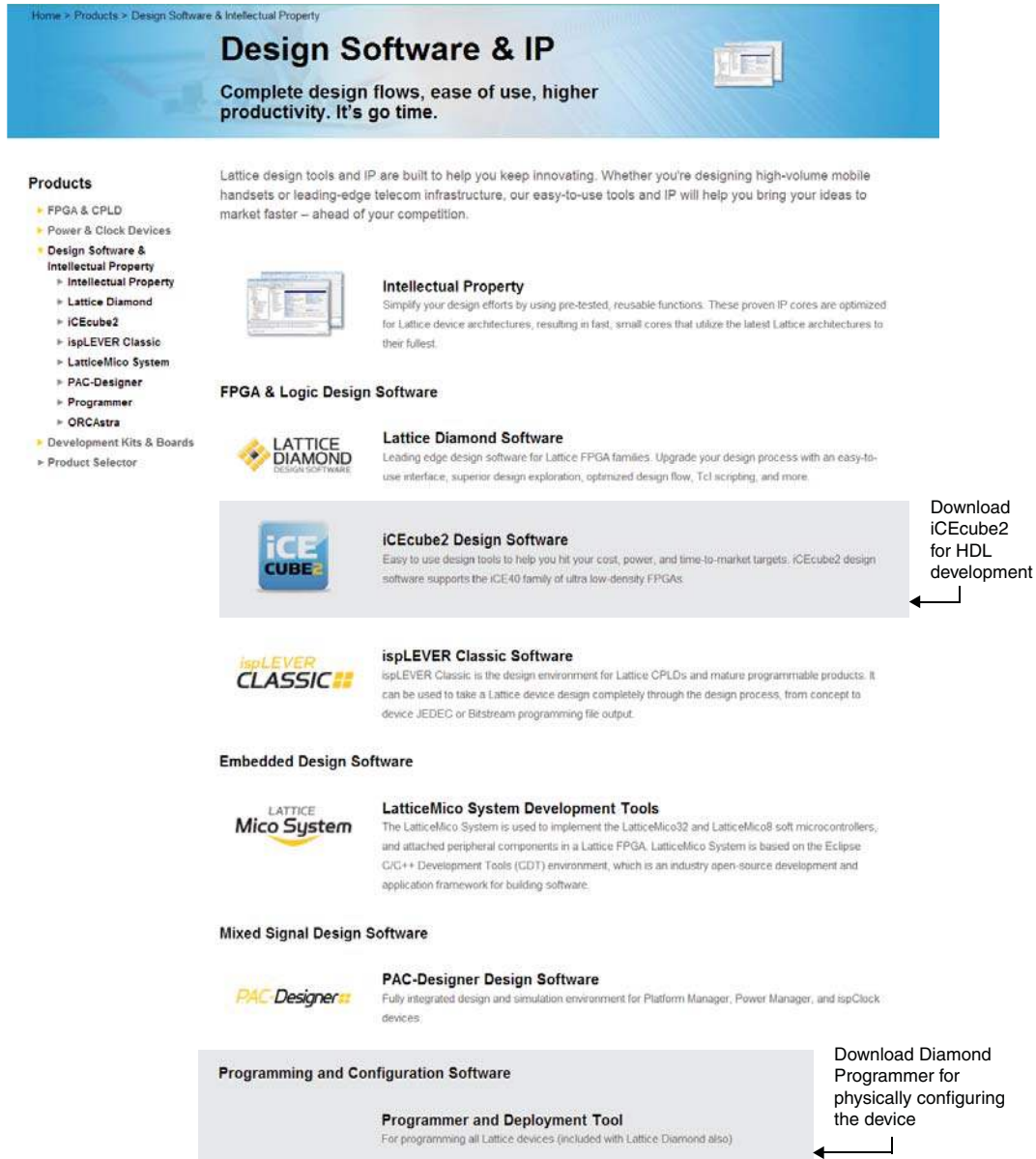
Figure 2. iCEstick Functional Block Diagram



Software Requirements

Before using the iCEstick board, download and install the latest version of Lattice iCEcube2™ and Diamond Programmer. Make sure you log in to the Lattice website, otherwise these software downloads will not be visible. These are available at <http://www.latticesemi.com/Products/DesignSoftwareAndIP.aspx>. If you install Diamond Programmer 2.2, you will require a software patch. This software patch is available at <http://www.lattice-semi.com/icestick>. Go to the Downloads tab and install the appropriate patch. This patch is not required with Diamond Programmer 3.0 or higher.

Figure 3. Software Downloads



The screenshot shows the Lattice website's 'Design Software & IP' section. On the left is a navigation menu under 'Products' with categories like FPGA & CPLD, Power & Clock Devices, Design Software & Intellectual Property, and Development Kits & Boards. The main content area is titled 'Design Software & IP' and includes a sub-header 'Complete design flows, ease of use, higher productivity. It's go time.' Below this, there are several software categories with descriptions and icons:

- Intellectual Property:** Simplify your design efforts by using pre-tested, reusable functions. These proven IP cores are optimized for Lattice device architectures, resulting in fast, small cores that utilize the latest Lattice architectures to their fullest.
- FPGA & Logic Design Software:**
 - Lattice Diamond Software:** Leading edge design software for Lattice FPGA families. Upgrade your design process with an easy-to-use interface, superior design exploration, optimized design flow, Tcl scripting, and more.
 - iCEcube2 Design Software:** Easy to use design tools to help you hit your cost, power, and time-to-market targets. iCEcube2 design software supports the iCE40 family of ultra low-density FPGAs. *Annotation: Download iCEcube2 for HDL development*
 - ispLEVER Classic Software:** ispLEVER Classic is the design environment for Lattice CPLDs and mature programmable products. It can be used to take a Lattice device design completely through the design process, from concept to device JEDEC or Bitstream programming file output.
- Embedded Design Software:**
 - LatticeMico System Development Tools:** The LatticeMico System is used to implement the LatticeMico32 and LatticeMico8 soft microcontrollers, and attached peripheral components in a Lattice FPGA. LatticeMico System is based on the Eclipse C/C++ Development Tools (CDT) environment, which is an industry open-source development and application framework for building software.
- Mixed Signal Design Software:**
 - PAC-Designer Design Software:** Fully integrated design and simulation environment for Platform Manager, Power Manager, and ispClock devices.
- Programming and Configuration Software:**
 - Programmer and Deployment Tool:** For programming all Lattice devices (included with Lattice Diamond also). *Annotation: Download Diamond Programmer for physically configuring the device*

Communication Between the PC and iCEstick

Communication between the iCEstick Board and a PC is via the FTDI 2232H USB device. To enable this connection the installation of the FTDI chip USB hardware drivers is needed. This driver is installed when Diamond Programmer was installed. These drivers enable the computer to recognize and program the iCEstick board. In addition these drivers allow communication between the PC and the iCEstick board to enable further demonstrations.

Connecting the iCEstick Evaluation Board

Insert the iCEstick evaluation board to an open USB slot in a PC. The default bitstream in the SPI flash loads the iCE40HX-1k device on the iCEstick board. One should see the green LED on the board light up and continue to be lit.

Preprogrammed Design and Board LEDs

There are a total of 5 LEDs on the iCEstick board. All are controlled by I/Os of the iCE40HX-1k device. The default bitstream loads the iCE40HX-1k device and the green LED lights up signifying that the device has loaded correctly and power is good. The other four red LEDs arranged in a diamond pattern begins to flash in a clockwise direction. This is the intended function of the default bitstream.

Table 1. User I/O and LEDs

LED location	CPLD pin (All in Bank 1)	CPLD I/O	LED color
D1	99	PIO1_14	Red
D2	98	PIO1_13	Red
D3	97	PIO1_12	Red
D4	96	PIO1_11	Red
D5	95	PIO1_10	Green

Download Demo Designs

The above demo is pre-programmed into the iCEstick board. Other than the default design, Lattice also distributes source and programming files for demonstration designs compatible with this board. To download the demo designs:

1. Browse to www.latticesemi.com/icestick and click on the Downloads tab to view other design files and capabilities that the iCEstick board could implement. Various demo designs are available and can be download.
2. Extract the contents of zip files to a local hard drive.

Lattice provides the following demos based on iCEstick board:

- UART over IrDA. In this demo design, the iCEstick device communicates with a laptop or PC through UART over USB. Then, the payload is transmitted through Vishay IrDA device. This data can be locally looped back or another iCEstick board could receive the data via it's IrDA receiver.
- Diligent Pmod Accelerometer. The demo makes use of Diligent PmodAcl module which is plugged into iCEstick board. In this demo design, the accelerometer setting and reading is done by the on-board iCE device and the direction of movement is displayed with the diamond pattern LEDs.

IrDA Functionality and Demo

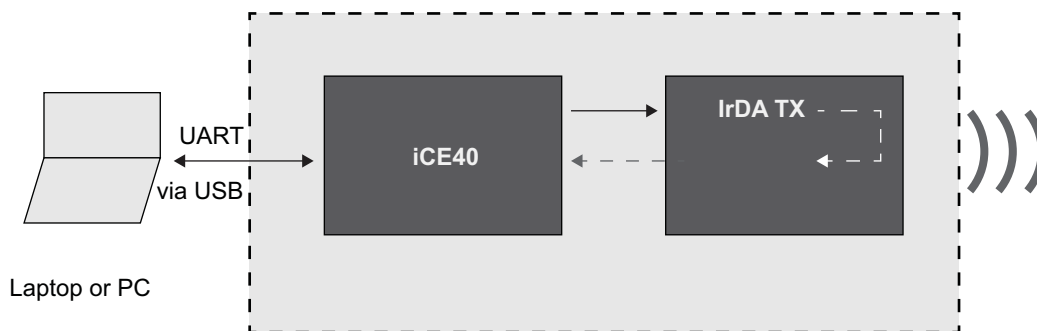
The iCEstick board has a Vishay TFDU4101 IrDA transceiver on it. This device allows transmit and receive of infrared data up to 115kbps.

Table 2. IrDA Pin Description

IrDA function	CPLD pin	CPLD I/O	Comment
RXD	106	PIO1_19	Receive data pin
TXD	105	PIO1_18	Transmit data pin
SD	107	PIO1_20	Shut down

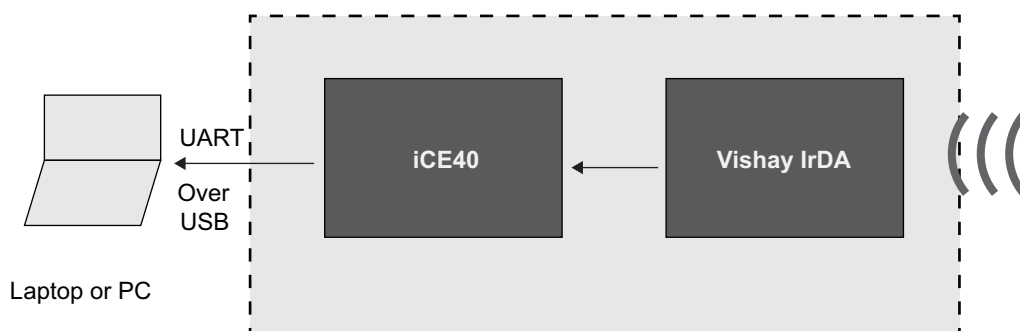
There are two possible configurations for the IrDA demo design: IrDA TX and IrDA RX. For an end to end complete IrDA link demo, two iCEstick boards are needed, however using just the IrDA Tx design can support a demo. The IrDA TX design transfers the data from the PC keyboard input in a terminal window to the IrDA Vishay device TXD. While the data is transmitted via infrared, it is also by default looped back to the receive channel of the IrDA device. In this demo the looped back data is received and before it is transmitted to the PC window the text is converted from lower case to upper case. This is the signal flow for the stand alone demo.

Figure 4. IrDA TX on iCEstick



The IrDA RX design receives infrared data from the Vishay IrDA Tx device. After the IrDA data is wirelessly received it is then sent to the iCE40 device. The iCE40 then send the character information to the open window on the PC. Thus whatever is typed in the TX terminal window is displayed in the Rx terminal window.

Figure 5. IrDA RX on iCEstick



This demo requires a terminal program on PC to communicate with the iCEstick board. The following instructions describe the setup for IrDA TX stand alone demo using the Tera Term terminal emulator program on Windows 7.

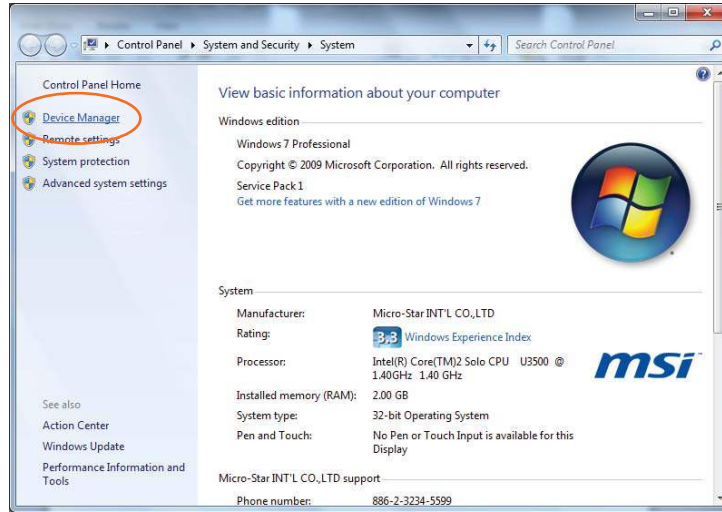
Setting Up for the IrDA TX Stand Alone Demo

To set up for the IrDA TX demo:

1. Program the iCE device with IrDA TX bitstream.
2. Plug iCEstick into a PC USB port.
3. Check if the USB driver is installed correctly.

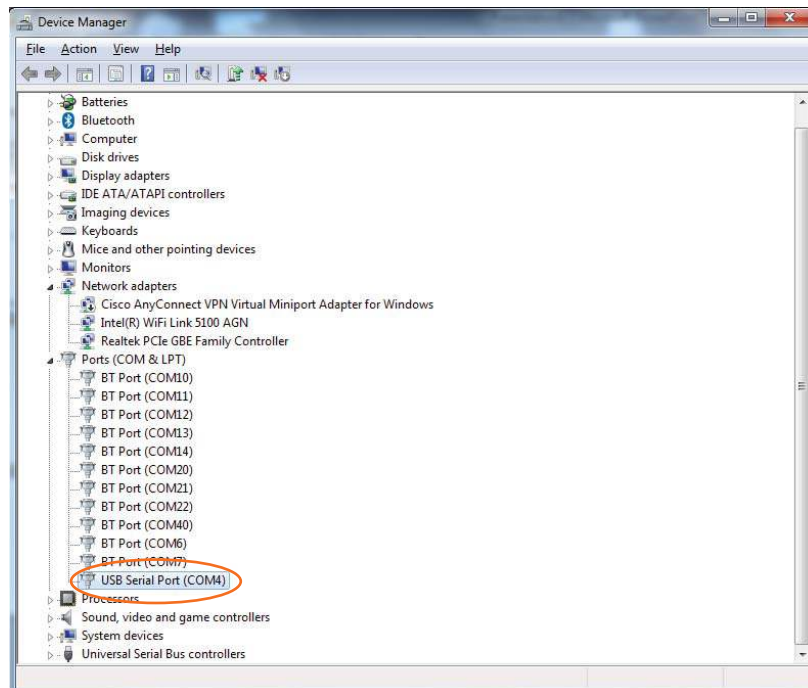
Go to **Start**, right-click **Computer** and select **Properties**. The System window is shown. Click **Device Manager**.

Figure 6. System Window



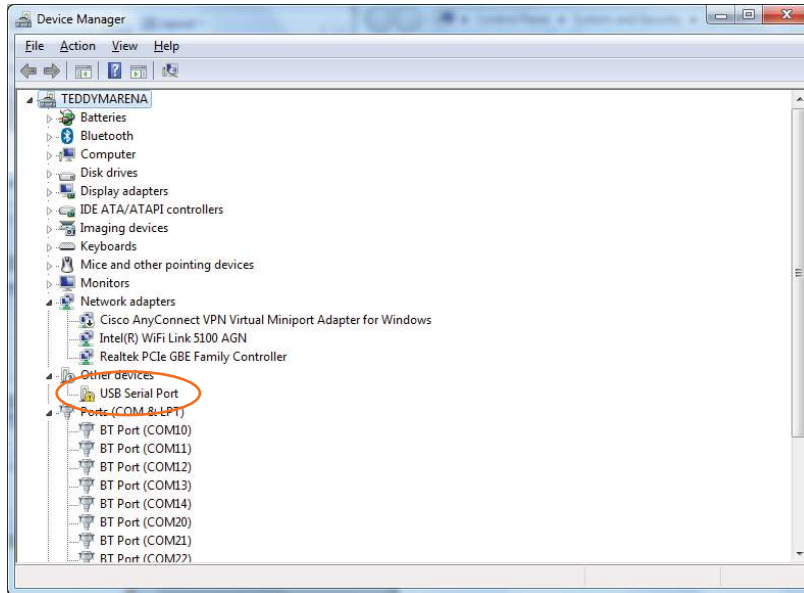
4. If the driver is installed correctly, the device is listed without an error tag under Ports (COM & LPT) as shown in Figure 7. Proceed to the next step.

Figure 7. Device Manager



If the driver is not installed correctly, the device is tagged with a yellow exclamation point as shown in Figure 8. You need to install the driver. To do this, right-click the device and select **Update Driver Software**.

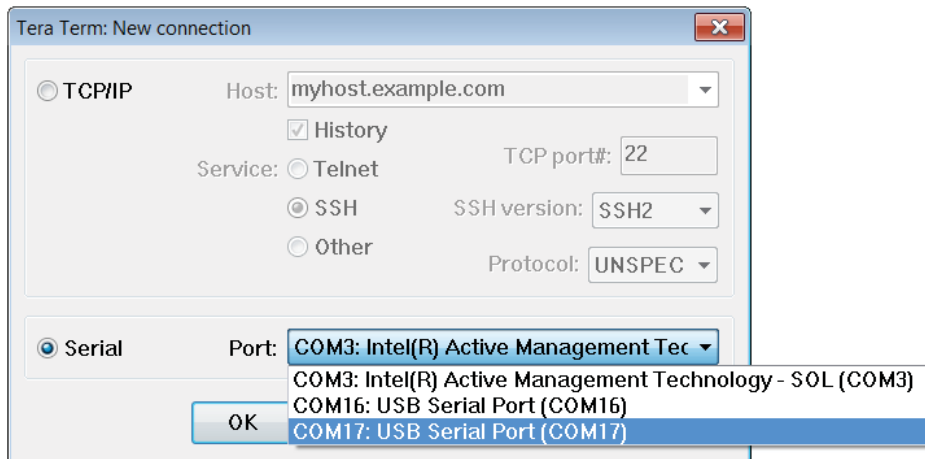
Figure 8. Device Manager with Driver Error



Request Windows to search the web for the driver. After Windows locates the FTDI driver, install it and proceed to the next step.

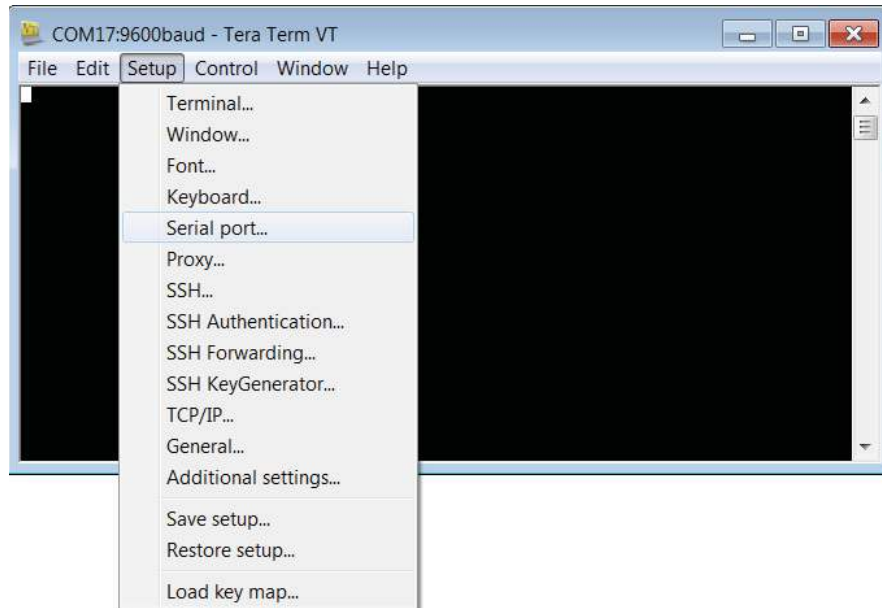
5. Install Tera Term software. The installer can be downloaded from http://download.cnet.com/Tera-Term/3000-20432_4-75766675.html.
6. Open Tera Term.
7. In the New connection dialog box, click **Serial**.
8. On the Port menu, click **COMxx: USB Serial Port (COMxx)**. If there are two or more options, select the last COM port on the list. Click **OK**.

Figure 9. New Connection Dialog Box



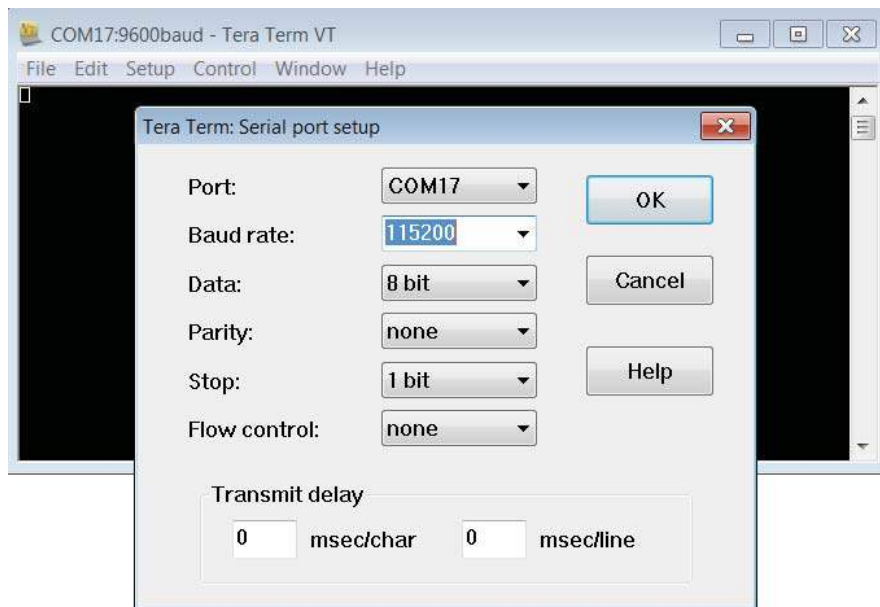
9. The selected COM port/default baud rate appear in the Tera Term VT window title bar as shown in Figure 10. On the Setup menu, click **Serial port**.

Figure 10. Tera Term VT Window with Selected COM Port /Default Baud Rate



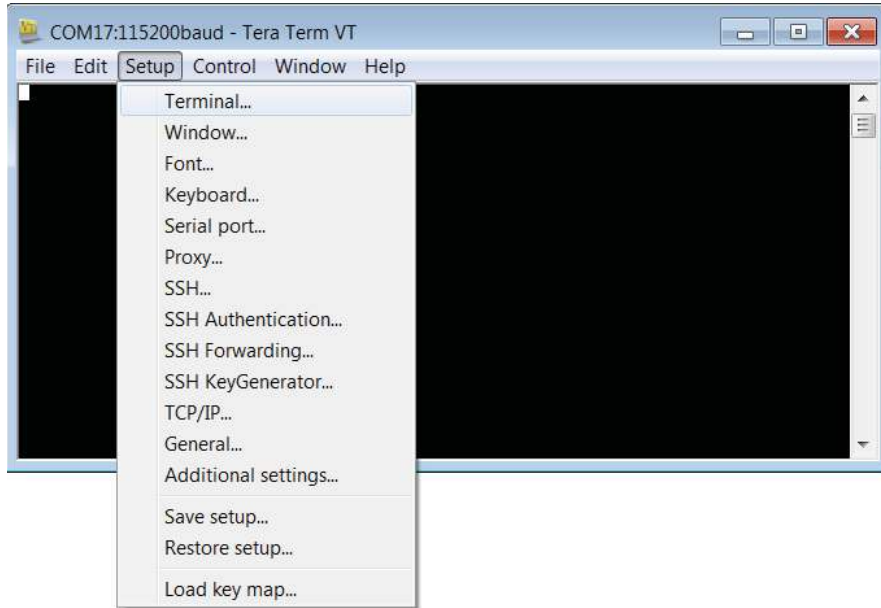
10. The Serial port setup dialog box opens. In the Baud rate menu, click **115200**. Leave other options with default settings. Click **OK**.

Figure 11. Serial Port Setup Dialog Box



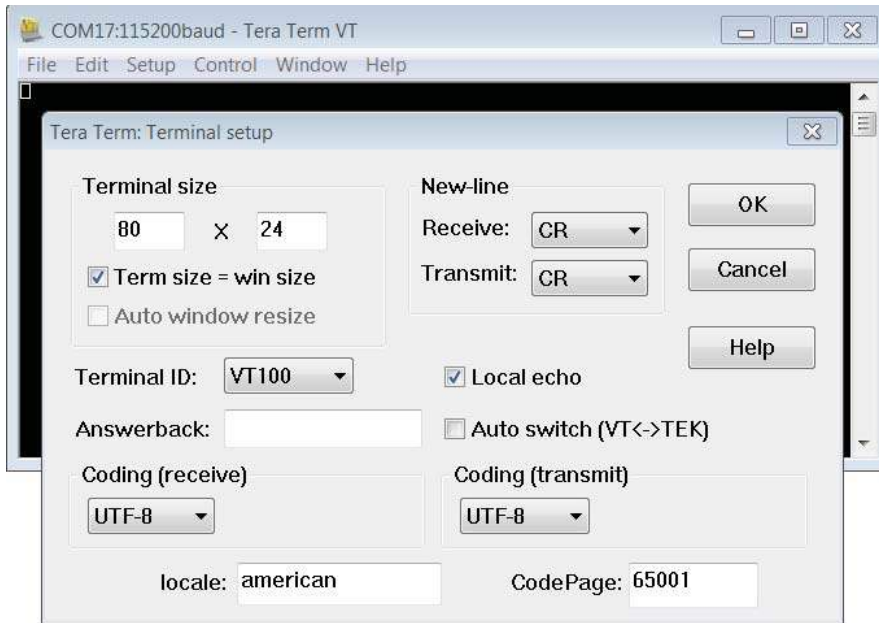
11. The selected COM port/115200 baud rate appear in the Tera Term VT window title bar as shown in Figure 12. On the Setup menu, click **Terminal**.

Figure 12. Tera Term VT Window with Selected COM Port /Baud Rate



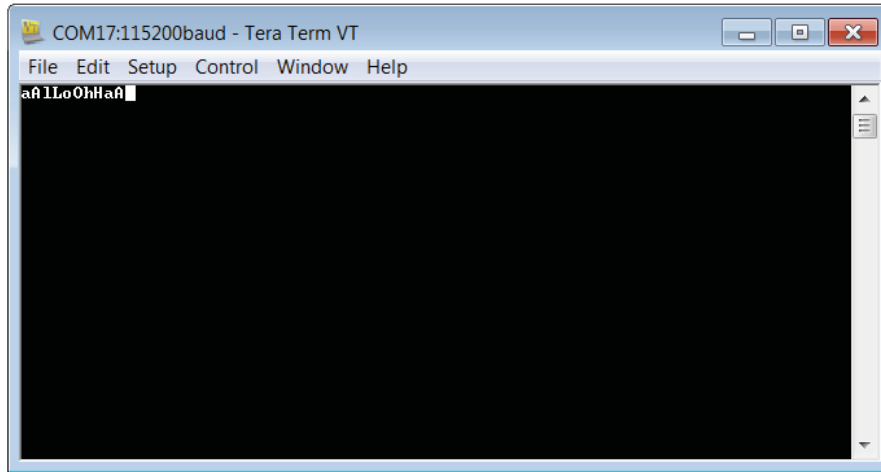
12. The Terminal setup dialog box opens. Select **Local echo**. Leave other options with default value. Click **OK**.

Figure 13. Terminal Setup Dialog Box



When you type in the Tera Term VT window using the TX design, a lower case character is echoed with a capital character from the iCE device as shown in the Figure 14.

Figure 14. Tera Term VT Window Using TX Design



For IrDA RX, the above Tera Term setting is the same but the bitstream for the iCE device is different. With a setup of two iCEstick boards facing each other, one programmed with IrDA TX and the other programmed with IrDA RX, the character typed in IrDA TX PC is transferred to and displayed on IrDA RX PC monitor. You can change the angle of the TX board facing the RX board to see when the IrDA link would break.

Diligent Pmod Connector and Accelerometer Demo

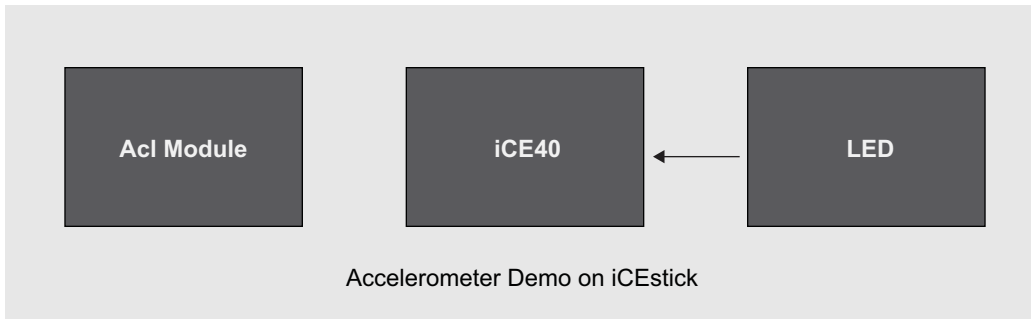
On the iCEstick board, location J2 is a 2x6 position Pmod (Peripheral MODule) Digilent connector. The iCEstick board supports a variety of Pmod peripheral modules for easy I/O expansion. Figure 3 lists the 0.1” through-hole headers on the iCEstick board that support Pmod modules. Pmod modules come in different form factors, and each Pmod header includes power and ground supplies. The easiest way to support a Pmod module is to add the appropriate female socket. Straight-through or right-angle connectors can be used. Male headers are an alternate solution when using the interface cable provided with most Pmod modules.

Table 3. Diligent Pmod Compatible Connector Description

Connection	Left Row pins	Right Row pins	Connection
PIO1_02	1	7	PIO1_06
PIO1_03	2	8	PIO1_07
PIO1_04	3	9	PIO1_08
PIO1_05	4	10	PIO1_09
Ground	5	11	Ground
3.3v	6	12	3.3v

The Accelerometer demo makes use of the Digilent PmodAcl accelerometer module from Diligent. The PmodAcl module needs to be plugged into J2 on the iCEstick board through the cable that comes with this module. The four LEDs D1, D2, D3 and D4 in the north, south, east and west pattern are configured to represent X+, Z+, X-, Z- of accelerometer movement direction respectively. When the accelerometer module is moved around, the diamond pattern LEDs on the iCEstick board goes on/off corresponding to the direction of the movement and orientation of the module. If all these LEDs light up at the same time (indicating a balance point), The D5 LED also lights up.

Figure 15. Accelerometer Demo on iCEstick

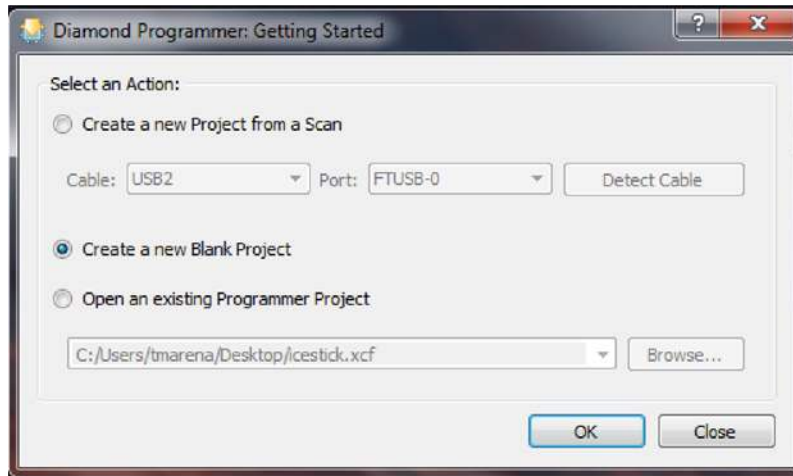


Programming Demo Designs with Lattice Programmer

To program a bitstream file to iCE device:

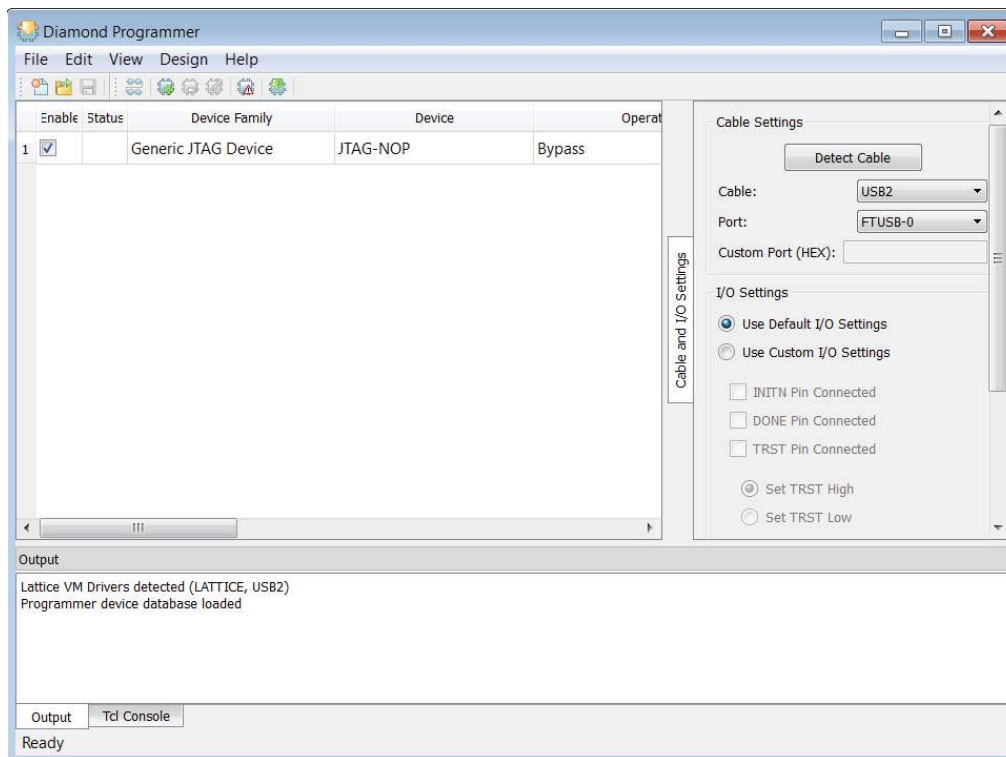
1. Plug the iCEstick board to a USB port on a host PC with Programmer installed.
2. Run Programmer. The Diamond Programmer Getting Started window opens. Under Select an Action, click **Create a new Blank Project**. Click **OK**. If you try to create a new project from a scan, you will receive an error. Please select **Create a new Blank Project**.

Figure 16. Diamond Programmer Getting Started Window



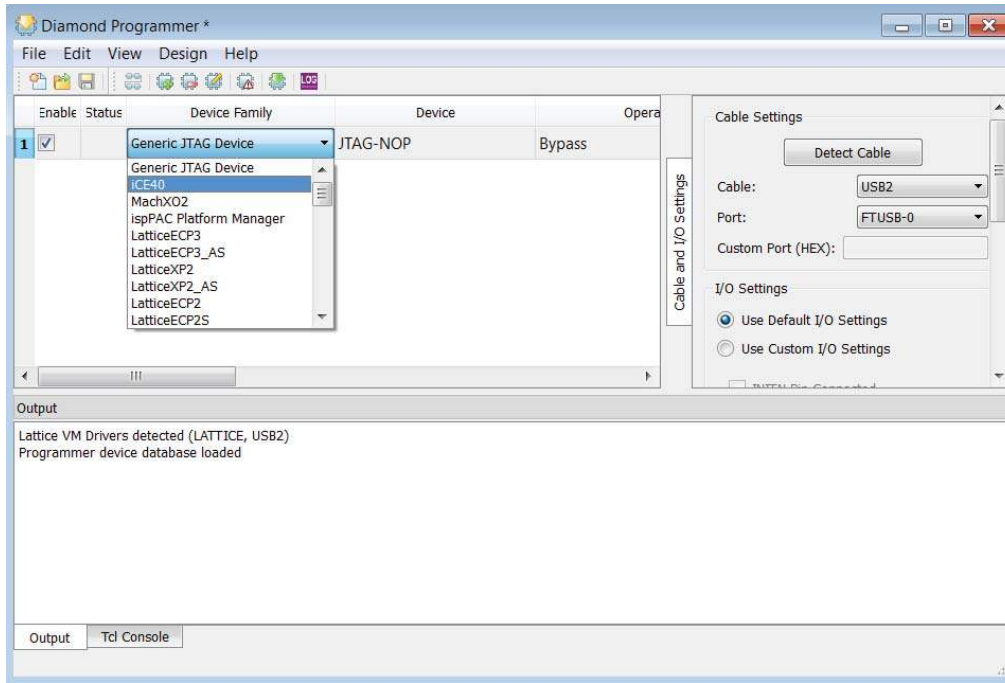
3. The Diamond Programmer interface opens. Under Cable Settings, in the Cable menu, click **USB2**. In the Port menu, click **FTUSB-0**. You can also click **Detect Cable** to set the correct cable and port.

Figure 17. Cable and Port Settings



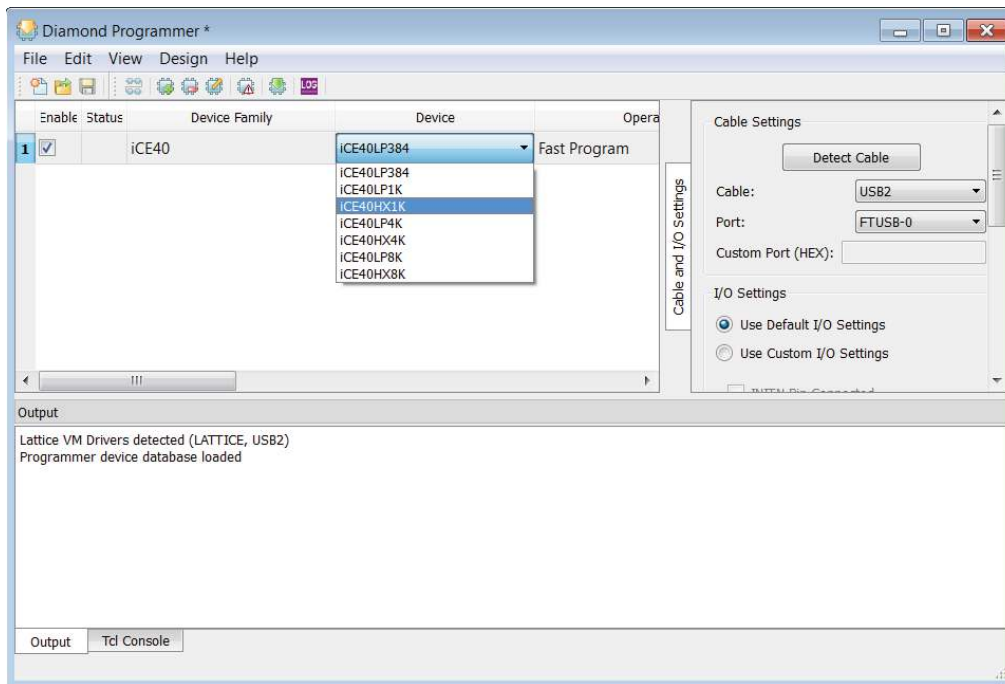
4. Select the **Enable** check box.
5. Double-click the cell under Device Family and click **iCE40**.

Figure 18. Device Family Options



6. Double-click the cell under Device and click **iCE40HX1K**.

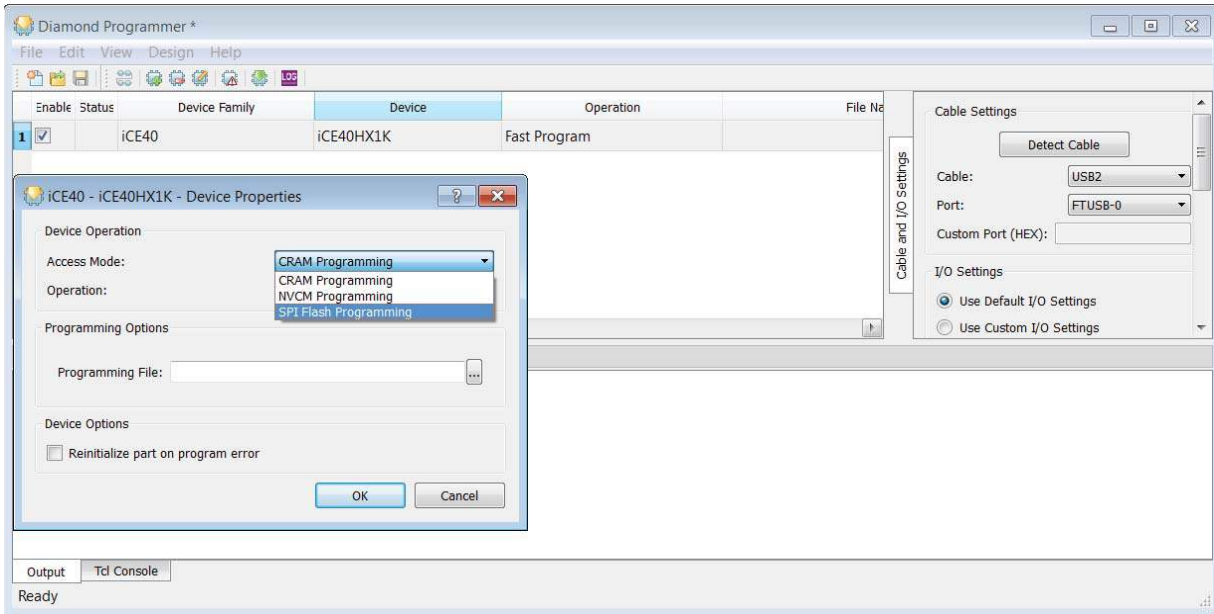
Figure 19. Device Options



7. Double-click the cell under Operation. The Device Properties dialog box opens as shown in Figure 20. On the Access Mode menu, click **SPI Flash Programming**. Click **OK**.

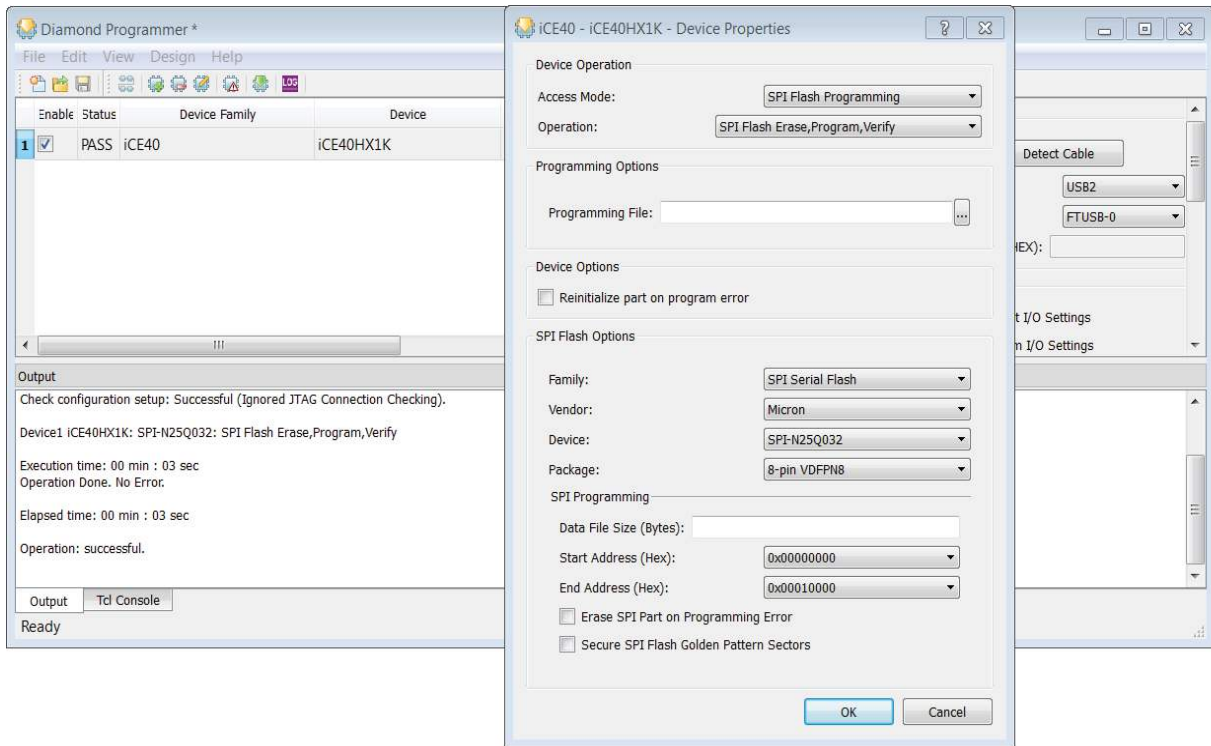
Warning: NVCM Programming is NOT recommended. NVCM Programming is one time programming. If you use NVCM Programming to program iCE device, the iCE device can no longer be reprogrammed.

Figure 20. Device Properties Dialog Box



8. Select the SPI flash part number. For the iCEstick, this is Micron SPI-N25Q032 8-pin VDFPN8 package. Also make sure to select the programming file. Once done, click **OK**.

Figure 21. Select Serial SPI Flash



9. On the Programmer toolbar, click the **Program** button to initiate the download. The bitstream starts downloading to the iCE device. This takes a few seconds to complete.

Expansion I/O Connections

The iCEstick board contains two unpopulated 0.1" headers for users to implement their own connections. Connectors J1 and J3 each consist of 10 positions for a total of 20 connections. Two of these are tied to 3.3v and two are tied to ground. This leaves 16 general purpose I/Os that connect to the iCE40HX-1k device for user I/O.

Table 4. Expansion I/O Connections

J1 Connector			J3 Connector		
Pin	CPLD I/O Bank 0	CPLD Pin	Pin	CPLD I/O Bank 2	CPLD Pin
1	3.3v	-	1	3.3v	-
2	Ground	-	2	Ground	-
3	PIO0_02	112	3	PIO2_17	62
4	PIO0_03	113	4	PIO2_16	61
5	PIO0_04	114	5	PIO2_15	60
6	PIO0_05	115	6	PIO2_14	56
7	PIO0_06	116	7	PIO2_13	48
8	PIO0_07	117	8	PIO2_12	47
9	PIO0_08	118	9	PIO2_11	45
10	PIO0_09	119	10	PIO2_10	44

Test Points

There are three unpopulated test points. TP1 is tied to 3.3v, TP2 is tied to 1.2v and TP3 is connected to ground.

Lattice Demonstration Bitstreams

All demonstration bitstreams and Design files are available at www.latticesemi.com/icestick.

Technical Support Assistance

e-mail: techsupport@latticesemi.com

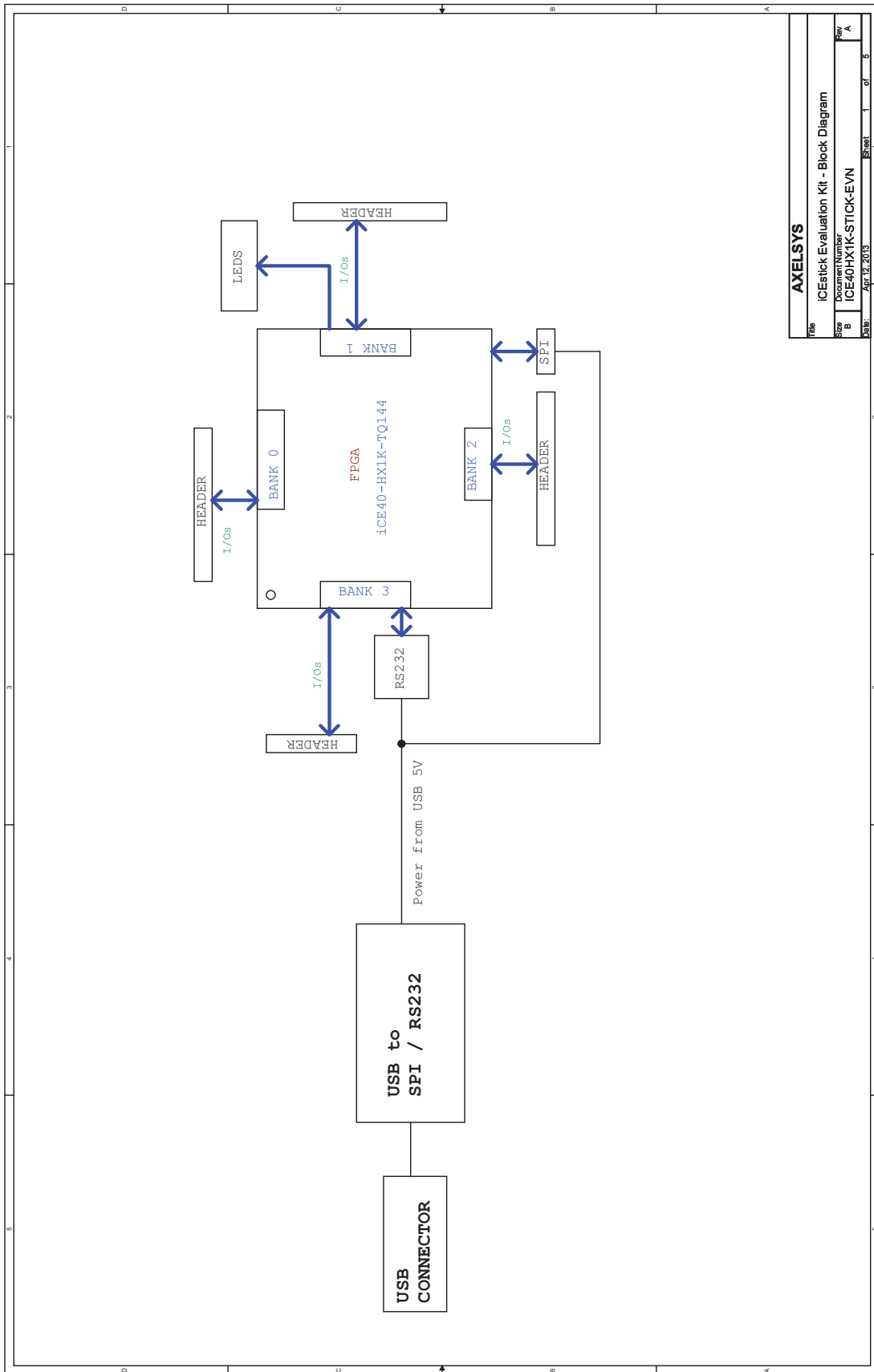
Internet: www.latticesemi.com

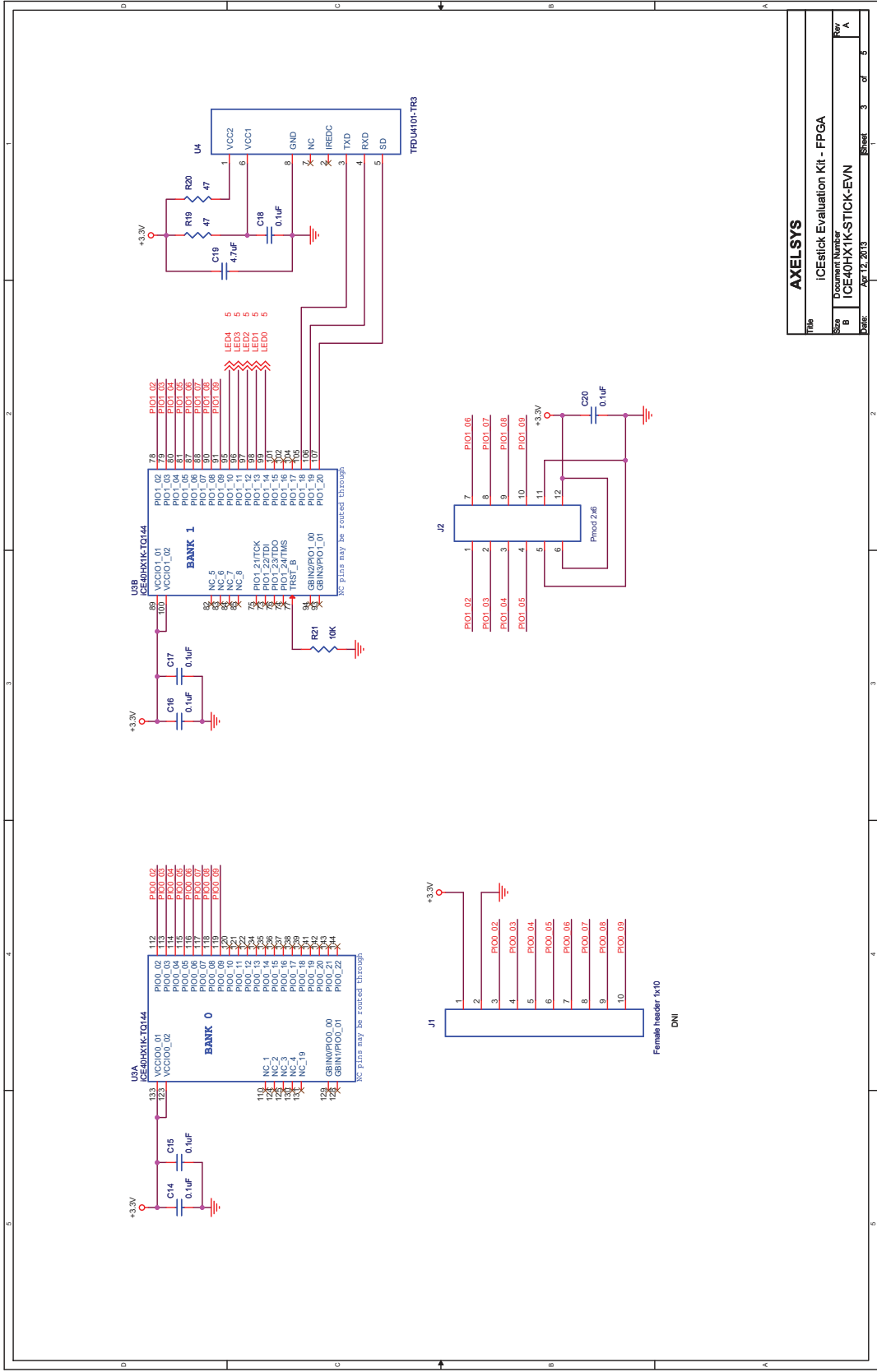
Revision History

Date	Version	Change Summary
August 2013	01.0	Initial release.

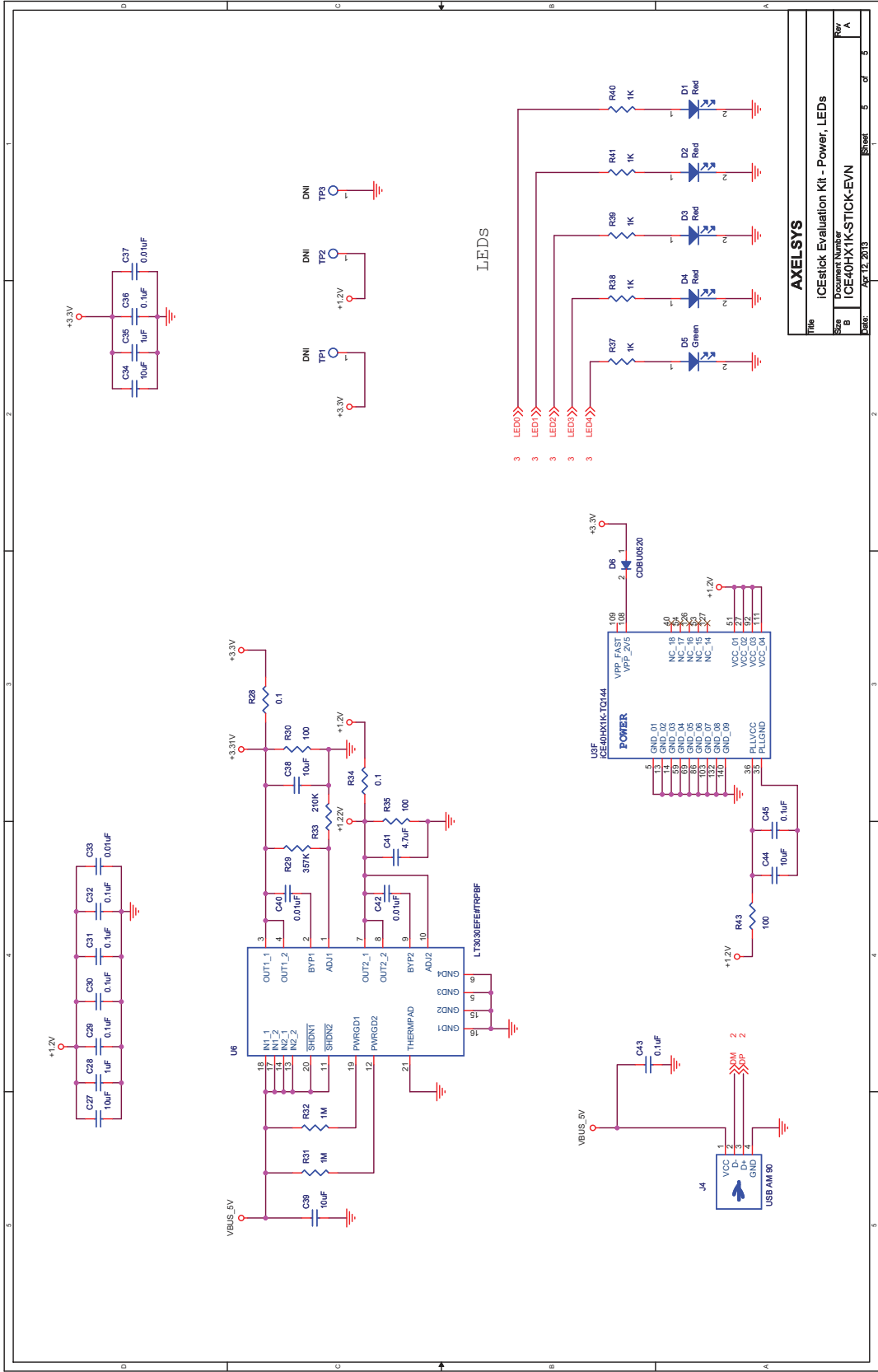
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Appendix A. Schematic Diagrams





AXELSYS			
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