CS8130

Multi-Standard Infrared Transceiver

Features

- Adds IR port to standard UART
- IrDA, HPSIR, ASK (CW) & TV remote compatible
- 1200bps to 115kbps data rate
- Programmable Tx LED power
- Programmable Rx threshold level
- Power down modes
- Direct, no modulation, mode
- Tiny 5x7mm 20 pin SSOP package
- +2.7V to +5.5V supply

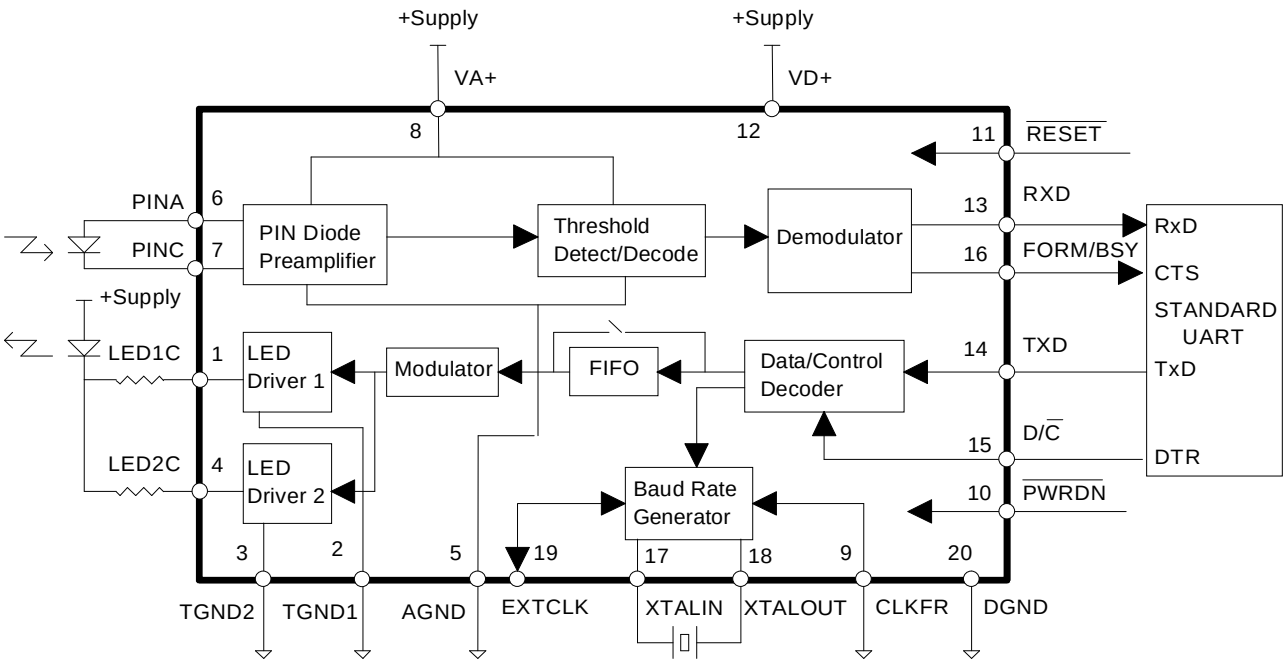
General Description

The CS8130 is an infrared transceiver integrated circuit. The receive channel includes on-chip high gain PIN diode amplifier, IrDA, HPSIR, ASK & TV remote compatible decoder, and data pulse stretcher. The transmit path includes IrDA, HPSIR, ASK & TV remote compatible encoder, and LED driver. The computer data port is standard UART TxD and RxD compatible, and operates from 1200 to 115200 baud.

External PIN diode and transmit LED are required. A control mode is provided to allow easy UART programming of different modes.

The CS8130 operates from power supplies of +2.7V to +5.5V.

Ordering Information:
See page 28.



TRANSMITTER DRIVER CHARACTERISTICS (T_A = 25 °C; All V+ = 3.0V, Digital Input Levels: Logic 0 = 0V, Logic 1 = V+; unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Units
Output capacitance (Note 1)			10	TBD	pF
Output rise time (10% to 90%)	tr	-	20	50	ns
Output fall time (90% to 10%)	tf	-	20	50	ns
Overshoot over final current		-	-	25	%
On resistance		-	-	0.5	Ω
Off leakage current		-	-	20	µA
Output current (each driver) (Note 2)		-	-	250	mA
Output jitter relative a jitter free input clock		-	-	200	ns

Notes: 1. Typical LED junction capacitance is 20pF.
2. 50% duty cycle, max pulse width 165 µs (3/16 of (1/1200 bps + 5%)).

RECEIVER CHARACTERISTICS (T_A = 25 °C; All V+ = 3.0V, Digital Input Levels: Logic 0 = 0V, Logic 1 = V+; unless otherwise specified)

Parameter		Symbol	Min	Typ	Max	Units
Input capacitance (Note 3)			-	10	TBD	pF
Input noise current			-	-	11	pA/rtHz
Maximum signal input current from detector			-	-	2	mA
Maximum DC input current (typically sunlight)			-	-	200	µA
Input current detection thresholds	RS4-0=00000:		-	7.8	-	nA
(Programmable with a 5 bit value)	RS4-0=00001:		-	15.6	-	nA
(Min, Max = Typical ±30%)	RS4-0=00010:		16.4	23.4	30.4	nA
(Note 4)	↓		↓	↓	↓	"
	RS4-0=11110:		169.5	242.2	314.9	nA
	RS4-0=11111:		175	250	325	nA
Bandpass filter response	High Pass -3dB:		-	35	-	kHz
	Low Pass -3dB:		-	700	-	kHz
Receiver power up time	With high (200µA) dc ambient		-	5	10	ms
	With normal (2µA) dc ambient		-	0.3	1	ms
Turn-around time, with receiver on continuously (Note 5)			-	5	10	ms
EMI rejection of system (0.5MHz to 100MHz). (Note 6)			3	-	-	V/m

Notes: 3. Typical PIN diode junction capacitance is 50pF.
4. The ±30% tolerance covers chip-to-chip variation. The temperature coefficient of the receiver threshold setting is low. Current detection thresholds are above the DC ambient condition. Settings of RS4-0 of less than 00010 are not practical because of noise.
5. Turn-around time is the time taken for the PIN diode receiver to recover from the IR energy from the transmitter. The remote end of the link must wait for this time after receiving data before transmitting a reply. This time may be reduced to <1 ms by good IR shielding from the transmit LED to the PIN diode.
6. This is a system specification. A metal shield over the PIN diode and CS8130 is recommended to ensure system compliance.

Specifications are subject to change without notice.

POWER SUPPLY SPECIFICATIONS (TA = 25°C; V+ = 3.0V, Digital Input Levels: Logic 0 = 0V, Logic 1 = V+, Note 7)

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage		2.7	3.0	5.5	V
Power Supply Current - All functions enabled (Note 8)		-	-	2.5	mA
Power Supply Current - All functions disabled (Note 9)		-	-	1	µA
Power Supply Current - Receiver only enabled (Note 8)		-	-	2.5	mA
Power Supply Current - Transmit only enabled (Note 10)		-	-	0.5	mA
Oscillator Power Supply Current low power mode: normal power mode:		- -	- -	0.5 1.5	mA mA
Data & State Retention Supply Voltage		2	-	-	V

Notes:
7. Power supply current specifications are with the supply at 3.0V. For approximate consumption at +5.0V, multiply the above currents by 1.667.
8. Oscillator in low power mode, does not include LED current. Subtract oscillator current if using an external clock to run the CS8130.
9. Floating digital inputs will not cause the power supply to increase beyond the specification.
10. Does not include LED current, does include oscillator current in low power mode.

RECOMMENDED OPERATING CONDITIONS (All voltages with respect to 0V)

Parameter	Symbol	Min	Typ	Max	Units
Operating Ambient Temperature	T_A	0	25	70	°C
Data and State Retention Temperature (In Power Down)		-40	-	85	°C

DIGITAL PIN CHARACTERISTICS (TA = 25°C, Supply = 3.0V)

Parameter	Symbol	Min	Typ	Max	Units
High-level Input Voltage	V_{IH}	2.0	-	-	V
Low-level Input Voltage	V_{IL}	-	-	0.8	V
High-level Output Voltage at I_O = -2.0mA	V_{OH}	VD-0.3	-	-	V
Low-level Output Voltage at I_O = 2.0mA	V_{OL}	-	-	0.3	V
Output Leakage Current in Hi-Z state				0.2	µA
Input Leakage Current (Digital Inputs)		-	-	0.2	µA
Output Capacitance	C_{OUT}	-	5	-	pF
Input Capacitance	C_{IN}	-	5	-	pF

ABSOLUTE MAXIMUM RATINGS (All voltages with respect to 0V)

Parameter	Symbol	Min	Max	Units
Power Supplies		-0.3	6.0	V
Input Current Except Supply Pins & Driver Pins		-	±10	mA
Input Voltage		-0.3	VD+0.3	V
Ambient temperature (Power Applied)		-55	+125	°C
Storage Temperature		-65	+150	°C
ESD using human body model (100pF with series 1.5kΩ)		2000	-	V

Warning: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS (T_A = 25 °C; All V+ = 3.0V, Digital Input Levels: Logic 0 = 0V, Logic 1 = V+; unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Units
XTALIN frequencies CLKFR pin low:		-	3.6864	-	MHz
(Note 11) CLKFR pin high:		-	1.8432	-	MHz
XTALIN duty cycle		45	50	55	%
Crystal Oscillator start up time		-	-	25	ms

Notes: 11. In normal oscillator mode, the crystal is internally loaded with 20 pF, which is the standard loading at which the crystal frequency is tuned. In low power oscillator mode, the internal loading on the crystal is reduced to approximately 5pF. The crystal frequency will therefore increase by about 0.03% in low power mode.

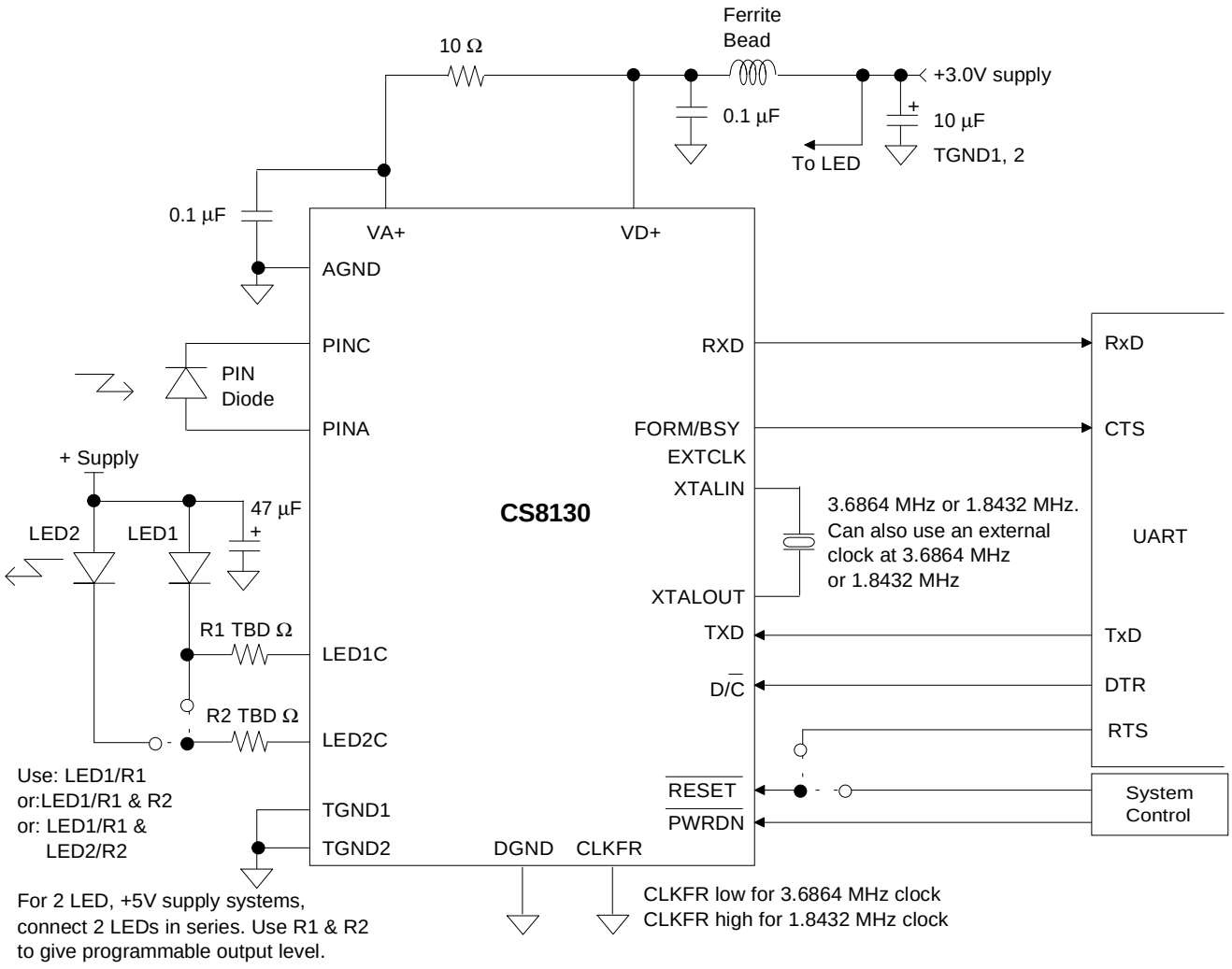


Figure 1. Recommended Connection Diagram

OVERVIEW

The CS8130 is an infrared transceiver I.C. The receive channel includes on-chip high gain PIN diode amplifier, IrDA, HP-SIR, 500 kHz Amplitude Shift Keying (ASK) & TV remote compatible decoder, and data pulse stretcher. The transmit path includes IrDA, HPSIR, 500 kHz ASK & TV remote compatible encoder, and LED drivers. The computer data port is standard UART TxD and RxD compatible, and operates from 1200 to 115200 baud. An on-chip baud rate generator is provided.

External PIN diode and transmit LED(s) are required. A control mode is provided to allow easy UART programming of different modes.

The CS8130 operates from power supplies of +2.7 V to +5.5 V. The device is supplied in a 20-pin SSOP package

FUNCTIONAL DESCRIPTION

The following pages describe the detailed operation of the CS8130.

IR Data Formats

The CS8130 supports three infrared data transmission formats: IrDA/HPSIR, 500kHz ASK and 38kHz ASK (TV Remote). There is also a direct access mode, which bypasses the CS8130 encoder and decoders, and gives direct access to the IR raw data. This mode is for situations where the encoding and/or decoding is done externally.

Modes may be set independently for transmit and receive, although this would be unusual.

Mode 1 IrDA/HP-SIR

The CS8130 is designed to allow easy realization of an IrDA compatible IR port (see IrDA Serial Infrared (SIR) Physical Layer Link Specification, Version 1.0, April 27 1994). Figure 2 shows the format of Mode 1. A pulse of IR energy indicates a logic ’0’. No IR indicates a logic ’1’. The pulse can be from 3/16 of a bit cell time at 115200 (~1.6 µs), to 3/16 of a bit cell time at 2400 bps (~78 µs). The width of the pulse may be fixed at 1.6µs for all baud rates, or may scale with the baud rate. The initial baud rate for IrDA is 9600 bps, with a negotiated baud rate possibility of 2400 to 115200 bps.

Mode 2 500 kHz ASK

Figure 3 shows the infrared data format for Mode 2. This is a Carrier Wave (CW) type system, where the presence of a 500kHz carrier is treated as a ’0’, and absence of a carrier is treated as a ’1’. Normally used baud rates are 9600 bps, 19.2 kbps and 38.4 kbps.

Mode 3 38 kHz ASK (TV remote mode)

Figure 4 shows the infrared data format for Mode 3, the TV remote control mode. This is similar to Mode 2, except that the modulation frequency is ~38kHz. The IR bit rate is approximately 2400 bps. Both modulation frequency and bit rate vary significantly for different manufacturer and model remote controls.

Mode 4 Direct Access Mode

In Mode 4, the IR transmission tracks directly what is present on the TXD pin. A logic ’1’ means that the LED is off, a logic ’0’ means that the LED is on. Care must be taken to ensure that the LED is not ’on’ continuously, otherwise the LED may be damaged.

In Mode 4, received IR is compared against the programmed threshold. The resulting logic output is routed directly to the RXD pin. A logic ’1’ means no IR is detected, a logic ’0’ means IR is being detected. If a IR carrier is being received,

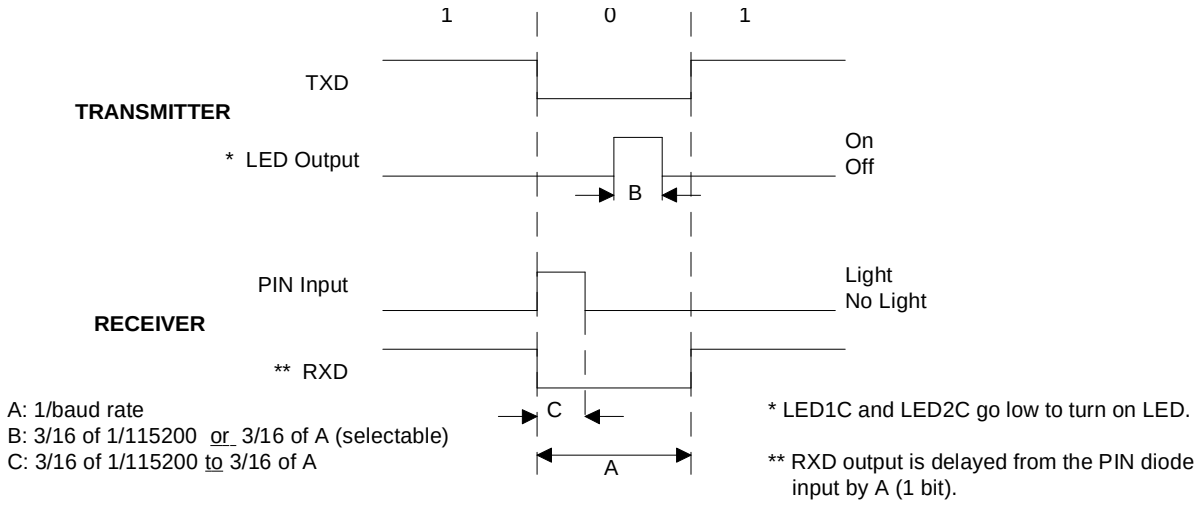


Figure 2. Infra Red Data Format Mode 1 (IRDA/HPSIR)

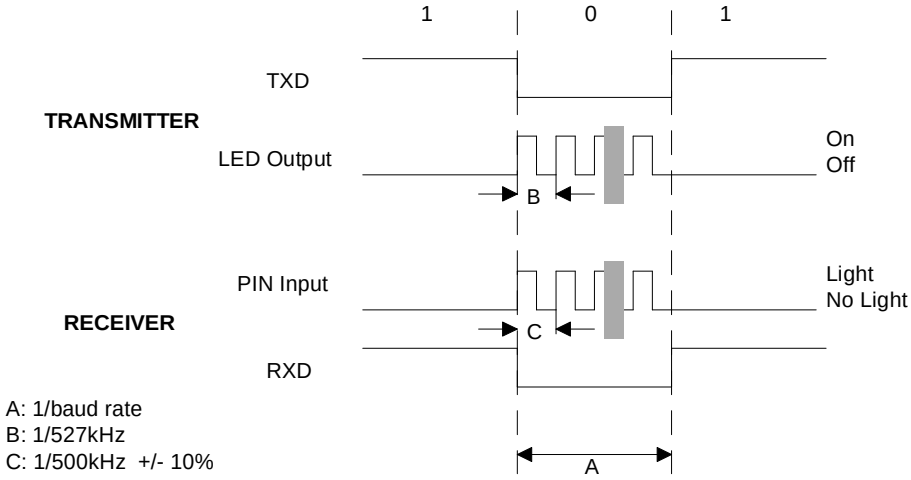


Figure 3. Infra Red Data Format Mode 2 (500kHz ASK)

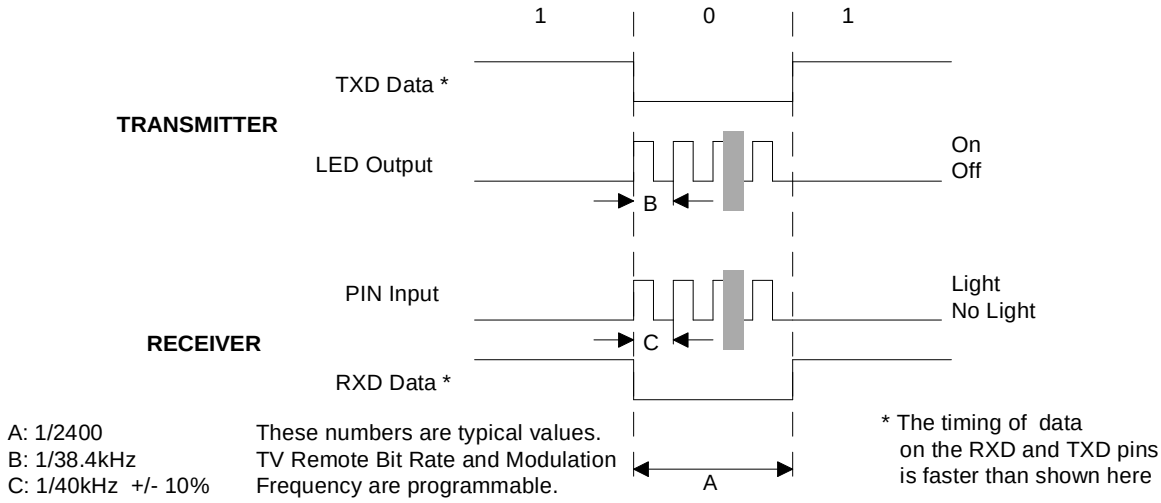


Figure 4. Infra Red Data Format 3 (TV Remote, 38kHz ASK)

then the RXD pin will oscillate at the carrier frequency.

Transmit Path

Data for transmission is input to the CS8130 on the TXD pin. The selected modulation scheme is then applied to the data, and the resulting signals are used to drive the LED. There are 2 LED output pins: LED1C and LED2C. They are open drain outputs, which pull down to TGND or float. The LED is connected via resistors to both LED1C and LED2C. The current level flowing through the LED is determined by the external resistors. Normally, LED1C is used to drive the LED. If additional current is needed, (for example for TV remote operation), then the second driver may be enabled. The amount of 'boost' current is determined by the external resistor connected to the LED2C pin.

For larger amounts of IR output, it may be preferable to use two LEDs, rather than drive a large current through one LED. For a +3V supply system using two LEDs, each one is connected, via a resistor, to each driver output. For a +5V supply system, 2 LEDS may be connected in series, and then routed to each driver via 2 resistors, one for each driver. This minimizes the power dissipation in the resistors.

Mode 1 Transmit Choices

In Mode 1 (IrDA), the pulse width may be fixed at 1.6 µs, or set to 3/16 of the bit period. Either of these settings will meet the IrDA standard, but fixed 1.6 µs pulses will save power at lower baud rates.

In addition, there is a choice which affects the output pulse jitter. The default state causes the CS8130 to look for the start bit on TXD. All subsequent LED transitions for that character are timed relative to the internal baud rate clock. Therefore there will be no jitter in the LED output pulse timing. However, the CS8130 now has to be programmed with the desired number of bits per character, which for IrDA compliance, is 8.

Alternatively, the CS8130 can generate output pulses based entirely on individual transitions on TXD, with no knowledge of which bit is the start bit. Thus a 1 to 0 transition will generate a pulse based on that transition edge. If TXD is low for multiple successive bits, then the CS8130 will generate pulses based on its internal clock. Therefore there is the possibility of jitter in the output pulses of N*271 ns. N can be 0, 1 2....., depending on the difference in frequency between the UART baud rate clock and the CS8130 clock. Clearly, if the CS8130 and its associated UART are running from the same clock, the possibility of jitter is eliminated.

Mode 2 (ASK) Transmit Choices

The modulation frequency is determined by the modulator divider registers. For nominal 500 kHz, use a divide value of 6, which yields a modulation frequency of 527 kHz.

Mode 3 (TV Remote) Transmit Choices

During transmission of IR, the start and stop bits present in the incoming data from the UART are stripped off (see Figure 5). The remaining data bits are then sent out at ~2400 bps. Since there should be no gaps in the transmitted data, the input data is buffered in a 22-character location FIFO. Characters can be received on the TXD pin while the previous characters are being transmitted. To prevent overflow, a hardware handshake mechanism is provided. If the FIFO is one character away from being full, the FORM/BSY pin is brought high, indicating that the UART should not send any more data. Once another character has been transmitted, FORM/BSY pin is brought low, indicating to the UART that it is OK to send another character.

The modulation frequency is determined by the modulator divider registers. The transmit bit rate is determined by the TV Remote transmit bit rate divider. The UART to CS8130 baud rate must be set to at least 20% faster than the transmit bit rate.

Receive Path

A PIN diode is attached to the PINA and PINC pins. Compensation for the DC ambient light is applied to the photocurrent from the diode. The change in photocurrent from ambient is amplified and compared to a threshold value. If the photocurrent is greater than the set threshold, the output is set to 'light'. If the photocurrent is less than the set threshold, the output is set to 'no light'. The threshold current is programmable. This allows users to make the tradeoff between noise immunity and the reliable transmission distance of the link. The PIN diode amplifier has a bandpass filter characteristic, to limit the effects of IR interference. The resulting logic signal is further qualified, depending on the IR format selected.

An autodetect feature is provided. If autodetect mode is enabled, and transmit TV remote mode is disabled, the FORM/BSY output pin indicates the format of incoming data. If high, then the incoming data is in IrDA/HPSIR format. If low, the data is in ASK format which matches the programmed modulation frequency.

Mode 1 (IrDA) Receive Choices

For Mode 1a, a logic circuit is set to only look for pulse widths of 1.6µs. For Mode 1b, a logic circuit looks for pulses of 3/16 of the set baud rate bit period. For Mode 1c, a logic circuit looks for pulse widths of ≥1.6 µs, but ≤3/16 of the set baud rate bit period.

Mode 2 (ASK) Receive Choices

For Mode 2, a logic circuit looks for sequences of 'light' and 'no light' which matches the expected 500kHz carrier. The modulator divider registers must be set to 6. The ASK receive timing sensitivity register should be set to 0, yielding a valid incoming frequency range of 461 kHz to 614 kHz.

The RXD data transitions will lag behind the infrared activity by 3 modulation cycles. This allows the modulation detect circuit time to verify the correct modulation frequency.

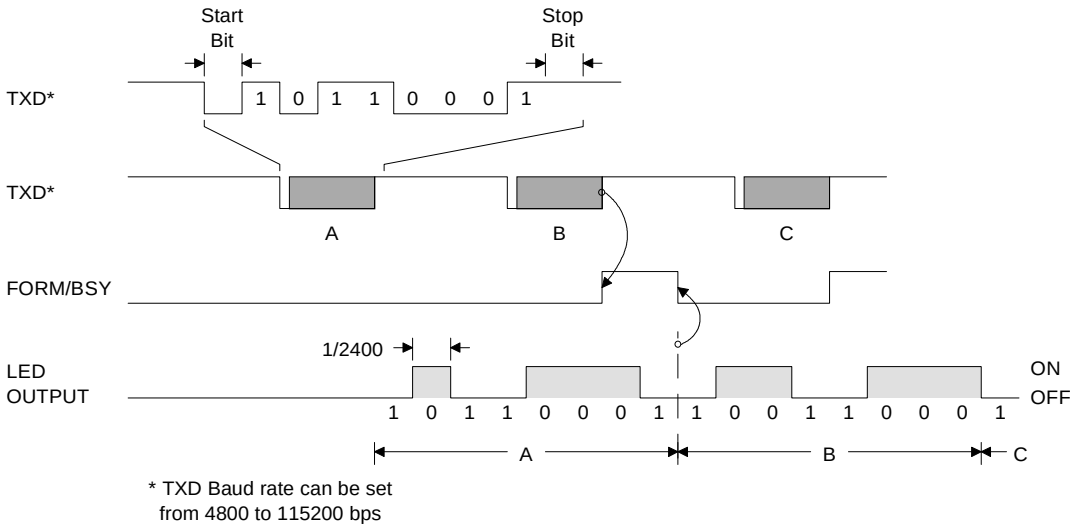


Figure 5. Mode 3 (TV Remote) Transmit Data Format

Mode 3 (TV remote) Receive Choices

The modulation frequency must be set into the modulator divider registers. The tolerance on the expected frequency must be programmed into the Receive ASK Timing Sensitivity (RATS) register. The RATS register sets the time window that the demodulator will accept for the period of valid data. Since the RATS register specifies time windows which are negative (e.g. 1000b (8) = +0.27 µs to -4.61 µs), then the modulation frequency must be set to lower than the desired nominal setting. For example, with RATS set to 1000 (8), and the desired nominal frequency being 38 kHz, then set the modulation divider registers to 35.10 kHz. With these settings, the demodulator will accept any frequency from 34.78 kHz to 41.88 kHz as valid. Smaller RATS register settings will result in tighter tolerance on the accepted receive modulation frequency. Changes in the RATS register settings must be accompanied by changes in the modulation frequency register to keep the nominal desired frequency in the center of the valid frequency band.

There are two TV remote receive data modes: "oversampled" mode and "programmed T period" mode. For "oversampled" mode, first choose the UART to CS8130 baud rate, typically 115.2 kbps. Then set the TV remote receive timing register to a rate which is less than 80% of the UART baud rate. The CS8130 will now start sampling the demodulated infrared data at the TV remote receive sample rate. The stream of samples will be assembled into characters, with a start bit and a stop bit, and will be transmitted to the UART via RXD at the UART baud rate. The system software can then concatenate successive characters and reconstruct the incoming bit stream.

"Programmed T period" mode requires that the bit period of the bursts of modulated carrier be known. This period is programmed into the TV remote receive timing registers. The UART to CS8130 baud rate must be set to at least 20% greater than 1/T. The CS8130 will now use the edges of the demodulated incoming infrared data to indicate each bit state. For continuous periods of low or high, the CS8130 will sample the level in the center of each incoming bit period (using T as the bit period). Any transition will reset the timer that is used for the sampling process, thereby eliminating errors caused by the sample timing being different to the incoming bit period. Characters are assembled and sent to the UART every 8 bits (see Figure 6).

If the T period is not known, it is possible to measure T by using "oversampled" mode, and

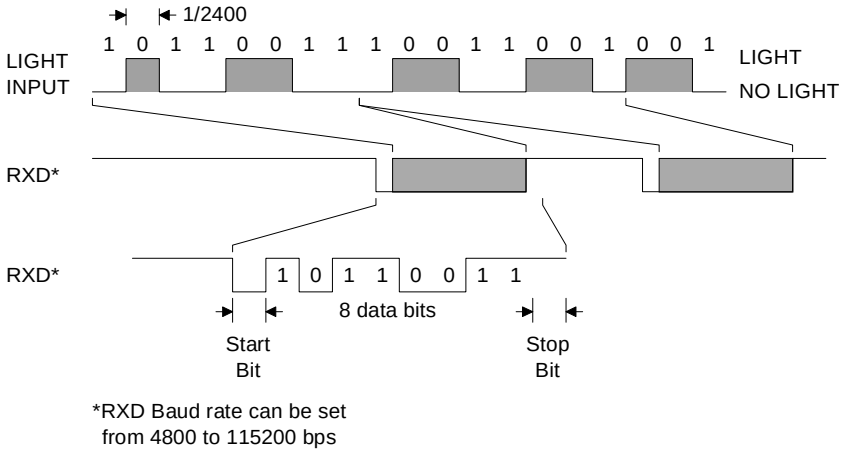


Figure 6. Mode 3 (TV remote) Receive Data Format

then switch to "programmed T period" mode to reduce processing overhead in the host CPU.

Clock Generation

The primary clock required is 3.6864 MHz. This may be generated by attaching a 3.6864 MHz crystal to the XTALIN and XTALOUT pins. In this case, the EXTCLK pin becomes an output, and may be used to drive external devices. If this is not required, power may be saved by disabling the EXTCLK output. The CLKFR pin should be connected to DGND, which causes the clock circuits to be configured for 3.6864 MHz operation.

The oscillator has a low power mode. This reduces the internal crystal loading capacitance on XTALOUT and XTALIN. The selection of this mode is via a bit in Control Register #4. Since the loading capacitance is reduced, then the crystal frequency will increase by approximately 0.03%.

Alternatively, a 3.6864 MHz clock may be input into the EXTCLK pin, in which case XTALIN must be grounded, and XTALOUT is left floating. The CLKFR pin must be connected to DGND.

If only a 1.8432 MHz clock is available, then it may be input into the EXTCLK pin and the CLKFR pin connected to VD+. This causes the CS8130 to double the incoming 1.8432 MHz clock to 3.6864 MHz for internal use. XTALIN must be grounded, and the XTALOUT pin is left floating.

The CS8130 automatically sets the direction of the EXTCLK pin. If the crystal oscillator is running when $\overline{\text{RESET}}$ goes high, then EXTCLK becomes an output. Since the crystal oscillator can take up to 25 ms to start, then it follows that $\overline{\text{RESET}}$ must be held low, with $\overline{\text{PWRDN}}$ high and power applied, for at least 25 ms. If using an external clock, then $\overline{\text{RESET}}$ low can be short (>1 µs).

Power Down

When the $\overline{\text{PWRDN}}$ pin is brought low, all internal logic is stopped, including the crystal oscillator. The power consumption in power down mode is very low (<1 µA). When the $\overline{\text{PWRDN}}$ pin is brought high, the crystal oscillator will start. If using the crystal oscillator, allow 25 ms for oscillator start up after bringing $\overline{\text{PWRDN}}$ high, before trying to use the CS8130. The control register status will not be changed by toggling $\overline{\text{PWRDN}}$.

Control Register #1 allows for individual disabling and enabling of the transmit and receive sections of the CS8130.

The CS8130 also goes into power down if both transmit enable and receive enable bits are false, and the D/$\overline{\text{C}}$ pin is brought high. This allows control of power down in a pod environment, where access to the $\overline{\text{PWRDN}}$ pin is difficult. In this mode, it is possible to select, via a control register bit, whether the crystal oscillator remains running, or is powered off. If the oscillator remains running, then it consumes power, but offers instant wake up. If the oscillator is powered off, then it consumes no power, but will take 25 ms to start up.

The $\overline{\text{PWRDN}}$ pin must always be 'high' or 'low'. If this pin is allowed to float, excessive power consumption may occur. All other digital inputs may be allowed to float without causing excessive power consumption in the CS8130 in power down mode.

The RXD and FORM/BSY output pins may be programmed to be high, low or float in power down. This allows maximum flexibility in different applications.

Reset

Bringing the $\overline{\text{RESET}}$ pin low will force the internal logic, including the control registers, into a known state, provided the $\overline{\text{PWRDN}}$ pin is high. $\overline{\text{RESET}}$ is disabled if the $\overline{\text{PWRDN}}$ pin is low. The reset state is given in each register definition table. $\overline{\text{RESET}}$ must be low for >25 ms if using the crystal oscillator (see Clock Generation above).

Control Register Definitions

The various control registers within the CS8130 may be written by setting the D/$\overline{\text{C}}$ pin to low, and sending characters from the UART to the TXD pin. The characters are interpreted as a 4-bit address field and a 4-bit data field, as shown in Figure 7. After the control character is received and written into the control register, it is optionally echoed back out the RXD pin. The baud rate used for this control mode is whatever is currently set in the baud rate register. If the "load baud rate" bit is written to, then the new baud rate takes effect after the character has been echoed back, if echo is enabled. Otherwise, the new baud rate is effective immediately.

One of the control registers contains a shadow register set enable bit, which effectively becomes the MSB of the 5-bit register address. Hence there are 31 4-bit registers. The shadow bit must be written to a 1 to allow access to the registers with addresses 16 through 31. The shadow bit register is always accessible, independent of the state of the shadow bit. The shadow bit must be written to 0 to enable access to registers 0 through 15.

The following tables define the detailed function of all the registers inside the CS8130.

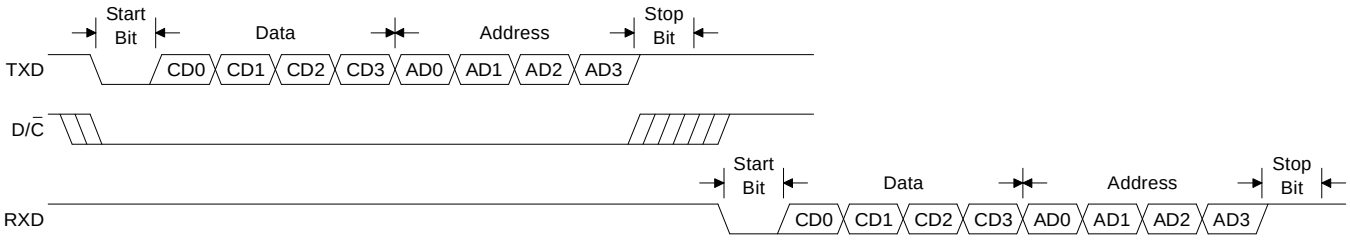


Figure 7. Control Mode Timing

Control Data Byte Format

D7	D6	D5	D4	D3	D2	D1	D0
AD3	**AD2**	**AD1**	**AD0**	**CD3**	**CD2**	**CD1**	**CD0**

BIT	NAME	VALUE		FUNCTION
AD3-0	Register Address (4 bits of transmitted address + MSB, which is the shadow (SHDW) bit state [Control Reg #3]. All registers have 4 data bits).	0_0000	0	Control register #1
		0_0001	1	Control register #2
		0_0010	2	Transmit Mode Register #1
		0_0011	3	Transmit Mode Register #2
		0_0100	4	Output Power register
		0_0101	5	Receive Mode register
		0_0110	6	Receive Sensitivity register #1
		0_0111	7	Receive Sensitivity register #2
		0_1000	8	Baud Rate Divider register #1
		0_1001	9	Baud Rate Divider register #2
		0_1010	10	Modulator Divider register #1
		0_1011	11	Modulator Divider register #2
		0_1100	12	Digital Output Pin Control register
		0_1101	13	Control Register #3
		0_1110	14	Reserved
		0_1111	15	Status register (read only)
		1_0000	16	TV Remote Receive Sample Rate & T Period Divider
		1_0001	17	TV Remote Receive Sample Rate & T Period Divider
		1_0010	18	TV Remote Receive Sample Rate & T Period Divider
		1_0011	19	TV Remote Transmit Bit Rate Divider #1
		1_0100	20	TV Remote Transmit Bit Rate Divider #2
		1_0101	21	Control Register #4
		1_0110	22	Reserved
		1_0111	23	Reserved
		1_1000	24	ASK Receive Timing Sensitivity register
		1_1001	25	Reserved
		1_1010	26	Reserved
		1_1011	27	Reserved
		1_1100	28	CS8130 Revision Level register (Read Only)
		1_1101	29	Reserved
		1_1110	30	Reserved (Resets to 1111; must not be changed)
		1_1111	31	Reserved (Resets to 1111; must not be changed)
CD3-0	Control Data			Contains control register data.

It is essential that all reserved registers and bits are not changed from their reset state. If reserved bits are changed, then internal test modes may be invoked, which may change some input pins to output pins, and may completely change the definition of some functions and signals. Reserved bits in registers, and reserved registers, may not return a known state when read, and should be ignored. Registers 28 and 15 are read only. Other non-reserved registers are write only. The CS8130 can be set to echo back register write commands to verify correct reception of the control settings.

Register 0, Control Register #1

	D3	D2	D1	D0
Register	**ECHO**	**0**	**RXEN**	**TXEN**
Reset (R)	0	0	0	0

BIT	NAME	VALUE		FUNCTION
ECHO	Echo Control Characters	0 1	R	Do not echo control characters Echo control characters.
RXEN	Receiver Enable	0 1	R	Receiver disabled Receiver enabled
TXEN	Transmitter Enable	0 1	R	Transmitter disbabled Transmitter enabled

Register 1, Control Register #2

	D3	D2	D1	D0
Register	**0**	**0**	**AUTD**	**LODB**
Reset (R)	0	0	0	0

BIT	NAME	VALUE		FUNCTION
AUTD	Receiver auto detect mode enable	0 1	R	Auto detect receive format disabled Auto detect receive format enabled
LODB	Load Baud Rate Counter	0 1	R	Do not load new baud rate count value Load new baud rate count value

The LODB bit resets to 0 automatically.

Register 2, Transmit Mode Register #1

	D3	D2	D1	D0
Register	**DIR**	**TVR**	**PWID**	**MODU**
Reset (R)	0	0	0	0

BIT	NAME	VALUE		FUNCTION
DIR	Direct Mode Enable	0 1	R	Mode 4 Direct access mode disabled Mode 4 Direct access mode enabled
TVR	TV Remote Mode Enable	0 1	R	Mode 3 TV remote mode disabled Mode 3 TV remote mode enabled
PWID	Select Pulse Width	0 1	R	Set pulse width to 1.6 µS Set pulse width to 3/16 of the bit period
MODU	Select Modulation Method	0 1	R	Mode 1 IrDA pulse modulation enabled Mode 2 Amplitude modulated carrier modulation

Register 3, Transmit Mode Register #2

	D3	D2	D1	D0
Register	**0**	**CHSY**	**BC1**	**BC0**
Reset (R)	0	1	1	0

BIT	NAME	VALUE			FUNCTION
CHSY	Character/bit synchronized	0 1		R	Bits are transmitted based on TXD bit transitions Bits are transmitted timed from the start bit
BC1-0	Number of bits per character (only needed if CHSY = 1)	00 01 10 11	0 1 2 3	R	6 data bits per character 7 data bits per character 8 data bits per character 9 data bits (8 data, 1 parity) per character

Register 4, Output Power Register

	D3	D2	D1	D0
Register	**0**	**0**	**OP1**	**OP0**
Reset (R)	0	0	0	0

BIT	NAME	VALUE			FUNCTION
OP1-0	Output Power Level	00 01 10 11	0 1 2 3	R	No LED output enabled LED1C output only enabled LED2C output only enabled Both LED1C and LED2C outputs enabled

Register 5, Receive Mode Register

	D3	D2	D1	D0
Register	**RTVR**	**RMOD**	**RWIDS**	**RWIDL**
Reset (R)	0	0	1	1

BIT	NAME	VALUE			FUNCTION
RTVR, RMOD, RWIDS, RWIDL	Receive Mode	0000	0		Mode 2 Amplitude modulated carrier mode
		0001	1		Mode 1a IRDA - fixed 1.6µs pulse
		0010	2		Mode 1b IRDA - variable 3/16 bit cell time pulse
		0011	3	R	Mode 1c IRDA - Any width pulse from 1.6µs to 3/16 bit cell time
		0100	4		Mode 4 Direct access mode
		1000	8		Mode 3 TV remote mode, oversampling receive
		1100	12		Mode 3 TV remote mode, timed bit cell receive
					All other combinations are reserved

Register 6, Receive Sensitivity Register #1

	D3	D2	D1	D0
Register	**RS3**	**RS2**	**RS1**	**RS0**
Reset (R)	0	1	1	1

Register 7, Receive Sensitivity Register #2

	D3	D2	D1	D0
Register	**0**	**0**	**0**	**RS4**
Reset (R)	0	0	0	0

BIT	NAME	VALUE			FUNCTION
RS4-0	Receive threshold setting.	00000	0		7.8 nA nominal receive threshold
		00001	1		15.6 nA nominal receive threshold
		"	"		"
		00111	7	R	62.5 nA nominal receive threshold
		"	"		"
		11110	30		242.2 nA nominal receive threshold
		11111	31		250 nA nominal receive threshold

Threshold settings of less than 20nA should not be used because background noise will cause the apparent occurrence of constant signal.

Register 8, Baud Rate Divider Register #1

	D3	D2	D1	D0
Register	**BR3**	**BR2**	**BR1**	**BR0**
Reset (R)	0	1	1	1

Register 9, Baud Rate Divider Register #2

	D3	D2	D1	D0
Register	**BR7**	**BR6**	**BR5**	**BR4**
Reset (R)	0	0	0	1

BIT	NAME	VALUE			FUNCTION
BR7-0	Baud Rate Divider Value (BRD). BRD=(3.6864E6/ (16*BR))-1, where BRD = divider value and BR = desired baud rate.	01011111 00101111 00010111 00001011 00001001 00000010 00000001	95 47 23 11 5 2 1	 R 	2400 bps 4800 bps 9600 bps 19.2 kbps 38.4 kbps 76.8 kbps 115.2 kbps

Register 10, Modulator Divider Register #1

	D3	D2	D1	D0
Register	**MD3**	**MD2**	**MD1**	**MD0**
Reset (R)	0	1	1	0

Register 11, Modulator Divider Register #2

	D3	D2	D1	D0
Register	**MD7**	**MD6**	**MD5**	**MD4**
Reset (R)	0	0	0	0

BIT	NAME	VALUE			FUNCTION
MD7-0	Modulator Divider Value (MD). MD=(3.6864E6/FR)-1, where MD = divider value and FR = desired modulation frequency.	01100000 00000110	96 6	 R	38 kHz 527kHz

The transmitted modulation frequency will be exact. The receive carrier detection frequency can be slightly different from the programmed frequency (see Receive ASK Carrier Timing Register).

Register 12, Output Pin Control Register

	D3	D2	D1	D0
Register	**RXDT**	**RXDH**	**FORT**	**FORH**
Reset (R)	0	1	0	1

BIT	NAME	VALUE		FUNCTION
RXDT	RXD output pin three-state enable	0 1	R	In power down, RXD will go high or low. In power down, RXD will float.
RXDH	RXD output pin high/low enable	0 1	 R	In power down, RXD will go low, if RXDT = 0 In power down, RXD will go high, if RXDT = 0
FORT	FORM/BSY output pin three-state enable	0 1	R	In power down, FORM/BSY will go high or low. In power down, FORM/BSY will float.
FORH	FORM/BSY output pin high/low enable	0 1	 R	In power down, FORM/BSY will go low, if FORT = 0 In power down, FORM/BSY will go high, if FORT = 0

Register 13, Control Register #3

	D3	D2	D1	D0
Register	**0**	**0**	**0**	**SHDW**
Reset (R)	0	0	0	0

BIT	NAME	VALUE		FUNCTION
SHDW	Shadow register set enable	0 1	R	Enable access to registers 0 though 15 Enable access to shadow registers (16 through 31)

Register 15, Status Register

	D3	D2	D1	D0
Register	**0**	**OSCR**	**ERR**	**DMOD**
Reset (R)	0		0	0

BIT	NAME	VALUE		FUNCTION
OSCR	Oscillator running flag	0 1		Oscillator not running, using external clock input, oscillator circuit is powered down. Oscillator running, EXTCLK is an output, if enabled.
ERR	Framing error flag	0 1	R	No error A framing error has occurred since the last read of this bit. Resets after read
DMOD	Detected Modulation Type	0 1	R	IrDA pulse style data format detected Amplitude modulated carrier style data format detected

To read this register, write 0000 to address 15. Independent of the setting of the ECHO bit, the CS8130 will transmit the above contents, with an address field of 1111.

Register 16, TV Remote Receive Timing Register #1

	D3	D2	D1	D0
Register	**TVR3**	**TVR2**	**TVR1**	**TVR0**
Reset (R)	1	1	1	1

Register 17, TV Remote Receive Timing Register #2

	D3	D2	D1	D0
Register	**TVR7**	**TVR6**	**TVR5**	**TVR4**
Reset (R)	1	1	1	1

Register 18, TV Remote Receive Timing Register #3

	D3	D2	D1	D0
Register	**TVR11**	**TVR10**	**TVR9**	**TVR8**
Reset (R)	0	1	1	1

BIT	NAME	VALUE	FUNCTION
TVR11-0	TV remote mode receiver timing register TVR = (3.6864E6 * T) -1 where T = the incoming bit period, and TVR = this register value.	000000000000 0 000000000001 1 ↓ ↓ 011111111111 2047R ↓ ↓ 111111111111 4095	T = 271 ns T = 542 ns ↓ T = 555 µs (1800 bps) ↓ T = 1.11 ms

For TV remote receive "oversampled" mode, this register value determines the input data sample rate. The sample rate is 3.6864 MHz divided by this register value. The sample rate should be set to as fast as possible, to give the best resolution on the incoming data edges, but should be less than 80% of the main UART communication baud rate.

For TV remote receive "programmed T period" mode, this register sets the expected incoming bit cell time (T). The main UART communications rate must be set to at least 20% greater than 1/T.

Register 19, TV Remote Transmit Bit Rate Divider Register #1

	D3	D2	D1	D0
Register	**TBR3**	**TBR2**	**TBR1**	**TBR0**
Reset (R)	1	1	1	1

Register 20, TV Remote Transmit Bit Rate Divider Register #2

	D3	D2	D1	D0
Register	**TBR7**	**TBR6**	**TBR5**	**TBR4**
Reset (R)	0	1	1	1

BIT	NAME	VALUE	FUNCTION
TBR7-0	TV remote mode transmit bit rate register TBR= (3.6864E6/(16*RATE)) -1 where TBR is this register value & RATE is the desired transmit bit rate.	01111111 127 R	RATE = 1800 bps

Register 21, Control Register #4

	D3	D2	D1	D0
Register	**OSCE**	**OSCL**	**EXCK**	**SRES**
Reset (R)	0	0	0	0

BIT	NAME	VALUE	FUNCTION
OSCE	Disable crystal oscillator in D/$\overline{C}$ controlled power down state	0 R 1	In D/$\overline{C}$ controlled power down state, crystal oscillator stays running. In D/$\overline{C}$ controlled power down state, crystal oscillator stops.
OSCL	Set oscillator in low power mode	0 R 1	Oscillator in normal power, high accuracy, mode. Oscillator in low power, medium accuracy mode.
EXCK	Disable external clock output driver	0 R 1	If crystal is used, enable clock output driver If crystal is used, disable clock output driver (Hi-Z)
SRES	Software Reset	0 R 1	Normal operation Causes a software reset, which forces all registers into their reset state. If ECHO is true, then the echo will occur at the current baud rate, before the baud rate changes to the default value.

Register 24, Receive ASK Timing Sensitivity Register

	D3	D2	D1	D0
Register	**RAT3**	**RAT2**	**RAT1**	**RAT0**
Reset (R)	0	0	0	0

BIT	NAME	VALUE			FUNCTION
RAT3-0	Receiver ASK Timing Sensitivity. Timing window = +0.27 µs to -RAT(2/3.6864E06) - 0.27 µs	0000 0001 0010 ↓ 1111	0 1 2 ↓ 15	R	+0.27 µs to -0.27 µs window (500 kHz ASK mode) +0.27 µs to -0.54 - 0.27 µs window +0.27 µs to -1.08 - 0.27 µs window ↓ +0.27 µs to -8.14 - 0.27 µs window

The timing window is relative to the modulation divider register nominal setting.

Register 28, CS8130 Silicon Revision Register

	D3	D2	D1	D0
Register	**REV3**	**REV2**	**REV1**	**REV0**

BIT	NAME	VALUE	FUNCTION
REV3-0	CS8130 silicon revision level	0000	1st silicon, designed to meet DS134PP2 data sheet, dated June 1994

This register should be read by the CS8130 driver to allow CS8130 future enhancements to be recognized, and incorporated into future versions of the driver.

Grounding & Layout

Grounding and layout for the CS8130 are critical, because of the sensitive nature of the PIN diode amplifier. The CS8130 should be over its own dedicated ground plane. The PIN diode should be very close to the PINA and PINC pins. The PIN diode traces should be very short (< 5 mm), and should be surrounded by ground plane. There should be holes in the ground plane provided for mounting a metal shield over the CS8130 and the PIN diode for EMI shielding. The PIN diode and transmit LEDs should be positioned so as to line up the front optical surfaces of the packages. The optical surface of the PIN diode and transmit LED(s) should be positioned 1cm back from the daylight IR filter window inside the case of the equipment. This ensures that direct sunlight does not fall upon the top surface of the PIN diode.

An evaluation kit, CDB8130, is available from Crystal. This may be used as an example of the correct layout for the CS8130 and the optical components.

Optical Components

TEMIC (Tel: 408 970 5684) provides Telefunken infrared LEDs and PIN diodes which are compatible with the CS8130. Contact Crystal for details of additional qualified LED and PIN diode sources.

Example Application Schematics

Crystal has prepared some example schematics which demonstrate possible uses for the CS8130.

Figure 8 shows a computer or PDA motherboard example, where one UART is used to drive both a wired RS232 COM port and an IR port.

Figure 9 shows a pod schematic. This is an external unit which can be plugged into any existing COM port to create an IR port.

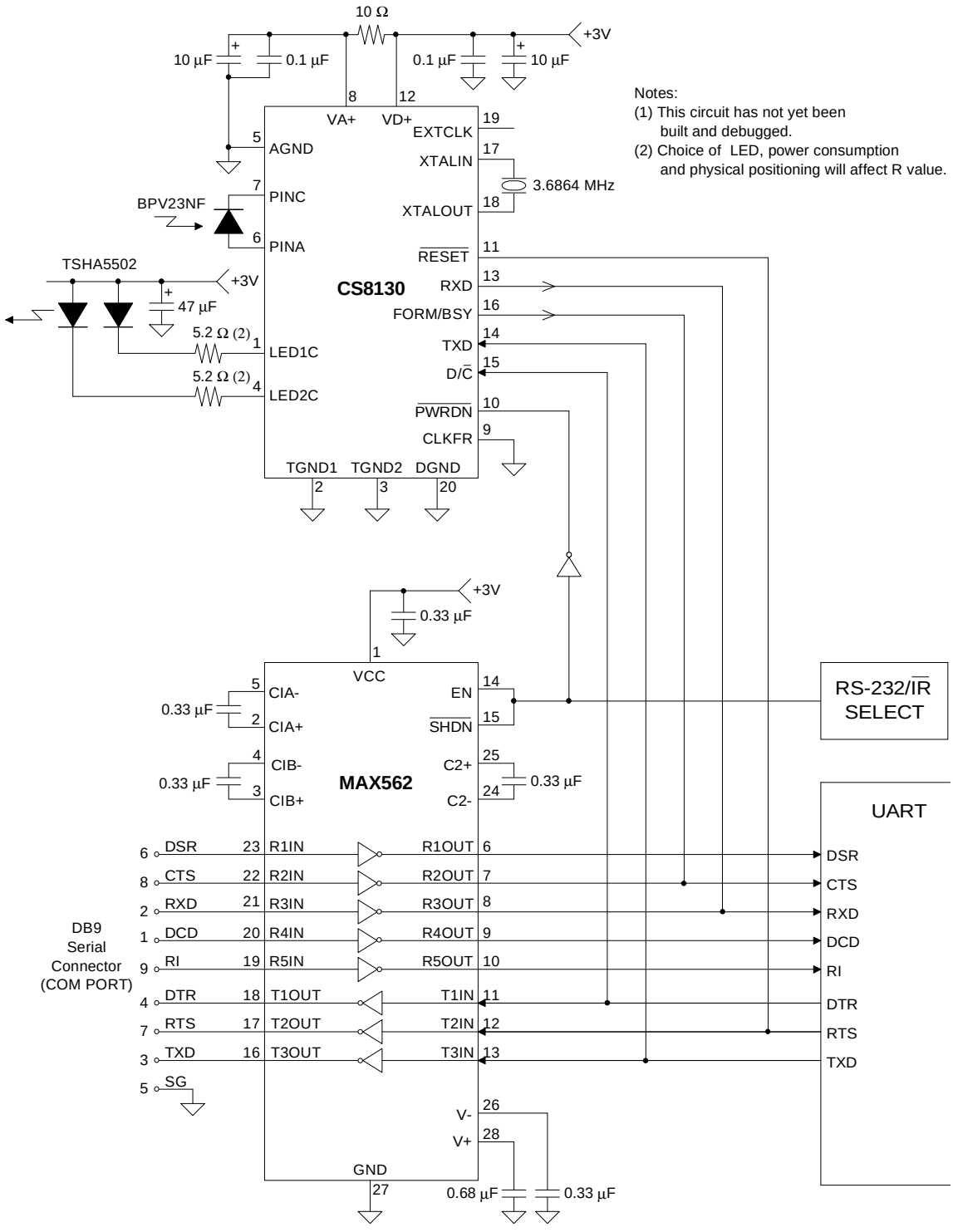
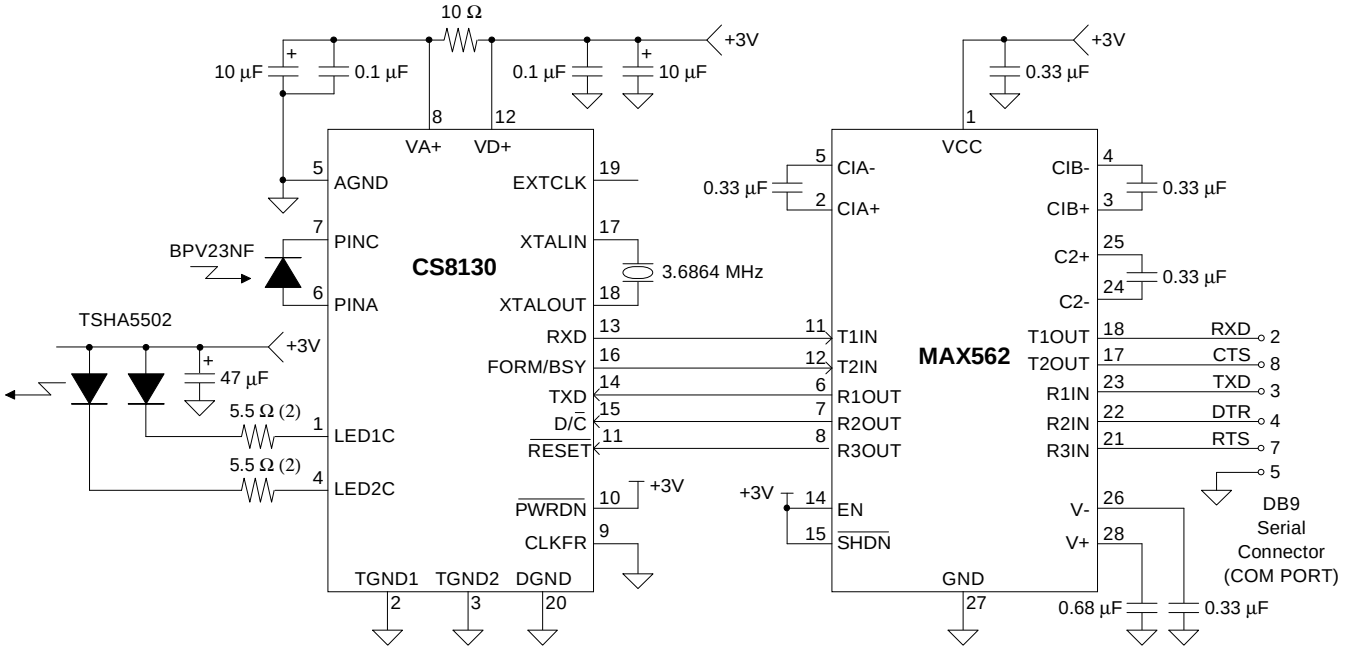


Figure 8. IR and RS232 from 1 UART

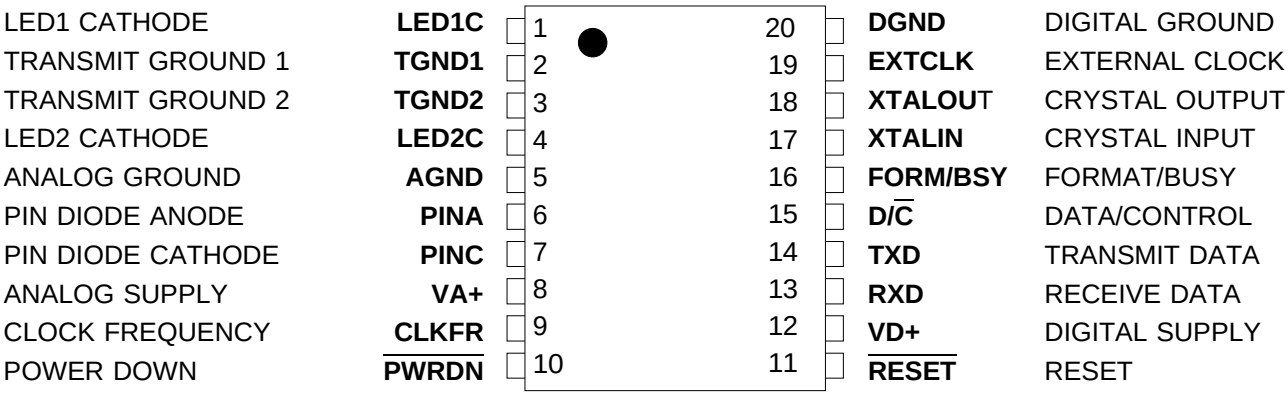


Notes:
(1) This circuit has not yet been built and debugged.
(2) Choice of LED, power consumption and physical positioning will affect R value.
(3) The creation of +3V or +5V supply is not included here.

RS232 COM PORT to Infra Red Interface Pod Schematic

Steven Harris
Crystal Semiconductor
5/26/94

Figure 9. Example Pod Schematic



Power Supplies

VD+ - Digital Positive Supply.
Digital positive supply voltage. Nominally +3V

VA+ - Analog Positive Supply.
Analog positive supply voltage. Nominally +3V.

DGND - Digital Ground.
Digital ground, 0V, connection.

AGND - Analog Ground.
Analog ground, 0V, connection.

TGND1, TGND2 - Transmitter Grounds.
LED Transmitter grounds, 0V, connections.

Analog Pins

LED1C, LED2C - Transmit LED Cathode.
These pins are connected to the transmit LED cathode via resistors. Appropriate resistor choice allows user setting of LED current options. The anode of the LED is connected to the positive supply.

PINC - Receiver PIN Diode Cathode
Receiver PIN diode cathode.

PINA - Receiver PIN Diode Anode.
Receiver PIN diode anode.

Digital Pins

RXD - Receiver Data Output

Receiver output data. Normally connected to RxD on the UART.

TXD - Transmit Data Input

Transmitter input data. Normally connected to TxD on the UART.

D/$\overline{C}$ - Data/Control Mode Input

The D/$\overline{C}$ pin determines whether the input data on TXD is treated as data to be transmitted via the LED, or as control information to set up the CS8130 internal registers. The D/$\overline{C}$ pin also can act as a power down control.

FORM/BSY - Received Data Format Output/Busy Signal Output

If auto format detect mode is enabled, this pin indicates the format of the incoming data. FORM is low for ASK format data, and high for IRDA/HPSIR format data.

In TV remote data mode (Mode 3), this pin becomes a handshake signal to the UART. FORM/BSY low means OK to send a character. FORM/BSY high means "I am busy, do not send another character".

$\overline{PWRDN}$ - Power Down Control Input

$\overline{PWRDN}$ low places the CS8130 into a very low power consumption "off" state.

$\overline{RESET}$ - Reset Input

$\overline{RESET}$ low places all the internal logic into a known state. All the control register bits are forced high or low, as defined in the register definition section. If the crystal oscillator is in use, then $\overline{RESET}$ must be held low for >25 ms, with $\overline{PWRDN}$ high and power applied. If an external clock is used, then the $\overline{RESET}$ pulse can be short (>1 µs).

XTALIN, XTALOUT - Crystal Connections

To use the internal oscillator, connect either a 3.6864 MHz or a 1.8432 MHz crystal between XTALOUT and XTALIN. If using an external clock, connect XTALIN to DGND.

EXTCLK - External Clock Input or Output

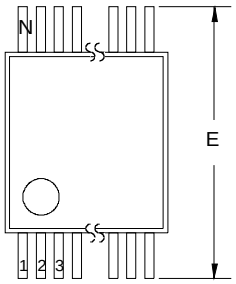
If no crystal is present on XTALIN and XTALOUT, EXTCLK becomes an input. A 3.6864 MHz or 1.8432 MHz clock should be connected to EXTCLK. XTALIN should be connected to DGND.

If a crystal is present on XTALIN and XTALOUT, EXTCLK becomes an output. EXTCLK will output the same frequency as the crystal. The EXTCLK output driver may be disabled to conserve power.

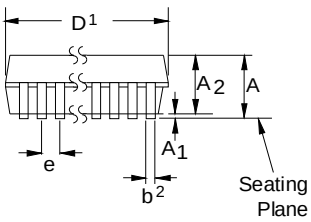
CLKFR - Clock Frequency Select Input

Tie CLKFR to ground to select a 3.6864 MHz clock. Connect CLKFR to the VD+ pin to select a 1.8432 MHz clock.

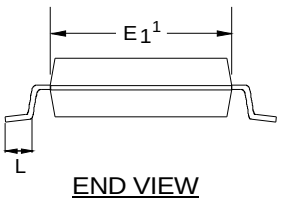
20 PIN SSOP



TOP VIEW



SIDE VIEW



END VIEW

SSOP Package Dimensions

Notes:

1. "D" and "E1" are reference datums and do not include mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20mm per side.
2. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13mm total in excess of b dimension at maximum material condition. Dambar intrusion shall not reduce dimension b by more than 0.07mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25mm from lead tips.

	MILLIMETERS			INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	Note
A	-	-	2.13	-	-	0.084	
A_1	0.05	0.15	0.25	0.002	0.006	0.010	
A_2	1.62	1.75	1.88	0.064	0.070	0.074	
b	0.22	0.30	0.38	0.009	0.012	0.015	2, 3
D	see other table			see other table			1
E	7.40	7.80	8.20	0.291	0.307	0.323	
E_1	5.00	5.30	5.60	0.197	0.209	0.220	1
e	0.61	0.65	0.69	0.024	0.026	0.027	
L	0.63	0.90	1.03	0.025	0.035	0.040	
N	see other table			see other table			
∝	0°	4°	8°	0°	4°	8°	

	D						
	MILLIMETERS			INCHES			
N	MIN	NOM	MAX	MIN	NOM	MAX	Note
20	6.90	7.20	7.50	0.272	0.283	0.295	1
28	9.90	10.20	10.50	0.390	0.402	0.413	1

ORDERING INFORMATION

Model	Package	Temperature
CS8130-CS	20-pin SSOIC	0 to +70 °C

ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS8130-CS	240 °C	2	365 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

REVISION HISTORY

Revision	Date	Changes
PP2	JUN 1994	Initial Release
F1	SEP 2005	Updated device ordering info. Updated legal notice. Added MSL data..

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to www.cirrus.com