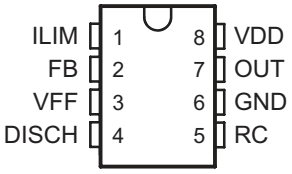
HIGH-SPEED VOLTAGE MODE PULSE WIDTH MODULATOR

Check for Samples: UCC25705-Q1, UCC25706-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Greater Than 4-MHz Operation**
- **Integrated Oscillator / Voltage Feed Forward Compensation**
- **>4:1 Input Voltage Range**
- **25-ns Current Limit Delay**
- **Programmable Maximum Duty Cycle Clamp**
- **Optocoupler Interface**
- **50-µA Start-Up Current**
- **4.2-mA Operating Current at 1 MHz**
- **Latch-Up Exceeds 100mA per JESD78 Class I**
- **Smallest Footprint of the 8-pin MSOP Package Minimizes Board Area and Height**

D PACKAGE
(TOP VIEW)



DESCRIPTION

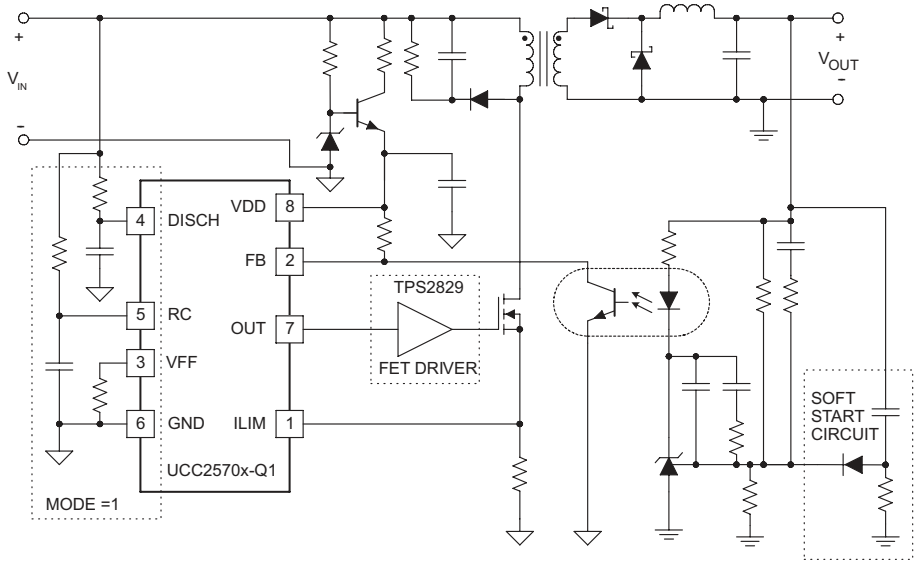
The UCC25705-Q1 and UCC25706-Q1 devices are 8-pin voltage mode primary side controllers with fast over-current protection. These devices are used as core high-speed building blocks in high performance isolated and non-isolated power converters.

UCC25705-Q1/UCC25706-Q1 devices feature a high speed oscillator with integrated feed-forward compensation for improved converter performance. A typical current sense to output delay time of 25 ns provides fast response to overload conditions. The IC also provides an accurate programmable maximum duty cycle clamp for increased protection which can also be disabled for the oscillator to run at maximum possible duty cycle.

Two UVLO options are offered. The UCC25705-Q1 with lower turn-on voltage is intended for dc-to-dc converters while the higher turn-on voltage and the wider UVLO range of the UCC25706-Q1 is better suited for offline applications.

The UCC2570x-Q1 family is offered in an 8-pin SOIC (D) package.

Figure 1. TYPICAL APPLICATION SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)(1)(2)

	VALUE	UNIT
Supply voltage	15	V
Input voltage (VFF,RC,ILIM)	7	V
Input voltage (FB)	15	V
Input current (DISCH)	1	mA
Output current (OUT) dc	±20	mA
Storage temperature, T_{stg}	–65 to 150	°C
Junction temperature, T_J	–55 to 150	°C
Lead temperature (soldering, 10 sec)	300	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult ti.com/packaging for more information.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
T_A	Operating ambient temperature	–40 to 105	°C

ORDERING INFORMATION TABLE

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–-40°C to 125°C	SOIC-8 – D	Reel of 2500	UCC25706QDRQ1	25706Q
–-40°C to 125°C	SOIC-8 – D	Reel of 2500	UCC25705QDRQ1	Preview

ESD RATINGS TABLE

PARAMETER		VALUE	UNIT
ESD	Human Body Model (HBM)	1000	V
	Charged- Device Model (CDM)	1000	V
	Machine Model (MM)	200	V

ELECTRICAL CHARACTERISTICS

V_{DD} = 11 V, V_{IN} = 30 V, R_T = 47 k, R_{DISCH} = 400 k, R_{FF} = 14 k, C_T = 220 pF, C_{VDD} = 0.1 µF, and no load on the outputs, T_A = –40° to 125°C, (unless otherwise specified)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
UVLO section (UCCx5705)						
Start threshold			8.0	8.8	9.6	V
Stop threshold			7.4	8.2	9.0	V
Hysteresis			0.3	0.6	1.0	V
UVLO section (UCCx5706)						
Start threshold			11.2	12.0	12.8	V
Stop threshold			7.2	8.0	8.8	V
Hysteresis			3.2	4.0	4.5	V
Supply Current Section						
Start-up current	V_{DD} = UVLO start – 1 V, V_{DD} comparator off			30	90	µA
I_{DD} active	V_{DD} comparator on, oscillator running at 1 MHz			4.2	5.0	mA
Line Sense Section						
Low line comparator threshold			0.95	1.00	1.15	V
Input bias current (VFF)			–100		100	nA
Oscillator Section						
Frequency	VFF = 1.2 V to 4.8 V		0.9	1.0	1.1	MHz
CT peak voltage	VFF = 1.2 V,	See (1)		1.2		V
	VFF = 4.8 V,	See (1)		4.8		V
CT valley voltage	See (1)			0		V
Current Limit Section						
Input bias current			0.2	–0.2	–1	µA
Current limit threshold			180	200	220	mV
Propagation delay, ILIM to OUT	50 mV overdrive			25	35	ns
Pulse Width Modulator Section						
FB input impedance	V_{FB} = 3 V		30	50	90	kΩ
Minimum duty cycle	V_{FB} < 2 V				0	%
Maximum duty cycle	V_{FB} = V_{DD},	F_{OSC} = 1 MHz	70	75	80	%
	V_{DISCH} = 0 V,	F_{OSC} = 1 MHz		93		%
PWM gain	V_{FF} = 2.5 V,	MODE = 1		12		%/V
Propagation delay, PWM to OUT				65	130	ns
Output Section						
V_{OH}	I_{OUT} = –5 mA,	V_{DD} – output		0.3	0.6	V
V_{OL}	I_{OUT} = 5 mA			0.15	0.4	V
Rise time	C_{LOAD} = 50 pF			10	25	ns
Fall time	C_{LOAD} = 50 pF			10	25	ns

(1) Specified by design.

PIN DESCRIPTIONS

DISCH: A resistor to VIN sets the oscillator discharge current programming a maximum duty cycle. When grounded, an internal comparator switches the oscillator to a quick discharge mode. A small 100-pF capacitor between DISCH and GND may reduce oscillator jitter without impacting feed-forward performance. I_{DISCH} must be between 25 µA and 250 µA over the entire V_{IN} range.

FB: Input to the PWM comparator. This pin is intended to interface with an optocoupler. Input impedance is 50-kΩ typical.

GND: Ground return pin.

I_{LIM}: Provides a pulse-by-pulse current limit by terminating the PWM pulse when the input is above 200 mV. This provides a high speed (25 ns typical) path to reset the PWM latch, allowing for a pulse-by-pulse current limit.

OUT: The output is intended to drive an external FET driver or other high impedance circuits, but is not intended to directly drive a power MOSFET. This improves the controller's noise immunity. The output resistance of the PWM controller, typically 60 Ω pull-up and 30 Ω pull-down, will result in excessive rise and fall times if a power MOSFET is directly driven at the speeds for which the UCC2570x-Q1 is optimized.

RC: The oscillator can be configured to provide a maximum duty cycle clamp. In this mode the on-time is set by RT and CT, while the off-time is set by R_{DISCH} and CT.Since the voltage ramp on CTis proportional to VIN, feed-forward action is obtained. Since the peak oscillator voltage is also proportional to VIN, constant frequency operation is maintained over the full power supply input range. When theDISCH pin is grounded, the duty cycle clamp is disabled. The RC pin then provides a low impedance path to ground CT during the off time.

V_{DD}: Power supply pin. This pin should be bypassed with a 0.1-µF capacitor for proper operation. The undervoltage lockout function of the UCC2570x-Q1 allows for a low current startupmode and ensures that all circuits become active in a known state. The UVLO thresholds on the UCC25705-Q1 are appropriate for a dc-to-dc converter application. The wider UVLO hysteresis of the UCC25706-Q1 (typically 4 V) is optimized for a bootstrap startup mode from a high impedance source.

V_{FF}: The feed-forward pin provides the controllerwith a voltage proportional to the power supply input voltage. When the oscillator is providing a duty cycle clamp, a current of 2 × I_{DISCH} is sourced from the V_{FF} pin. A single resistor R_{FF} between V_{FF} and GND then set V_{FF} to:

$$VFF \approx VIN \times \left(\frac{2 \times R_{FF}}{2 \times R_{FF} + R_{DISCH}} \right)$$

When the DISCH pin is grounded and the duty cycle clamp is not used, the internal current source is disabled and a resistor divider from VIN is used to set VFF. In either case, when the voltage on V_{FF} is less than 1.0 V, both the output and oscillator are disabled.

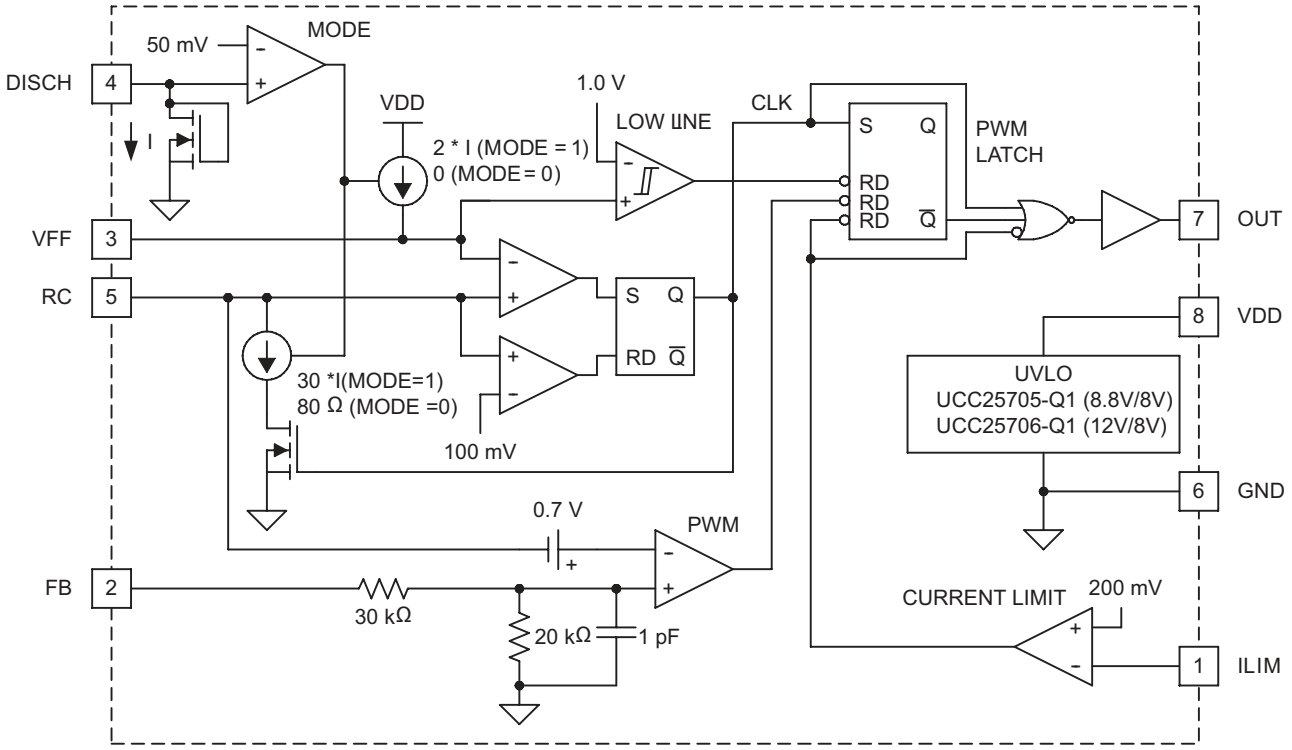


Figure 2. Block Diagram

FUNCTIONAL DESCRIPTION

Oscillator and PWM

The oscillator can be programmed to provide a duty cycle clamp or be configured to run at the maximum possible duty cycle.

The PWM latch is set during the oscillator discharge and is reset by the PWM comparator when the C_T waveform is greater than the feedback voltage. The voltage at the FB pin is attenuated before it is applied to the PWM comparator. The oscillator ramp is shifted by approximately 0.65-V at room temperature at the PWM comparator. The offset has a temperature coefficient of approximately -–2 mV/°C.

The I_{LIM} comparator adds a pulse by pulse current limit by resetting the PWM latch when V_{ILIM} > 200 mV. The PWM latch is also reset by a low line condition (V_{FF} <1.0 V).

All reset conditions are dominant; asserting any output will force a zero duty cycle output.

Oscillator With Duty Cycle Clamp (MODE = 1)

The timing capacitor C_T is charged from ground to V_{FF} through R_T. The discharge path is through an on-chip current sink that has a value of 30 × I_{DISCH}, where I_{DISCH} is the current through the external resistor R_{DISCH}. Since the charge and discharge currents are both proportional to V_{IN}, their ratio, and the maximum duty cycle remains constant as V_{IN} varies.

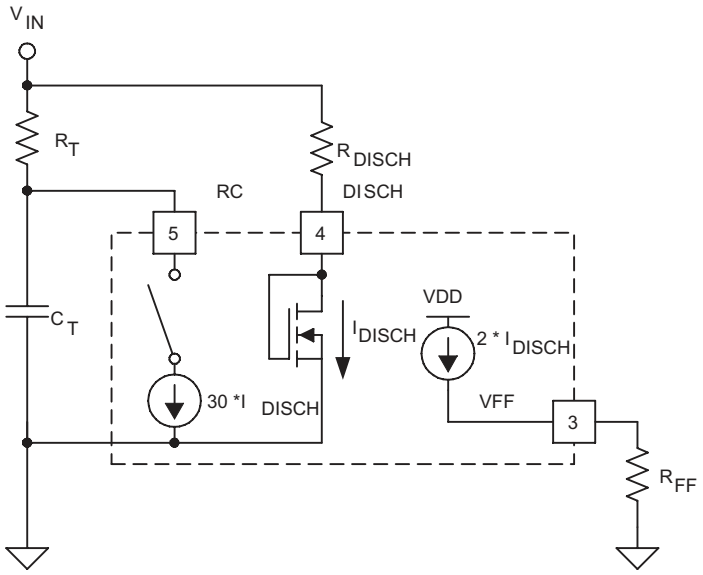


Figure 3. Duty Cycle Clamp (MODE = 1)

The on-time is approximately:

$$T_{ON} = \alpha \times R_T \times C_T \text{ where } \alpha = \frac{V_{FF}}{V_{IN}} \approx \frac{2 \times R_{FF}}{R_{DISCH}}$$

The off-time is:

$$T_{OFF} = \alpha \times \frac{C_T \times (R_T \times R_{DISCH})}{30 \times R_T - R_{DISCH}}$$

The frequency is:

$$f = \frac{1}{\alpha \times R_T \times C_T} \times \frac{1}{1 + \frac{R_{DISCH}}{30 \times R_T - R_{DISCH}}}$$

The maximum duty cycle is:

$$\text{Duty Cycle} = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \left(1 - \frac{R_{DISCH}}{30 \times R_T}\right)$$

Component Selection for Oscillator With Duty Cycle Clamp (MODE = 1)

For a power converter with the following specifications:

- $V_{IN(min)}$ = 18 V
- $V_{IN(max)}$ = 75 V
- $V_{IN(shutdown)}$ = 15 V
- F_{OSC} = 1 MHz
- MAX = 0.78 at $V_{IN(min)}$

In this mode, the on-time is approximately:

- $T_{ON(max)}$ = 780 ns
- $T_{OFF(min)}$ = 220 ns
- $V_{FF(min)} = \frac{18}{15} = 1.20\,V$

1. Pick C_T = 220 pF.
2. Calculate R_T.

$$R_T = \frac{V_{IN(min)} \times T_{ON(max)}}{V_{FF(min)} \times C_T}$$

R_T = 51.1 kΩ

3. R_{DISCH}

$$R_{DISCH} = \frac{30 \times R_T}{1 + \left(\frac{\left(\frac{V_{FF(min)}}{V_{IN(min)}} \right) \times R_T \times C_T}{T_{OFF(min)}} \right)}$$

R_{DISCH} = 383 kΩ.

I_{DISCH} must be between 25 µA and 250 µA over the entire VIN range.

With the calculated values, I_{DISCH} ranges from 44 µA to 193 µA, within the allowable range. If I_{DISCH} is too high, C_T must be decreased.

4. R_{FF}

$$R_{FF} = \frac{V_{FF(min)} \times R_{DISCH}}{2 \times (V_{IN(min)} - 1)}$$

The nearest 1% standard value to the calculated value is 13.7 k.

Oscillator Without Duty Cyle Clamp (MODE = 0)

In this mode, the timing capacitor is discharged through a low impedance directly to ground. The DISCH pin is externally grounded. A comparator connected to DISCH senses the ground connection and disables both the discharge current source and V_{FF} current source. A resistor divider is now required to set V_{FF}.

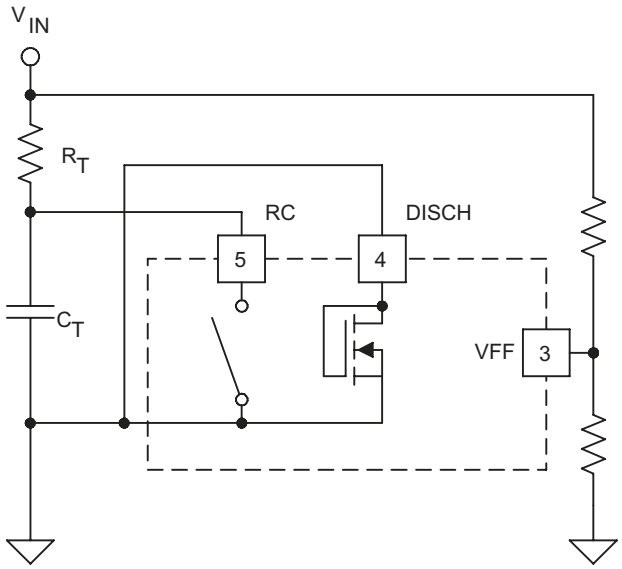


Figure 4. Ocsillator Without Clamp (MODE = 0)

In this mode, the on-time is approximately: $T_{ON} = \alpha \times R_T \times C_T$ where $\alpha = \frac{V_{FF}}{V_{IN}}$

The off-time is: $T_{OFF} \approx 75$ ns

The frequency is:

$$f = \frac{1}{\alpha \times R_T \times C_T + 75ns}$$

Component Selection for Oscillator Without Duty Cycle Clamp (MODE = 0)

For a power converter with the following specifications:

- $V_{IN(min)}$ = 18 V
- $V_{IN(max)}$ = 75 V
- $V_{IN(shutdown)}$ = 15 V
- F_{OSC} = 1 MHz

With these specifications,

$$V_{FF(min)} = \frac{18}{15} = 1.2V$$

1. Pick C_T = 220 pF
2. Calculate R_T.

$$R_T = \frac{\frac{V_{IN(min)}}{V_{FF(min)}} \times \left(\frac{1}{F_{OSC}} - 75ns \right)}{C_T}$$

TYPICAL CHARACTERISTICS

UCC25705-Q1 UVLO THRESHOLDS vs TEMPERATURE

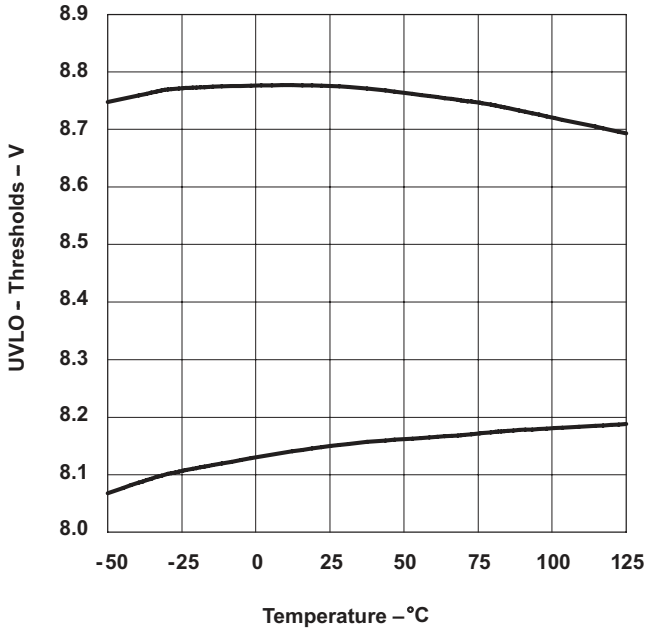


Figure 5.

UCC25706-Q1 UVLO THRESHOLDS vs TEMPERATURE

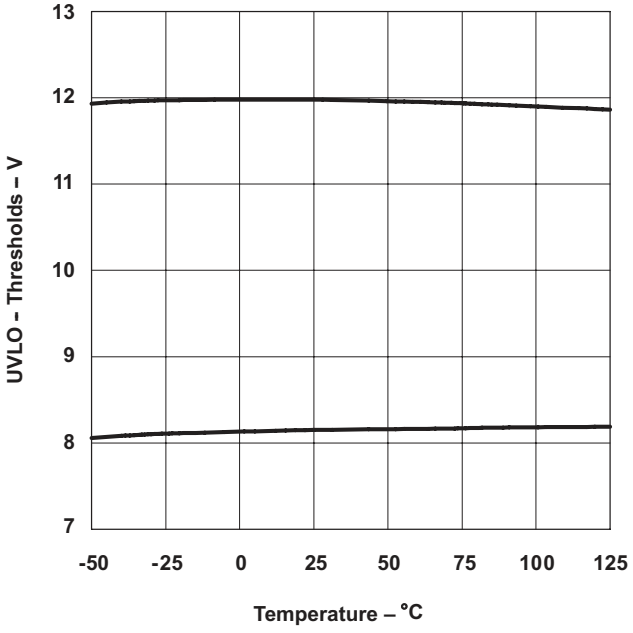


Figure 6.

OPERATING CURRENT (AT 1MHz) vs TEMPERATURE

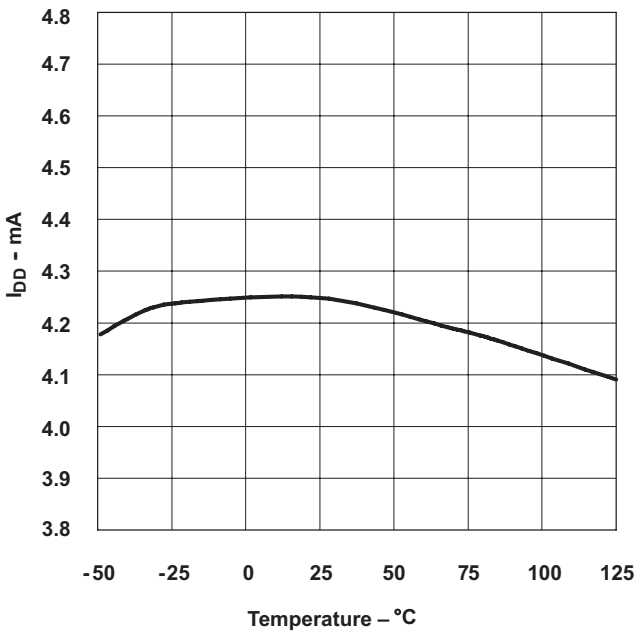


Figure 7.

LOW-LINE THRESHOLD vs TEMPERATURE

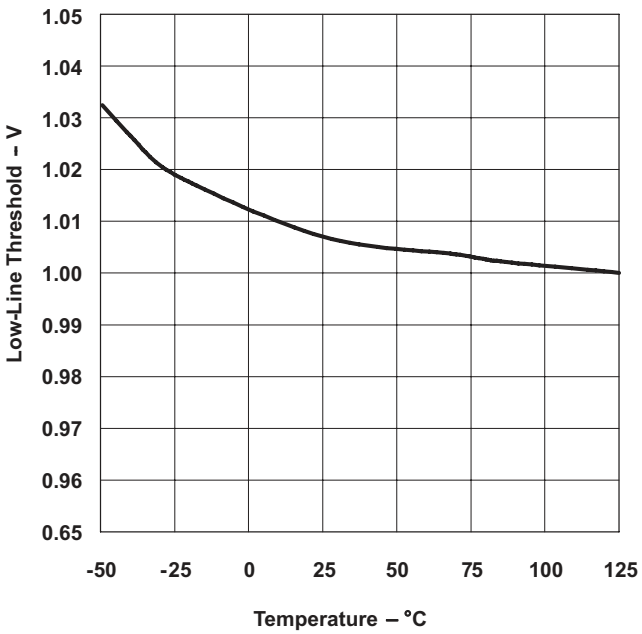


Figure 8.

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY vs TEMPERATURE

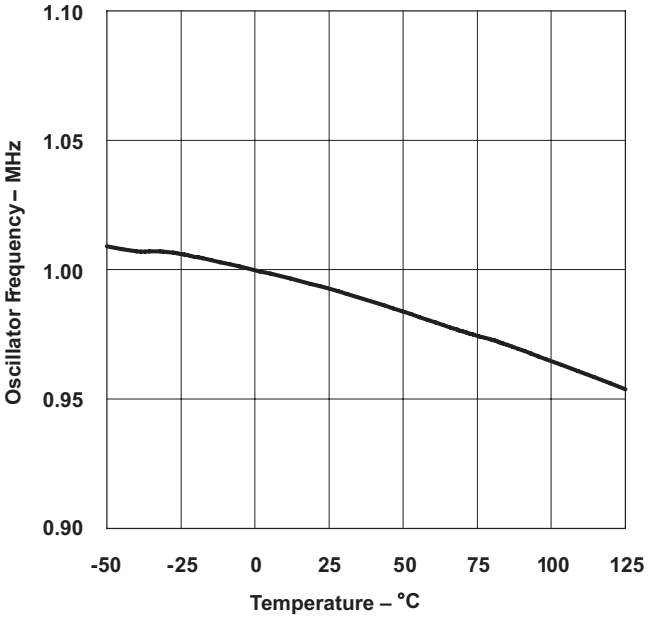


Figure 9.

PROGRAMMABLE MAXIMUM DUTY CYCLE vs TEMPERATURE

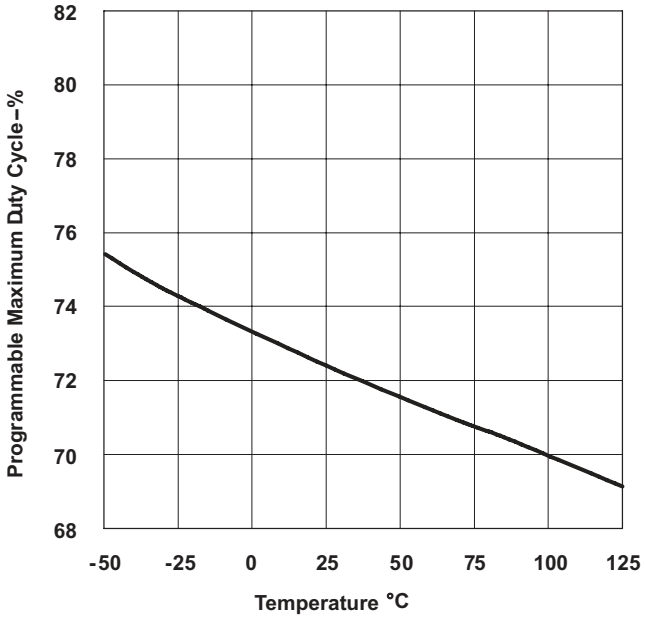


Figure 10.

CURRENT-LIMIT THRESHOLD vs TEMPERATURE

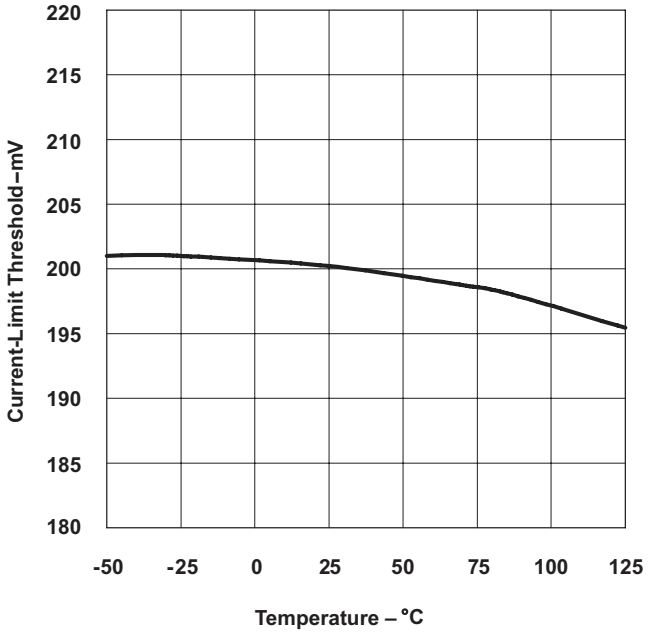


Figure 11.

CURRENT-LIMIT PROP DELAY vs TEMPERATURE

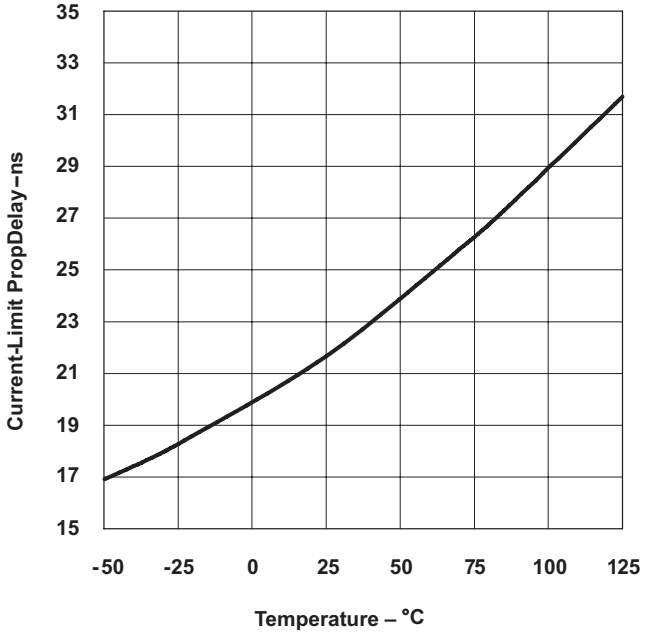


Figure 12.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC25706QDRQ1	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25706Q	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC25706-Q1 :

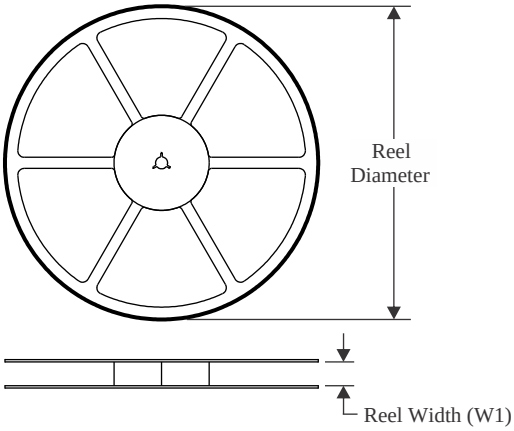
- Catalog : UCC25706

NOTE: Qualified Version Definitions:

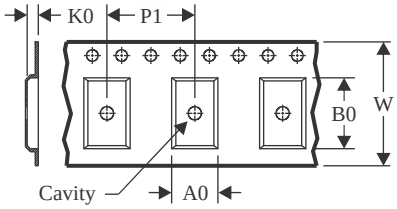
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

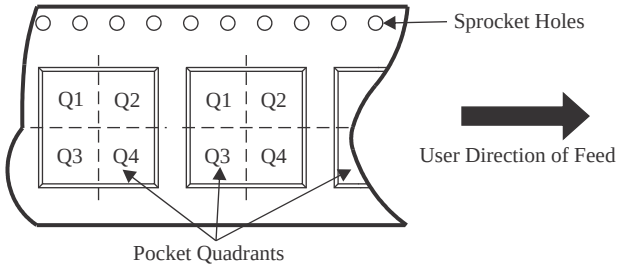


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

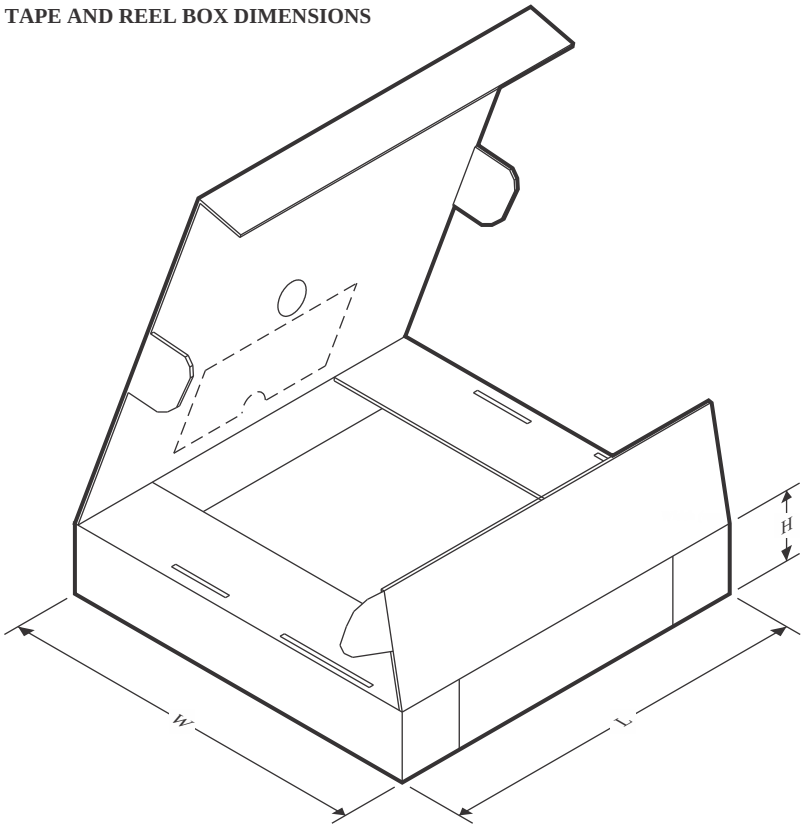
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

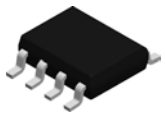
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC25706QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC25706QDRQ1	SOIC	D	8	2500	356.0	356.0	35.0

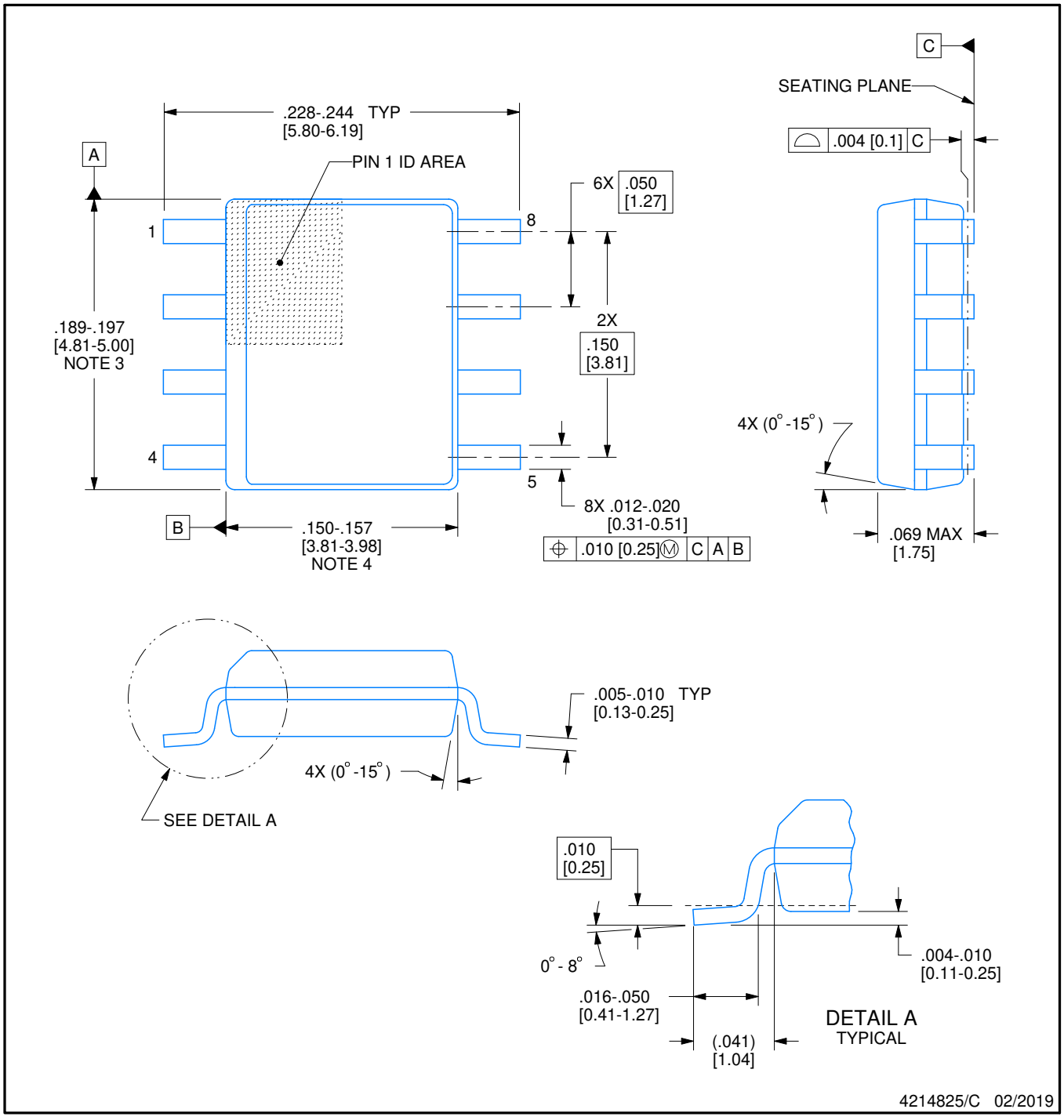


PACKAGE OUTLINE

D0008A

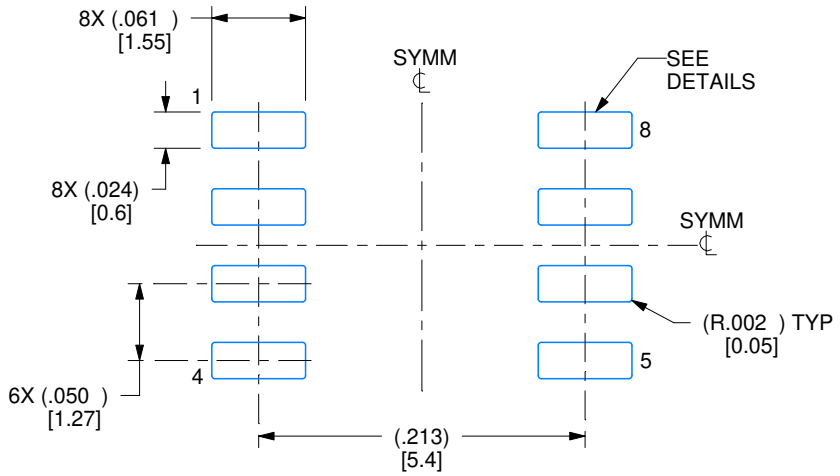
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

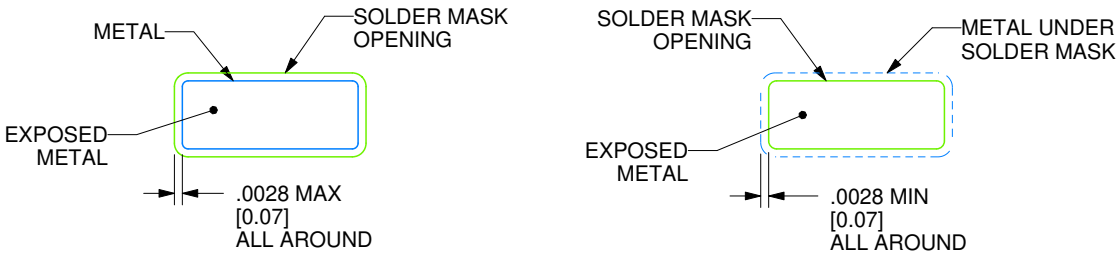


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

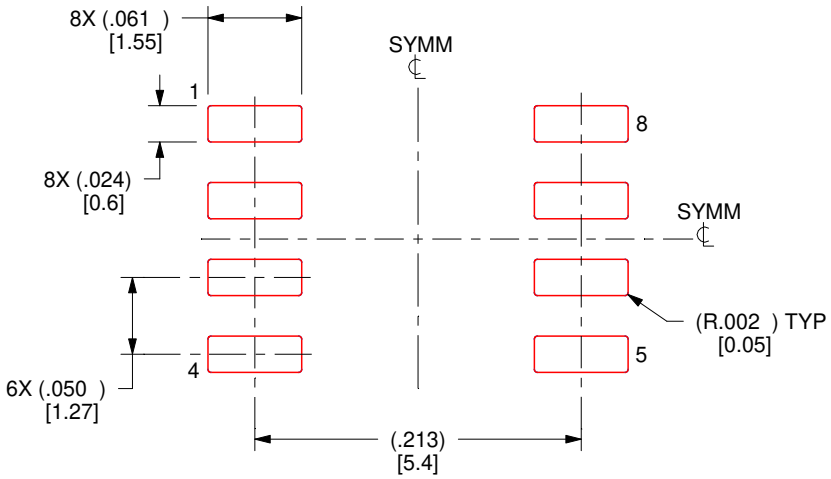
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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