XK372
3.2x2.5mm
LVCMOS Clock Oscillator

CONNOR WINFIELD

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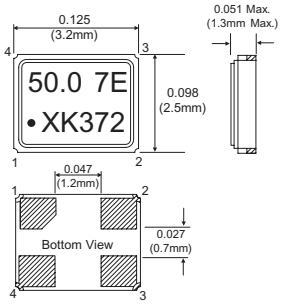
Description:

The Connor-Winfield XK372 3.2x2.5 mm, LCMOS, Surface Mount, Crystal Controlled Oscillators (XO) are designed for applications requiring low jitter and tight frequency stability. The RoHS compliant surface mount package is designed for high-density mounting and is optimum for mass production.

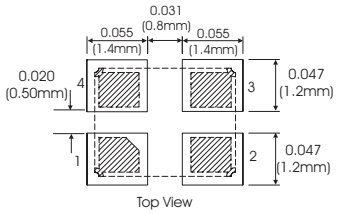
Features:

- Supply Voltage: 3.3V Operation
- Frequency Tolerance: ±50 ppm
- Temperature Range: -40 to 85°C
- LVCMOS Output Logic
- Tri-State Enable/Disable Pad 1
- Low Jitter < 0.1ps RMS
- Ceramic Surface Mount Package
- Tape and Reel Packaging
- RoHS Compliant / Lead Free ✓RoHS

Package Layout



Suggested Pad Layout



Dimensional Tolerance: ±0.005 (±0.127mm)

Pad Connections

1:	Output Enable (OE)
2:	Ground
3:	Output
4:	Supply Voltage (Vdd)

Ordering Information

XK3	7	2	-050.0M
Oscillator Type 3.2x2.5 mm LVCMOS Clock Oscillator Series	Supply Voltage and Temperature Range 7 = 3.3V, -40 to 85°C	Frequency Stability 2 = ±50 ppm	Output Frequency Frequency Format -xxx.xM Min.* -xxx.xxxxxxM Max* *Max 6 digits after decimal point M = MHz

Example Part Number: XK372-050.0M

Absolute Maximum Ratings

Parameter	Minimum	Nominal	Maximum	Units	Notes
Storage Temperature	-55	-	125	°C	
Supply Voltage (Vdd)	-0.5	-	5.0	Vdc	
Input Voltage -0.5	-		Vdd + 0.5	Vdc	

Input Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Enable Input Voltage - (Vih)	70%Vdd	-	-	Vdc	1
Disable Input Voltage - (Vil)	-	-	30%Vdd	Vdc	1
Standby Current (Osc. Disabled)	-	-	10	uA	

LVCMOS Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Load	-	15	-	pF	
Voltage High (Voh)	90%Vdd	-	-	Vdc	
Low (Vol)	-	-	10%Vdd	Vdc	
Duty Cycle at 50% Level	45	50	55	%	
Rise / Fall Time: 10% to 90%	-	5	8	ns	

RoHS COMPLIANT

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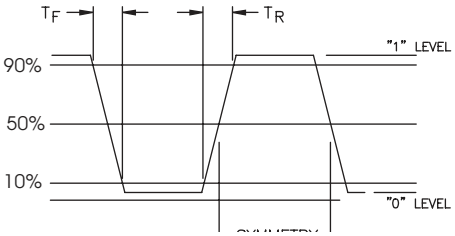
Operating Specifications

Parameter	Minimum	Nominal	Maximum	Units	Notes
Output Frequency (Fo)	20	-	50	MHz	
Total Frequency Tolerance:	-50		50	PPM	2
Operating Temperature Range:	-40		85	°C	
Supply Voltage (Vdd)	3.135		3.465	Vdc	
Supply Current (Idd)			10	mA	
Jitter:					
Period Jitter	-	3	5	ps RMS	
Integrated Phase Jitter	-	60	100	fs RMS	3
SSB Phase Noise Fo = 50 MHz					
@ 10 Hz offset	-	-70	-	dBc/Hz	
@ 100 Hz offset	-	-105	-	dBc/Hz	
@ 1 KHz offset	-	-140	-	dBc/Hz	
@ 10 KHz offset	-	-165	-	dBc/Hz	
@ 100 KHz offset	-	-170	-	dBc/Hz	
Start Up Time	-	2	5	ms	

Notes:

1. *When the oscillator is disabled the output is at high impedance. Output is enabled with no connection on pad 1.*
2. *Includes calibration @ 25°C, frequency stability vs. change in temperature, supply voltage and load variations, shock and vibration and 10 years aging.*
3. *BW = 12 KHz to Fo/2 MHz.*

LVCMOS Output Waveform



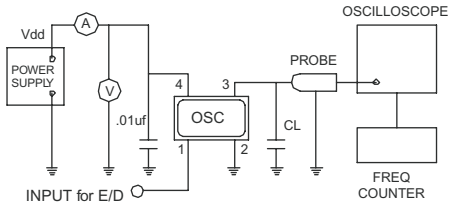
Package Characteristics

Package	Hermetically sealed ceramic package and metal cover

Enable / Disable Function

Pad 1 Input:	Output:
High or Open: (Voh)	Enabled
Low: (Vol)	Disabled (High Impedance)

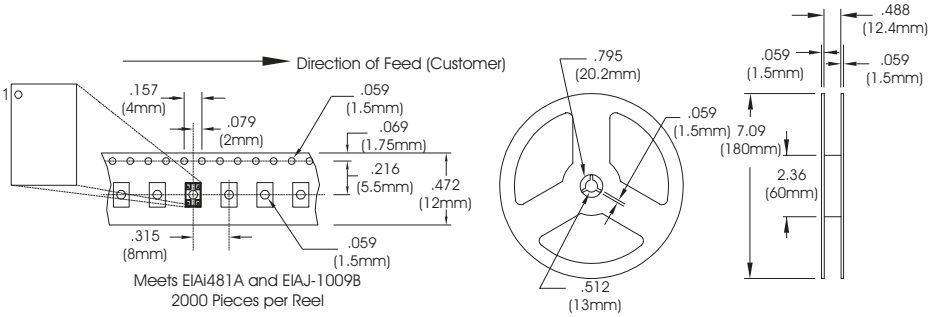
Test Circuit



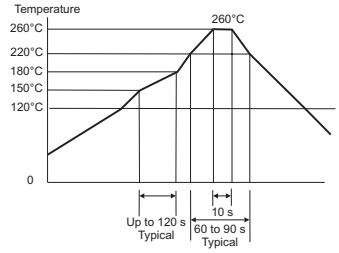
Environmental Characteristics

Vibration:	Vibration per Mil Std 883E Method 2007.3 Test Condition A.
Shock:	Mechanical Shock per Mil Std 883E Method 2002.4 Test Condition B.
Soldering Process:	RoHS compliant lead free. See soldering profile below.

Tape and Reel Dimensions



Solder Profile



Meets IPC/JEDEC J-STD-020C

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