FAIRCHILD SEMICONDUCTOR®

January 2008

FAN2013 — 2A Low-Voltage, Current-Mode Synchronous PWM Buck Regulator

Features

- 95% Efficiency, Synchronous Operation
- Adjustable Output Voltage from 0.8V to V_{IN}-1
- 4.5V to 5.5V Input Voltage Range
- Up to 2A Output Current
- Fixed-Frequency 1.3 MHz PWM Operation
- 100% Duty Cycle Low-Dropout Operation (LDO)
- Soft-Start Function
- Excellent Load Transient Response
- Power-Good Flag
- Over-Voltage, Under-Voltage Lockout, Short-Circuit, and Thermal Shutdown Protections
- 3x3mm 6-lead MLP Package

Applications

- Hard Disk Drive
- Set-Top Box
- Point-of-Load Power
- Notebook Computer
- Communications Equipment

Description

The FAN2013 is a high-efficiency, low-noise, synchronous Pulse Width Modulated (PWM) current-mode DC-DC converter designed for low-voltage applications. It provides up to 2A continuous-load current from the 4.5V to 5.5V input. The output voltage is adjustable over a wide range by means of an external voltage divider.

The FAN2013 is enabled when the input voltage on the V_{IN} pin exceed the UVLO threshold.

A current-mode control loop with a fast transient response ensures excellent line and load regulation. The fixed 1.3MHz switching frequency enables designers to choose a small, inexpensive external inductor and capacitor. Filtering can be accomplished with small components, reducing space and cost.

Protection features include input under-voltage lockout, short-circuit protection, and thermal shutdown. Soft-start limits inrush current during start-up conditions.

The device is available in a 3x3mm 6-lead MLP.

Typical Application

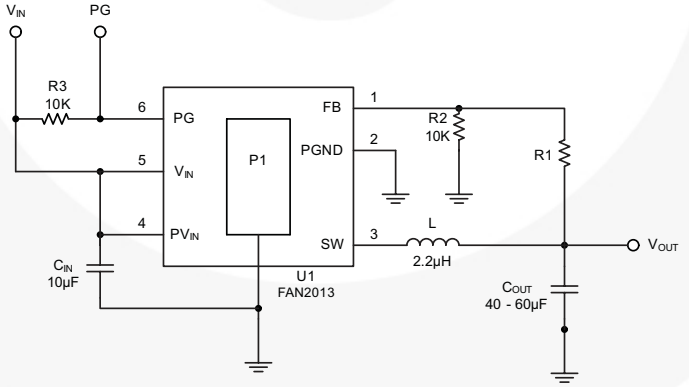


Figure 1. Typical Application

Ordering Information

Part Number	Output Voltage	Package	Packing Method
FAN2013MPX	0.8V to V_{IN}-1V	3x3mm 6-Lead Molded Leadless Package (MLP)	Tape and Reel

All packages are lead free per JEDEC: J-STD-020B standard.

Pin Assignments

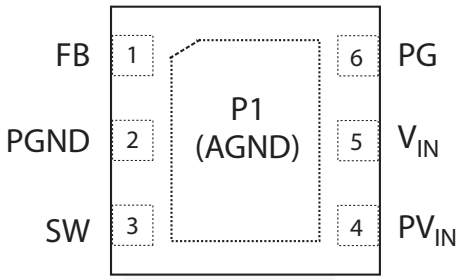


Figure 2. Pin Assignments (Top View)

Pin Definitions

Pin #	Name	Description
P1	AGND	**Analog Ground**. P1 must be soldered to the PCB ground.
1	FB	**Feedback Input**. Adjustable voltage option; connect this pin to the resistor divider.
2	PGND	**Power Ground**. This pin is connected to the internal MOSFET switches. This pin must be externally connected to AGND.
3	SW	**Switching Node**. This pin is connected to the internal MOSFET switches.
4	PVIN	**Supply Voltage Input**. This pin is connected to the internal MOSFET switches.
5	VIN	**Supply Voltage Input**.
6	PG	**Open Drain Power Good**.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	Supply Voltage		-0.3	6.2	V
	Input Voltage on PVIN and Any Other Pin		-0.3	V_{IN}	V
θ_{JC}	Thermal Resistance, Junction-to-Tab[1]			8	°C/W
T_L	Lead Soldering Temperature (10 Seconds)			260	°C
T_{STG}	Storage Temperature		-65	150	°C
T_J	Junction Temperature		-40	150	°C
ESD	Electrostatic Discharge Protection Level[2]	HBM	3.5		kV
		CDM	2		

Notes:

1. Junction-to-ambient thermal resistance, θ_{JA}, is a strong function of PCB material, board thickness, thickness and number of copper planes, number of via used, diameter of via used, available copper surface, and attached heat sink characteristics.
2. Using Mil Std. 883E, method 3015.7 (Human Body Model) and EIA/JESD22C101-A (Charged Device Model).

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbols	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Supply Voltage Range	4.5		5.5	V
V_{OUT}	Output Voltage Range, Adjustable Version	0.8		V_{IN}-1	V
I_{OUT}	Output Current			2.0	A
L	Inductor[3]		2.2		µH
C_{IN}	Input Capacitor[3]	10	20		µF
C_{OUT}	Output Capacitor[3]	20	40		µF
T_A	Operating Ambient Temperature Range	-40		+85	°C

Note:

3. Refer to the *Applications* section for details.

Electrical Characteristics

V_{IN} = 4.5V to 5.5V, V_{OUT} = 1.2V, I_{OUT} = 200mA, C_{IN} = 10µF, C_{OUT} = 40µF, L = 2.2µH, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IN}	Input Voltage		4.5		5.5	V
I_Q	Quiescent Current	I_{OUT} = 0mA		10	16	mA
V_{UVLO}	UVLO Threshold	V_{IN} Rising	3.4	3.7	4.0	V
		Hysteresis		150		mV
R_{ON_PMOS}	PMOS On Resistance	V_{IN} = V_{GS} = 5V		90		MΩ
R_{ON_NMOS}	NMOS On Resistance	V_{IN} = V_{GS} = 5V		90		mΩ
I_{LIMIT}	P-Channel Current Limit	4.5V < V_{IN} < 5.5V	2.8	3.5	4.2	A
T_{OVP}	Over-Temperature Protection	Rising Temperature		150		°C
		Hysteresis		20		°C
f_{SW}	Switching Frequency		1000	1300	1600	kHz
R_{LINE}	Line Regulation	V_{IN} = 4.5 to 5.5V, I_{OUT} = 100mA		0.16		%/V
R_{LOAD}	Load Regulation	0mA ≤ I_{OUT} ≤ 2000mA		0.2	0.6	%
V_{OUT}	Output Voltage During Load Transition[4]	I_{OUT} from 1500mA to 100mA, C_{OUT} = 60µF			5	%
		I_{OUT} from 100mA to 1500mA, C_{OUT} = 60µF	-5			%
I_{LEAK}	Reverse Leakage Current into Pin SW	V_{IN} = Open, EN = GND, V_{SW} = 5.5V		0.1	1.0	µA
V_{REF}	Reference Voltage			0.8		V
V_{OUT}	Output Voltage Accuracy	V_{IN} = 4.5 to 5.5V, 0mA ≤ I_{OUT} ≤ 2000mA, T_A= 0°C to +85°C	-2		2	%
		V_{IN} = 4.5 to 5.5V, 0mA ≤ I_{OUT} ≤ 2000mA, T_A= -40°C to +85°C	-3		3	%
V_{PG}	Power Good Output Threshold and Hysteresis	FB Voltage Rising		0.85 x V_{OUT}		%
		Hysteresis		2		V
t_{PG}	Power Good Output Delay			100		µs
V_{PG_LOW}	Power Good Voltage Low	I_{sink}=6mA, Open-Drain Output			0.4	V
V_{OVP}	Over-Voltage Protection Threshold and Hysteresis	FB Voltage Rising		1.07 x V_{OUT}		V
		Hysteresis		2		%

Notes:

4. Please refer to the load transient response test waveform shown in Figure 3.

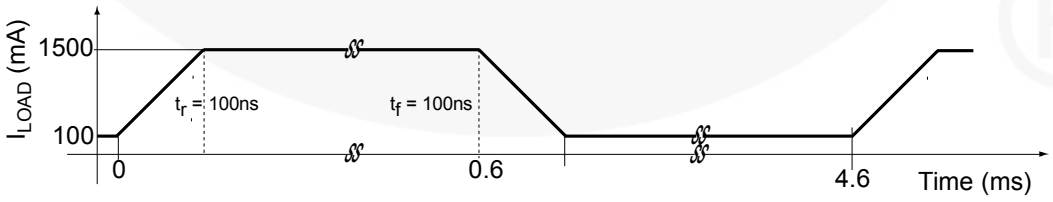


Figure 3. Load Transient Response Test Waveform

Typical Performance Characteristics

T_A = 25°C, C_{IN} = 10µF, C_{OUT} = 40µF, L = 2.2µH, V_{IN} = 5V, V_{OUT} = 1.2V, unless otherwise noted.

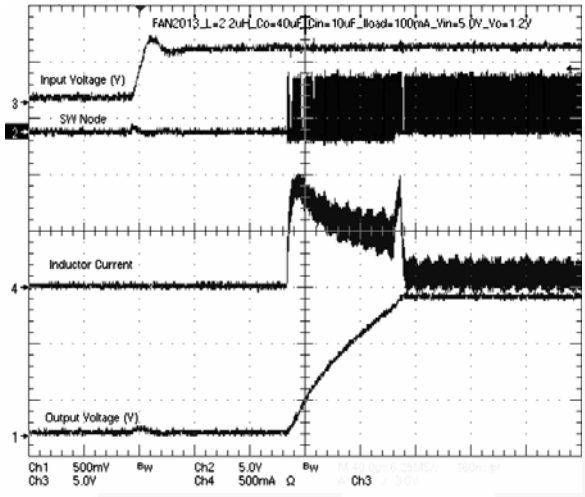


Figure 4. Start-up with 100mA Resistive Load

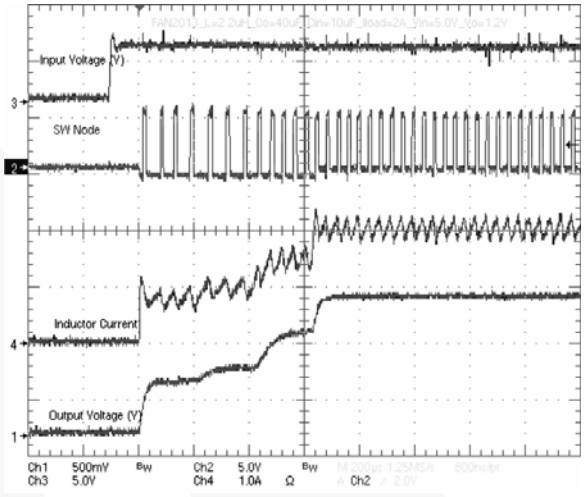


Figure 5. Start-up with 2A Resistive Load

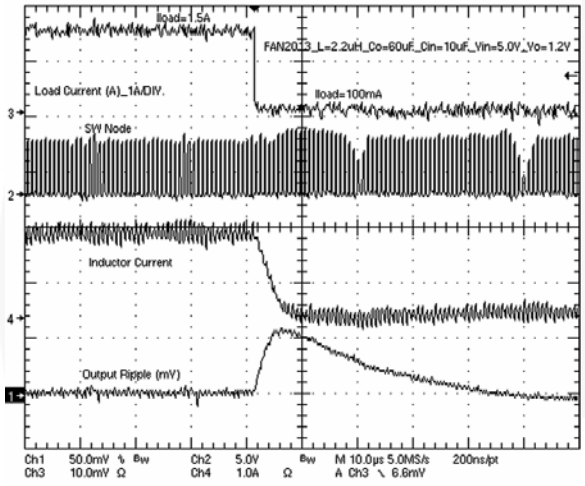


Figure 6. Load Transient Response 1.5A to 100mA

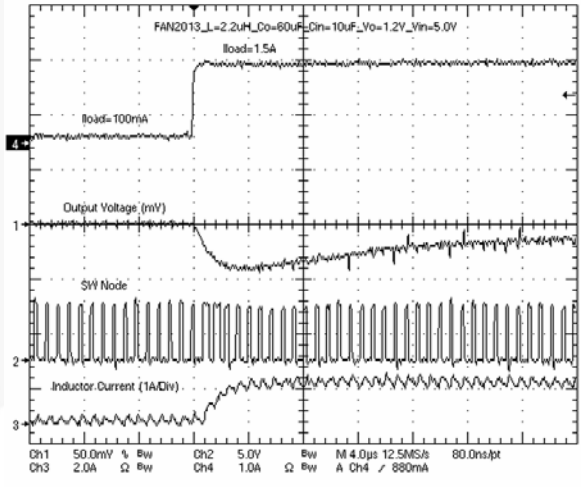


Figure 7. Load Transient Response 100mA to 1.5A

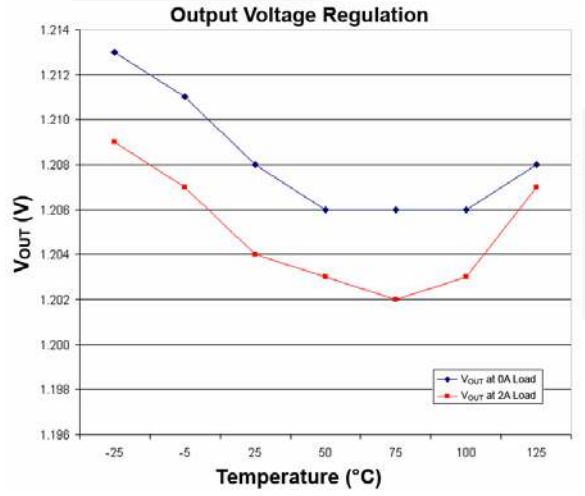


Figure 8. Output Voltage Regulation

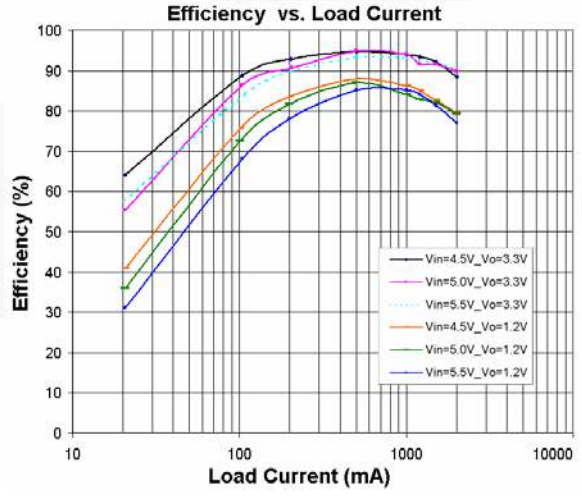


Figure 9. Power Efficiency

Block Diagram

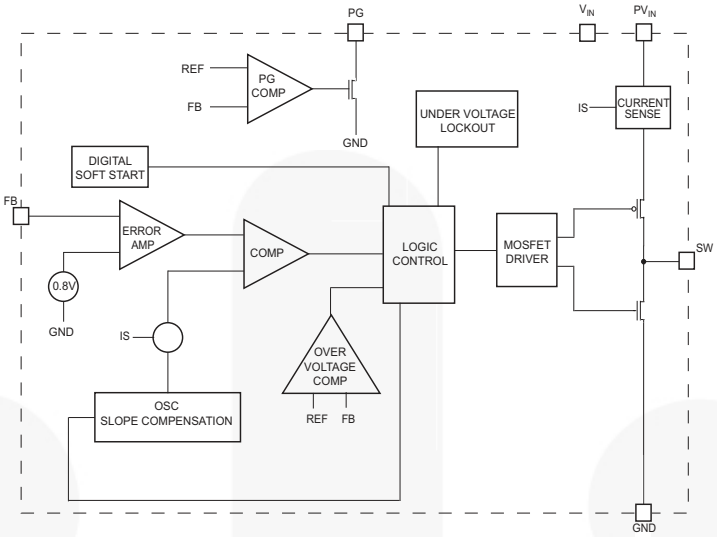


Figure 10. Block Diagram

Detailed Operation Description

The FAN2013 is a step-down pulse-width modulated (PWM) current mode converter with a fixed switching frequency of 1.3MHz. At the rising edge of each clock cycle, the P-channel transistor is turned on until the PWM comparator trips or the current limit is reached. During the ON time, the inductor current ramps up and is monitored by the internal current-mode control loop. After a minimum dead time, the N-channel transistor is turned ON and the inductor current ramps down. As the clock cycle is completed, the N-channel switch is turned OFF and the next clock cycle starts. The duty cycle is given by the ratio of output voltage and input voltage. The converter runs at minimum duty cycle when output voltage is at minimum and input voltage is at maximum, and at 100% duty cycle when the input voltage approaches the output voltage, as described below.

100% Duty Cycle Operation

As the input voltage approaches the output voltage and the duty cycle exceeds the typical 95%, the converter turns the P-channel transistor continuously on. In this mode, the output voltage is equal to the input voltage, minus the voltage drop across the P-channel transistor:

$$V_{OUT} = V_{IN} – I_{LOAD} \times (R_{DS\_ON} + R_L) \quad (1)$$

where
R_{DS_ON} = P-channel switch on resistance
I_{LOAD} = Output current
R_L = Inductor DC resistance

UVLO and Soft Start

The internal voltage reference, V_{REF}, and the IC remain reset until V_{IN} reaches the 3.7V UVLO threshold.

The FAN2013 has an internal soft-start circuit that limits the inrush current during start-up. This prevents possible voltage drops of the input voltage and eliminates the output voltage overshoot. The soft-start is implemented as a digital circuit, increasing the switch current in four steps to the P-channel current limit (3.5A). Typical start-up time for a 40µF output capacitor with a load current of 2.0A is 800µs.

Output Over-Voltage Protection

When output voltage, V_{OUT}, reaches approximately 7% above the nominal value, the device turns OFF the P-channel switch and turns ON part of the N-channel transistor with a built-in current limit of about 400mA. When V_{OUT} reaches the hysteresis of about 2%, the device starts switching normally in closed loop. If output voltage is pulled up by an external voltage source with a current limit higher than typical 400mA, the output voltage stays up at the external voltage source level.

The over-voltage protection is designed to limit the output voltage excursion in case of a transient response from full load to a minimum load.

Output Short-Circuit Protection

The switch peak current is limited cycle by cycle to a typical value of 3.5A. In the event of an output voltage short circuit, the device operates with a frequency of 400kHz and minimum duty cycle, making the average typical input current .45A.

Thermal Shutdown

When the die temperature exceeds 150°C, a reset occurs and remains in effect until the die cools to 130°C, when the circuit is allowed to restart.

Applications Information

Setting the Output Voltage

The internal voltage reference is 0.8V. The output is divided down by a voltage divider, R1 and R2 to the FB pin. The output voltage is:

$$V_{OUT} = V_{REF}\left(1 + \frac{R_1}{R_2}\right) \quad (2)$$

According to this equation, assuming desired output voltage of 1.2V, and given R2 = 10KΩ as the recommended resistance for any output voltage setting, the calculated value of R1 is 5KΩ.

Inductor Selection

The inductor parameters directly related to device performance are saturation current and DC resistance. The FAN2013 operates with a typical inductor value of 2.2µH. The lower the DC resistance, the higher the efficiency. For saturation current, the inductor should be rated higher than the maximum load current, plus half of the inductor ripple current, calculated by:

$$\Delta I_L = V_{OUT} \times \frac{1-(V_{OUT}/V_{IN})}{L \times f} \quad (3)$$

where:
ΔI_L = Inductor Ripple Current
f = Switching Frequency
L = Inductor Value

Recommended inductors are listed in Table1.

Table 1. Recommended Inductors

Inductor Value	Vendor	Part Number
2.2µH	Coiltronics	SD25 2R2
2.2µH	Murata	LQH66SSN2R2M03

Capacitors Selection

For best performances, a low-ESR input capacitor is required. A ceramic capacitor of at least 10µF, placed as close to the V_{IN} and AGND pins as possible is recommended.

The output capacitor determines the output ripple and the transient response. A minimum of 20µF output capacitor is required for the FAN2013 to operate in stable conditions.

Table 2. Recommended Capacitors

Capacitor Value	Vendor	Part Number
10µF	Taiyo Yuden	JMK212BJ106MG
		JMK316BJ106KL
	TDK	C2012X5ROJ106K
		C3216X5ROJ106M
	Murata	GRM32ER61C106K

PCB Layout Recommendations

The inherently high peak currents and switching frequency of power supplies require a careful PCB layout design. For best results, use wide traces for high-current paths and place the input capacitor, the inductor, and the output capacitor as close as possible to the integrated circuit terminals. To minimize voltage stress to the device resulting from ever-present switching spikes, use an input bypass capacitor with low ESR. Note that the peak amplitude of the switching spikes depends upon the load current; the higher the load current, the higher the switching spikes.

The resistor divider that sets the output voltage should be routed away from the inductor to avoid RF coupling. The ground plane at the bottom side of the PCB acts as an electromagnetic shield to reduce EMI. The recommended PCB layout is shown below in Figure 11.

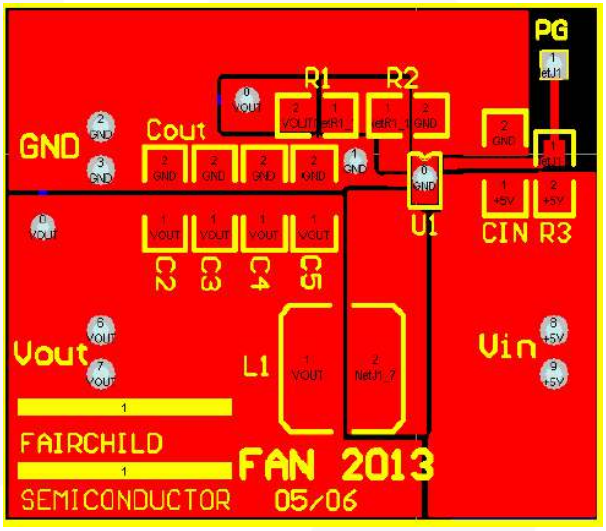
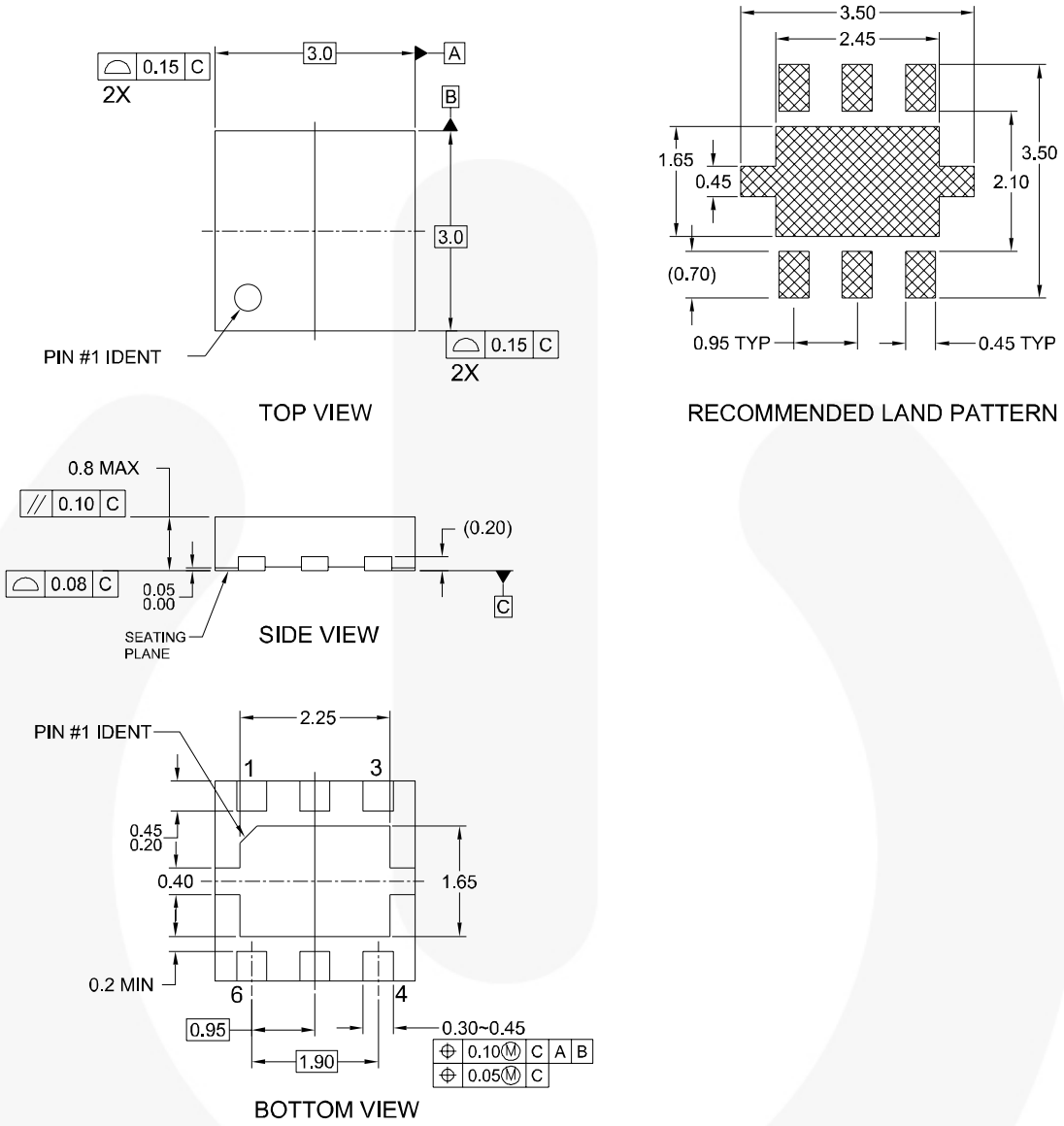


Figure 11. Recommended PCB Layout

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-229,
VARIATION WEEA, DATED 11/2001
EXCEPT FOR DAP EXTENSION TABS

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER
ASME Y14.5M, 1994

MLP06FrevA

Figure 12. 3x3mm 6-Lead Molded Leadless Package (MLP)

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