

# LOW POWER, SINGLE-SUPPLY, RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

## *MicroAmplifier™* Series

### FEATURES

- RAIL-TO-RAIL INPUT
- RAIL-TO-RAIL OUTPUT (within 1mV)
- LOW QUIESCENT CURRENT: 150 $\mu$ A typ
- *Micro*SIZE PACKAGES
  - SOT23-5
  - MSOP-8
  - TSSOP-14
- GAIN-BANDWIDTH
  - OPA344: 1MHz,  $G \geq 1$
  - OPA345: 3MHz,  $G \geq 5$
- SLEW RATE
  - OPA344: 0.8V/ $\mu$ s
  - OPA345: 2V/ $\mu$ s
- THD + NOISE: 0.006%

### APPLICATIONS

- PCMCIA CARDS
- DATA ACQUISITION
- PROCESS CONTROL
- AUDIO PROCESSING
- COMMUNICATIONS
- ACTIVE FILTERS
- TEST EQUIPMENT

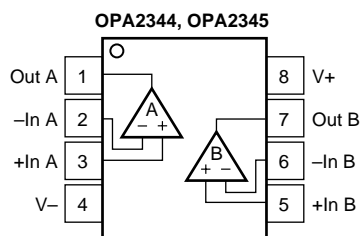
### DESCRIPTION

The OPA344 and OPA345 series rail-to-rail CMOS operational amplifiers are designed for precision, low-power, miniature applications. The OPA344 is unity gain stable, while the OPA345 is optimized for gains greater than or equal to five, and has a gain-bandwidth product of 3MHz.

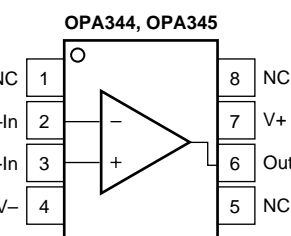
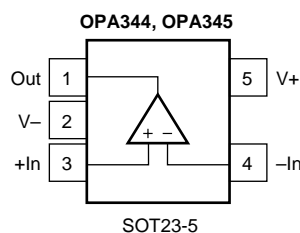
The OPA344 and OPA345 are optimized to operate on a single supply from 2.5V and up to 5.5V with an input common-mode voltage range that extends 300mV beyond the supplies. Quiescent current is only 250 $\mu$ A (max).

Rail-to-rail input and output make them ideal for driving sampling analog-to-digital converters. They are also well suited for general purpose and audio applications and providing I/V conversion at the output of D/A converters. Single, dual and quad versions have identical specs for design flexibility.

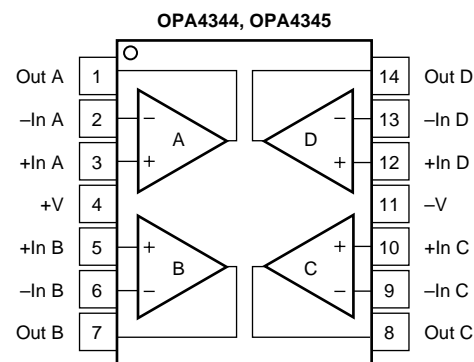
A variety of packages are available. All are specified for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . A SPICE macromodel is available for download from [www.ti.com](http://www.ti.com).



SO-8, MSOP-8, 8-Pin DIP (OPA2344 Only)



SO-8, 8-Pin DIP (OPA344 Only)



TSSOP-14, SO-14, 14-Pin DIP (OPA4344 Only)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

# SPECIFICATIONS: $V_S = 2.7V$ to $5.5V$

At  $T_A = +25^\circ C$ ,  $R_L = 10k\Omega$  connected to  $V_S/2$  and  $V_{OUT} = V_S/2$ , unless otherwise noted.  
**Boldface** limits apply over the temperature range,  $T_A = -40^\circ C$  to  $+85^\circ C$ .

PARAMETER	CONDITION	OPA344NA, UA, PA OPA2344EA, UA, PA OPA4344EA, UA, PA			UNITS
		MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b> Input Offset Voltage <b>Over Temperature</b> <b>vs Temperature</b> vs Power Supply <b>Over Temperature</b> Channel Separation, dc $f = 1kHz$	$V_{OS}$  $dV_{OS}/dT$ $PSRR$  $V_S = +5.5V, V_{CM} = V_S/2$  $V_S = 2.7V$ to $5.5V, V_{CM} < (V+) - 1.8V$ <b><math>V_S = 2.7V</math> to <math>5.5V, V_{CM} &lt; (V+) - 1.8V</math></b>		$\pm 0.2$ <b><math>\pm 0.8</math></b> $\pm 3$ 30  0.2 130	$\pm 1$ <b><math>\pm 1.2</math></b>  200 <b>250</b>	mV mV $\mu V/^\circ C$ $\mu V/V$ $\mu V/V$ $\mu V/V$ dB
<b>INPUT BIAS CURRENT</b> Input Bias Current <b>Over Temperature</b> Input Offset Current	$I_B$  $I_{OS}$		$\pm 0.2$ <b>See Typical Curve</b> $\pm 0.2$	$\pm 10$  $\pm 10$	pA pA pA
<b>NOISE</b> Input Voltage Noise Input Voltage Noise Density Current Noise Density	$e_n$ $i_n$  $f = 0.1$ to $50kHz$ $f = 10kHz$ $f = 10kHz$		8 30 0.5		$\mu V_{rms}$ $nV/\sqrt{Hz}$ $fA/\sqrt{Hz}$
<b>INPUT VOLTAGE RANGE</b> Common-Mode Voltage Range Common-Mode Rejection Ratio <b>Over Temperature</b> Common-Mode Rejection <b>Over Temperature</b> Common-Mode Rejection <b>Over Temperature</b>	$V_{CM}$ CMRR CMRR CMRR CMRR  $V_S = +5.5V, -0.3V < V_{CM} < (V+) - 1.8$ <b><math>V_S = +5.5V, -0.3V &lt; V_{CM} &lt; (V+) - 1.8</math></b> $V_S = +5.5V, -0.3V < V_{CM} < 5.8V$ <b><math>V_S = +5.5V, -0.3V &lt; V_{CM} &lt; 5.8V</math></b> $V_S = +2.7V, -0.3V < V_{CM} < 3V$ <b><math>V_S = +2.7V, -0.3V &lt; V_{CM} &lt; 3V</math></b>	-0.3 76 <b>74</b> 70 <b>68</b> 66 <b>64</b>	92  84  80	$(V+) + 0.3$	V dB dB dB dB dB
<b>INPUT IMPEDANCE</b> Differential Common-Mode			$10^{13} \parallel 3$ $10^{13} \parallel 6$		$\Omega \parallel pF$ $\Omega \parallel pF$
<b>OPEN-LOOP GAIN</b> Open-Loop Voltage Gain <b>Over Temperature</b>  <b>Over Temperature</b>	$A_{OL}$    $R_L = 100k\Omega, 10mV < V_O < (V+) - 10mV$ <b><math>R_L = 100k\Omega, 10mV &lt; V_O &lt; (V+) - 10mV</math></b> $R_L = 5k\Omega, 400mV < V_O < (V+) - 400mV$ <b><math>R_L = 5k\Omega, 400mV &lt; V_O &lt; (V+) - 400mV</math></b>	104 <b>100</b> 96 <b>90</b>	122  120		dB dB dB dB
<b>FREQUENCY RESPONSE</b> Gain-Bandwidth Product Slew Rate Settling Time, 0.1% 0.01% Overload Recovery Time Total Harmonic Distortion + Noise	GBW SR   $THD+N$  $C_L = 100pF$  $V_S = 5.5V, 2V$ Step $V_S = 5.5V, 2V$ Step $V_{IN} \cdot G = V_S$ $V_S = 5.5V, V_O = 3Vp-p, G = 1, f = 1kHz$		1 0.8 5 8 2.5 0.006		MHz $V/\mu s$ $\mu s$ $\mu s$ $\mu s$ %
<b>OUTPUT</b> Voltage Output Swing from Rail <sup>(1)</sup>  <b>Over Temperature</b>  <b>Over Temperature</b> Short-Circuit Current Capacitive Load Drive	$I_{SC}$ $C_{LOAD}$   $R_L = 100k\Omega, A_{OL} \geq 96dB$ $R_L = 100k\Omega, A_{OL} \geq 104dB$ <b><math>R_L = 100k\Omega, A_{OL} \geq 100dB</math></b> $R_L = 5k\Omega, A_{OL} \geq 96dB$ <b><math>R_L = 5k\Omega, A_{OL} \geq 90dB</math></b>		1 3 40  $\pm 15$ See Typical Curve	10 <b>10</b> 400 <b>400</b>	mV mV mV mV mA
<b>POWER SUPPLY</b> Specified Voltage Range Operating Voltage Range Quiescent Current (per amplifier) <b>Over Temperature</b>	$V_S$  $I_Q$  $V_S = 5.5V, I_Q = 0$	2.7	2.5 to 5.5 150	5.5 250 <b>300</b>	V V $\mu A$ $\mu A$
<b>TEMPERATURE RANGE</b> Specified Range Operating Range Storage Range Thermal Resistance SOT23-5 Surface Mount MSOP-8 Surface Mount 8-Pin DIP SO-8 Surface Mount TSSOP-14 Surface Mount 14-Pin DIP SO-14 Surface Mount	$\theta_{JA}$	-40 -55 -65		85 125 150	$^\circ C$ $^\circ C$ $^\circ C$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$

NOTE: (1) Output voltage swings are measured between the output and power-supply rails.

# SPECIFICATIONS: $V_S = 2.7V$ to $5.5V$

At  $T_A = +25^\circ C$ ,  $R_L = 10k\Omega$  connected to  $V_S/2$  and  $V_{OUT} = V_S/2$ , unless otherwise noted.  
**Boldface** limits apply over the temperature range,  $T_A = -40^\circ C$  to  $+85^\circ C$ .

PARAMETER	CONDITION	OPA345NA, UA OPA2345EA, UA OPA4345EA, UA			UNITS
		MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b> Input Offset Voltage $V_{OS}$ <b>Over Temperature vs Temperature</b> $dV_{OS}/dT$ vs Power Supply <b>Over Temperature</b> Channel Separation, dc $f = 1kHz$	$V_S = +5.5V, V_{CM} = V_S/2$  $V_S = 2.7V$ to $5.5V, V_{CM} < (V+) - 1.8V$ <b><math>V_S = 2.7V</math> to <math>5.5V, V_{CM} &lt; (V+) - 1.8V</math></b>		$\pm 0.2$ <b><math>\pm 0.8</math></b> $\pm 3$ 30  0.2 130	$\pm 1$ <b><math>\pm 1.2</math></b>  200 <b>250</b>	mV mV $\mu V/^\circ C$ $\mu V/V$ $\mu V/V$ $\mu V/V$ dB
<b>INPUT BIAS CURRENT</b> Input Bias Current $I_B$ <b>Over Temperature</b> Input Offset Current $I_{OS}$			$\pm 0.2$ <b>See Typical Curve</b> $\pm 0.2$	$\pm 10$  $\pm 10$	pA pA pA
<b>NOISE</b> Input Voltage Noise Input Voltage Noise Density $e_n$ Current Noise Density $i_n$	$f = 0.1$ to $50kHz$ $f = 10kHz$ $f = 10kHz$		8 30 0.5		$\mu V_{rms}$ $nV/\sqrt{Hz}$ $fA/\sqrt{Hz}$
<b>INPUT VOLTAGE RANGE</b> Common-Mode Voltage Range $V_{CM}$ Common-Mode Rejection Ratio $CMRR$ <b>Over Temperature</b> Common-Mode Rejection Ratio $CMRR$ <b>Over Temperature</b> Common-Mode Rejection Ratio $CMRR$ <b>Over Temperature</b>	$V_S = +5.5V, -0.3V < V_{CM} < (V+) - 1.8$ <b><math>V_S = +5.5V, -0.3V &lt; V_{CM} &lt; (V+) - 1.8</math></b> $V_S = +5.5V, -0.3V < V_{CM} < 5.8V$ <b><math>V_S = +5.5V, -0.3V &lt; V_{CM} &lt; 5.8V</math></b> $V_S = +2.7V, -0.3V < V_{CM} < 3V$ <b><math>V_S = +2.7V, -0.3V &lt; V_{CM} &lt; 3V</math></b>	-0.3 76 <b>74</b> 70 <b>68</b> 66 <b>64</b>	92  84  80	$(V+) + 0.3$	V dB dB dB dB dB dB
<b>INPUT IMPEDANCE</b> Differential Common-Mode			$10^{13} \parallel 3$ $10^{13} \parallel 6$		$\Omega \parallel pF$ $\Omega \parallel pF$
<b>OPEN-LOOP GAIN</b> Open-Loop Voltage Gain $A_{OL}$ <b>Over Temperature</b>  <b>Over Temperature</b>	$R_L = 100k\Omega, 10mV < V_O < (V+) - 10mV$ <b><math>R_L = 100k\Omega, 10mV &lt; V_O &lt; (V+) - 10mV</math></b> $R_L = 5k\Omega, 400mV < V_O < (V+) - 400mV$ <b><math>R_L = 5k\Omega, 400mV &lt; V_O &lt; (V+) - 400mV</math></b>	104 <b>100</b> 96 <b>90</b>	122  120		dB dB dB dB
<b>FREQUENCY RESPONSE</b> Gain-Bandwidth Product $GBW$ Slew Rate $SR$ Settling Time, 0.1% 0.01% Overload Recovery Time Total Harmonic Distortion + Noise $THD+N$	$C_L = 100pF$  $G = 5, 2V$ Output Step $G = 5, 2V$ Output Step $V_{IN} \cdot G = V_S$ $V_S = 5.5V, V_O = 2.5V_{p-p}, G = 5, f = 1kHz$		3 2 1.5 1.6 2.5 0.006		MHz $V/\mu s$ $\mu s$ $\mu s$ $\mu s$ %
<b>OUTPUT</b> Voltage Output Swing from Rail <sup>(1)</sup>  <b>Over Temperature</b>  <b>Over Temperature</b> Short-Circuit Current $I_{SC}$ Capacitive Load Drive $C_{LOAD}$	$R_L = 100k\Omega, A_{OL} \geq 96dB$ $R_L = 100k\Omega, A_{OL} \geq 104dB$ <b><math>R_L = 100k\Omega, A_{OL} \geq 100dB</math></b> $R_L = 5k\Omega, A_{OL} \geq 96dB$ <b><math>R_L = 5k\Omega, A_{OL} \geq 90dB</math></b>		1 3  40  $\pm 15$ See Typical Curve	10 <b>10</b> 400 <b>400</b>	mV mV mV mV mV mA
<b>POWER SUPPLY</b> Specified Voltage Range $V_S$ Operating Voltage Range Quiescent Current (per amplifier) $I_Q$ <b>Over Temperature</b>	$V_S = 5.5V, I_Q = 0$	2.7	2.5 to 5.5 150	5.5 250 <b>300</b>	V V $\mu A$ $\mu A$
<b>TEMPERATURE RANGE</b> Specified Range Operating Range Storage Range Thermal Resistance $\theta_{JA}$ SOT23-5 Surface Mount MSOP-8 Surface Mount SO-8 Surface Mount TSSOP-14 Surface Mount SO-14 Surface Mount		-40 -55 -65		85 125 150	$^\circ C$ $^\circ C$ $^\circ C$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$

NOTE: (1) Output voltage swings are measured between the output and power-supply rails.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Voltage, V+ to V- .....	7.5V
Signal Input Terminals, Voltage <sup>(2)</sup> .....	(V-) -0.5V to (V+) +0.5V
Current <sup>(2)</sup> .....	10mA
Output Short-Circuit <sup>(3)</sup> .....	Continuous
Operating Temperature .....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
Junction Temperature .....	150°C
Lead Temperature (soldering, 10s) .....	300°C
ESD Tolerance (Human Body Model) .....	4000V

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only. Functional operation of the device at these conditions, or beyond the specified operating conditions, is not implied. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

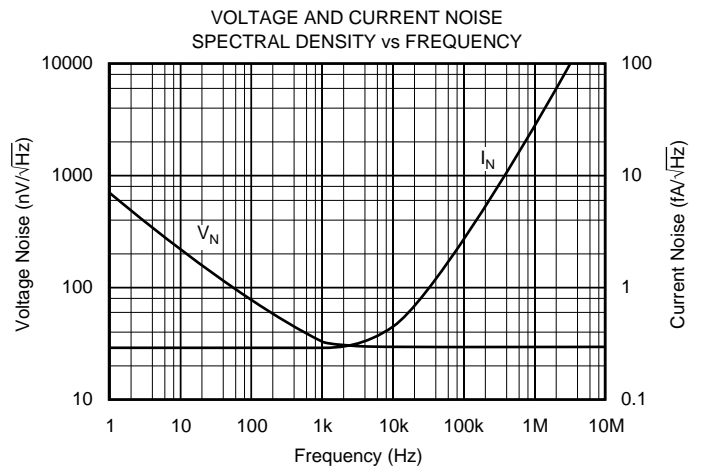
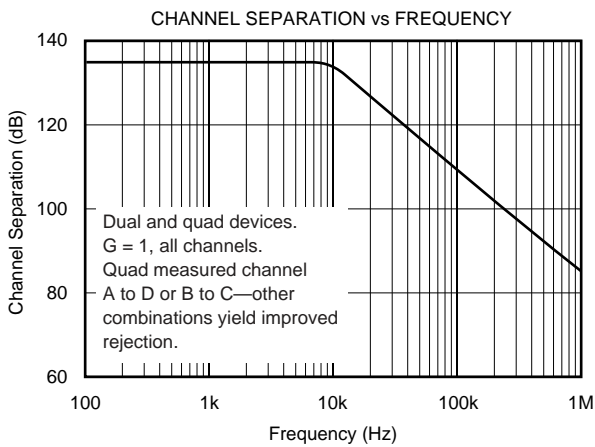
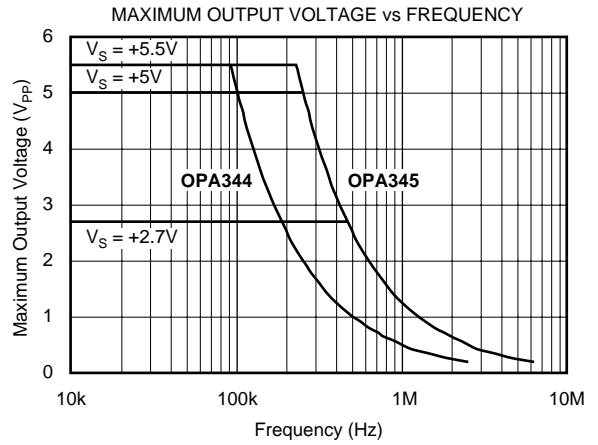
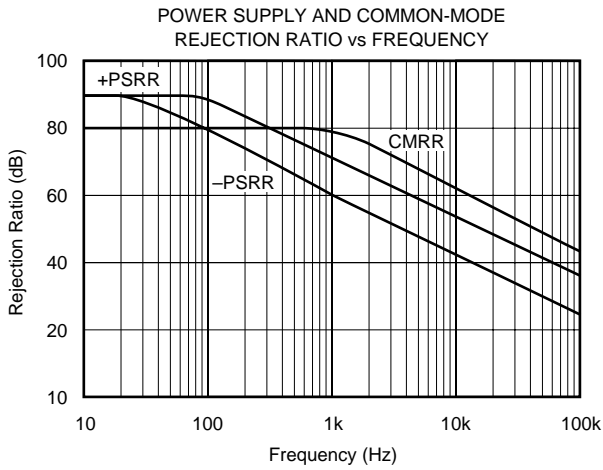
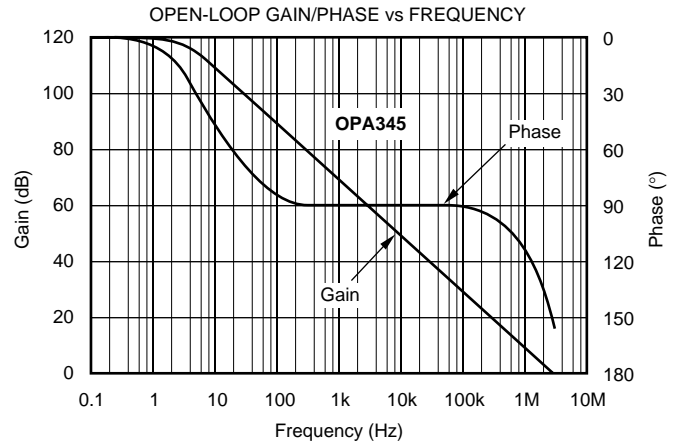
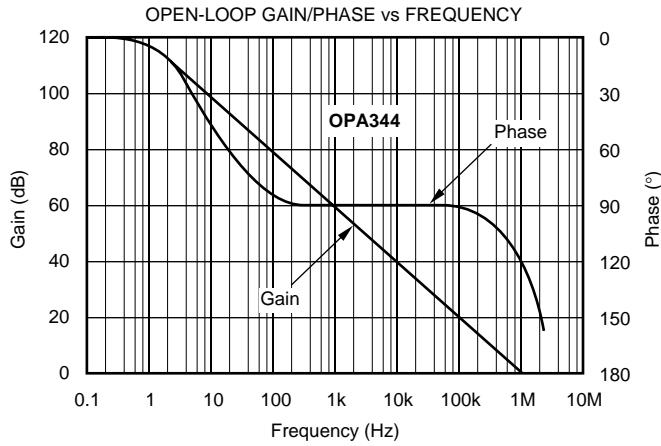
PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER <sup>(2)</sup>	TRANSPORT MEDIA
OPA344NA "	SOT23-5 "	DBV "	-40°C to +85°C "	B44 "	OPA344NA/250 OPA344NA/3K	Tape and Reel Tape and Reel
OPA344UA "	SO-8 "	D "	-40°C to +85°C "	OPA344UA "	OPA344UA OPA344UA/2K5	Rails Tape and Reel
OPA344PA	8-Pin Dip	P	-40°C to +85°C	OPA344PA	OPA344PA	Rails
OPA2344EA "	MSOP-8 "	DGK "	-40°C to +85°C "	C44 "	OPA2344EA/250 OPA2344EA/2K5	Tape and Reel Tape and Reel
OPA2344UA "	SO-8 "	D "	-40°C to +85°C "	OPA2344UA "	OPA2344UA OPA2344UA/2K5	Rails Tape and Reel
OPA2344PA	8-Pin DIP	P	-40°C to +85°C	OPA2344PA	OPA2344PA	Rails
OPA4344EA "	TSSOP-14 "	PW "	-40°C to +85°C "	OPA4344EA "	OPA4344EA/250 OPA4344EA/2K5	Rails Tape and Reel
OPA4344UA "	SO-14 "	D "	-40°C to +85°C "	OPA4344UA "	OPA4344UA OPA4344UA/2K5	Rails Tape and Reel
OPA4344PA	14-Pin DIP	N	-40°C to +85°C	OPA4344PA	OPA4344PA	Rails
OPA345NA "	SOT23-5 "	DBV "	-40°C to +85°C "	A45 "	OPA345NA/250 OPA345NA/3K	Tape and Reel Tape and Reel
OPA345UA "	SO-8 "	D "	-40°C to +85°C "	OPA345UA "	OPA345UA OPA345UA/2K5	Rails Tape and Reel
OPA2345EA "	MSOP-8 "	DGK "	-40°C to +85°C "	B45 "	OPA2345EA/250 OPA2345EA/2K5	Tape and Reel Tape and Reel
OPA2345UA "	SO-8 "	D "	-40°C to +85°C "	OPA2345UA "	OPA2345UA OPA2345UA/2K5	Rails Tape and Reel
OPA4345EA "	TSSOP-14 "	PW "	-40°C to +85°C "	OPA4345EA "	OPA4345EA/250 OPA4345EA/2K5	Tape and Reel Tape and Reel
OPA4345UA "	SO-14 "	D "	-40°C to +85°C "	OPA4345UA "	OPA4345UA OPA4345UA/2K5	Rails Tape and Reel

NOTES: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "OPA344UA/2K5" will get a single 2500-piece Tape and Reel.

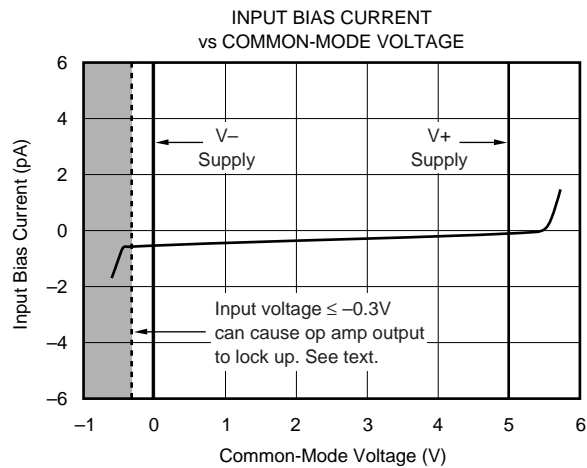
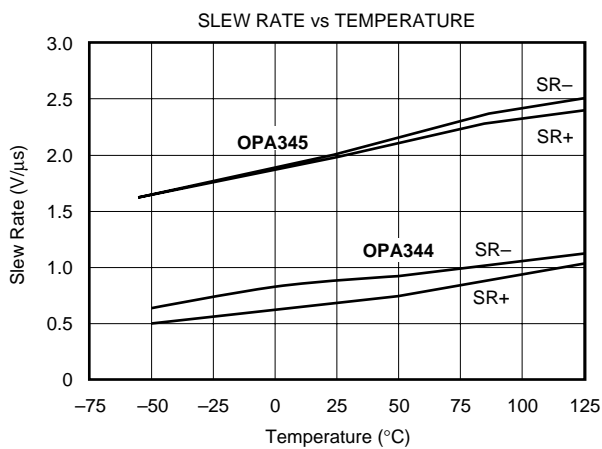
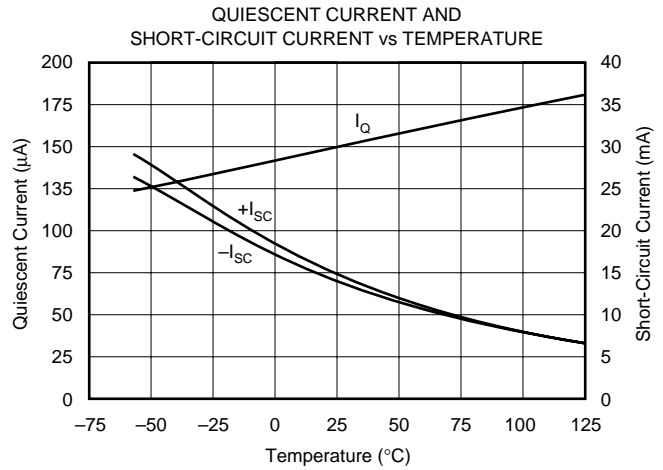
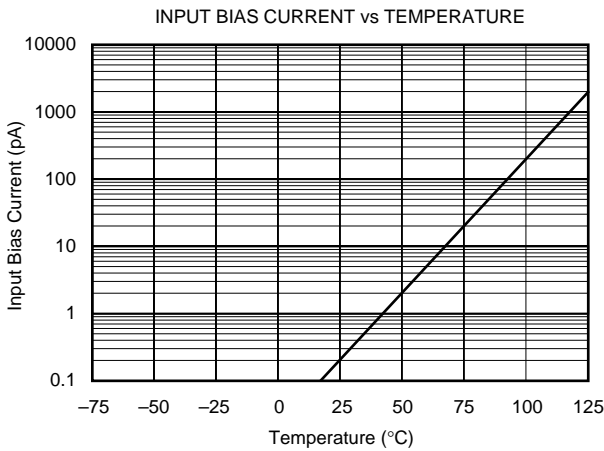
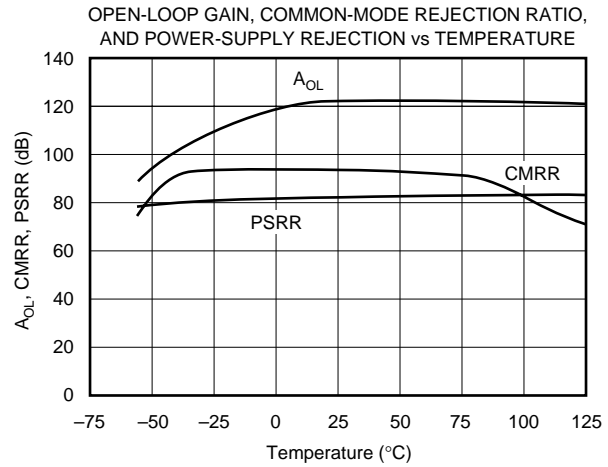
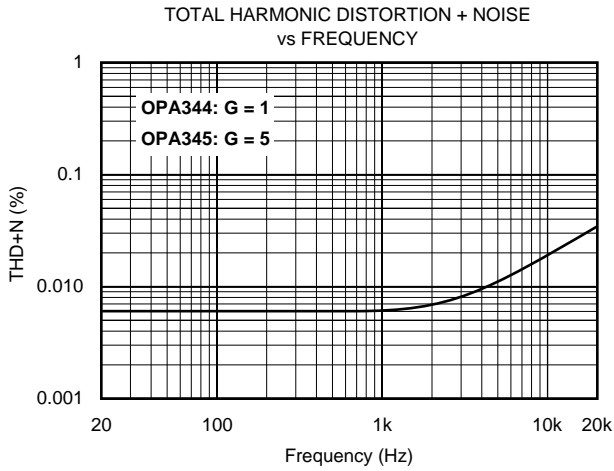
# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , unless otherwise noted.



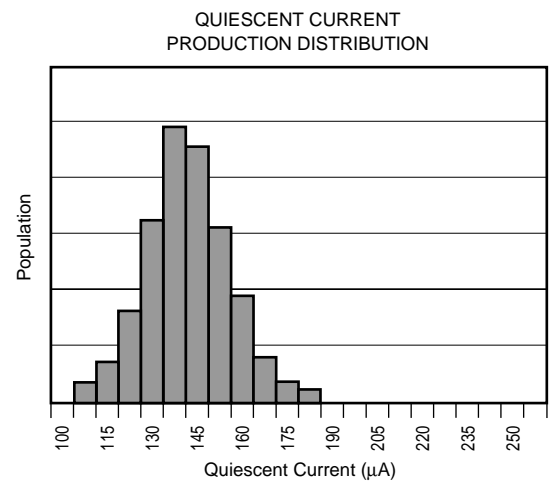
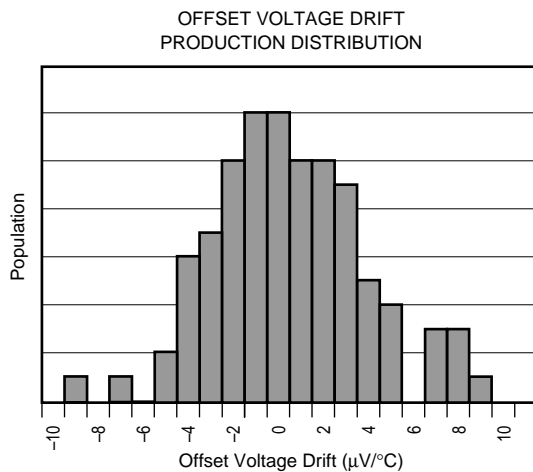
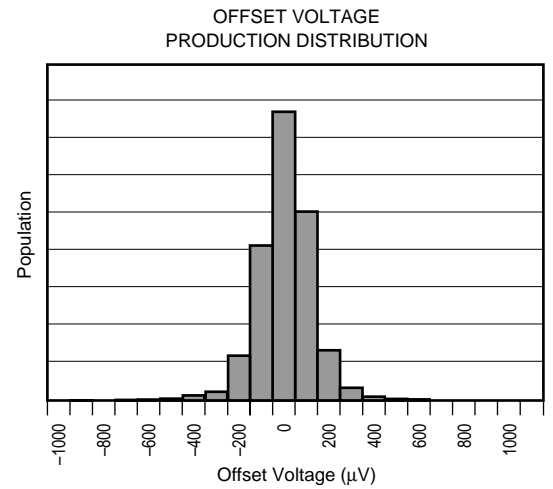
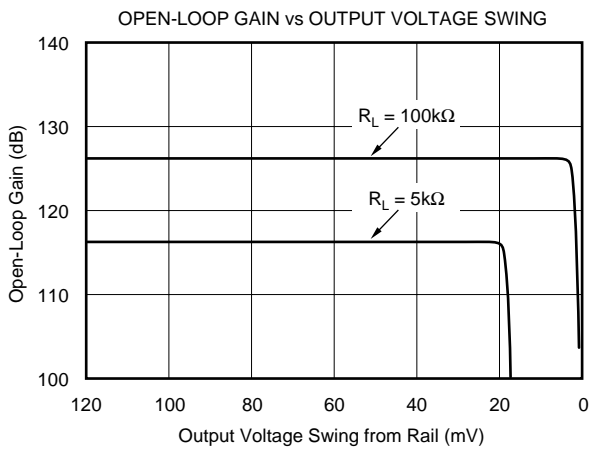
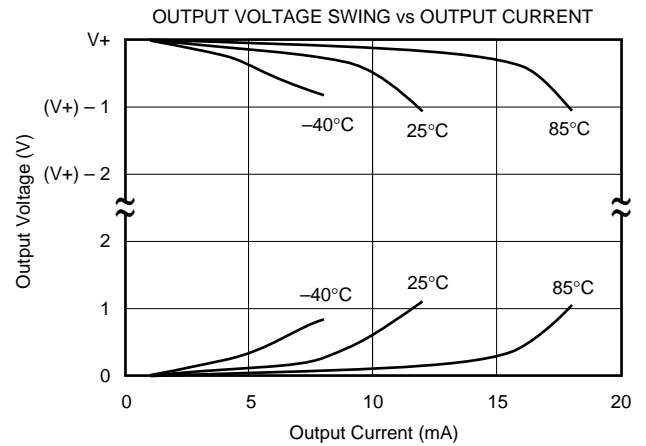
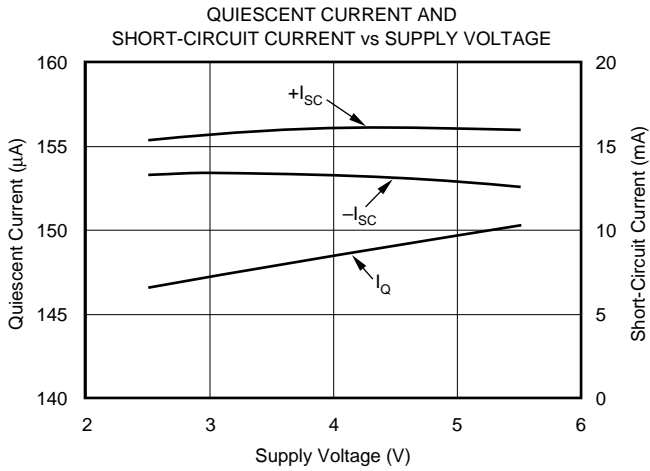
# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , unless otherwise noted.



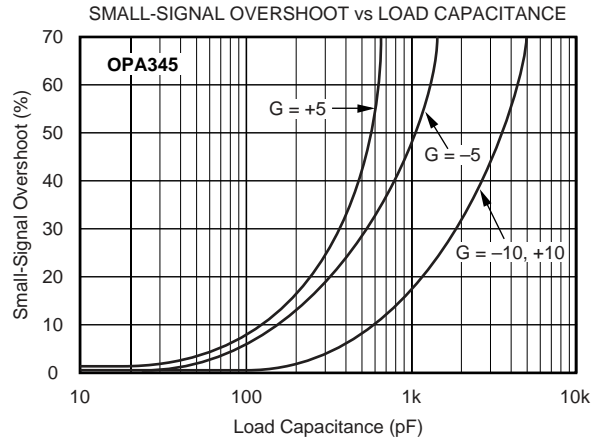
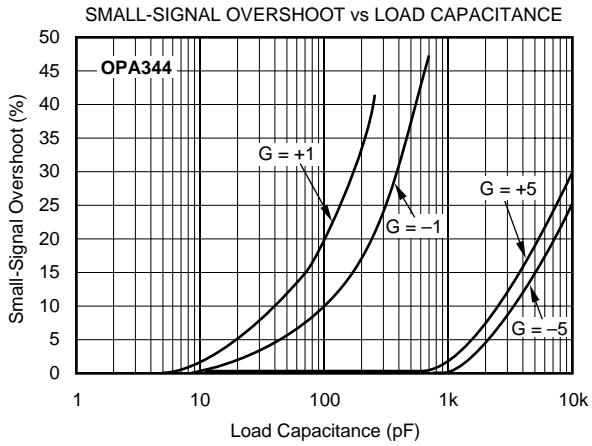
# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (Cont.)

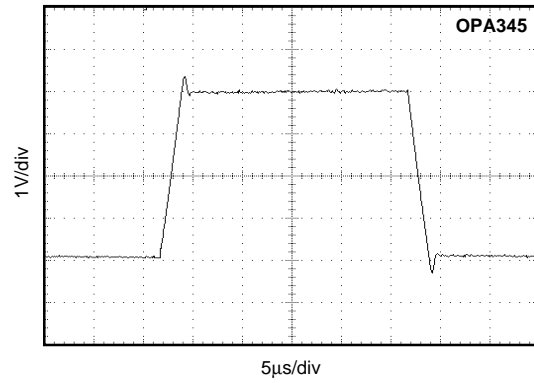
At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , unless otherwise noted.



LARGE-SIGNAL STEP RESPONSE: OPA344  
 $G = +1$ ,  $R_L = 10\text{k}\Omega$ ,  $C_L = 100\text{pF}$



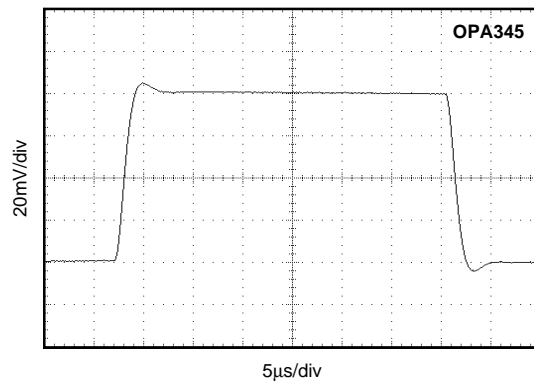
LARGE-SIGNAL STEP RESPONSE: OPA345  
 $G = +5$ ,  $R_L = 10\text{k}\Omega$ ,  $C_L = 100\text{pF}$



SMALL-SIGNAL STEP RESPONSE: OPA344  
 $G = +1$ ,  $R_L = 10\text{k}\Omega$ ,  $C_L = 100\text{pF}$



SMALL-SIGNAL STEP RESPONSE: OPA345  
 $G = +5$ ,  $R_L = 10\text{k}\Omega$ ,  $C_L = 100\text{pF}$





# APPLICATIONS INFORMATION

OPA344 series op amps are unity gain stable and can operate on a single supply, making them highly versatile and easy to use. OPA345 series op amps are optimized for applications requiring higher speeds with gains of 5 or greater.

Rail-to-rail input and output swing significantly increases dynamic range, especially in low supply applications. Figure 1 shows the input and output waveforms for the OPA344 in unity-gain configuration. Operation is from  $V_S = +5V$  with a  $10k\Omega$  load connected to  $V_S/2$ . The input is a  $5Vp-p$  sinusoid. Output voltage is approximately  $4.997Vp-p$ .

Power supply pins should be bypassed with  $0.01\mu F$  ceramic capacitors.

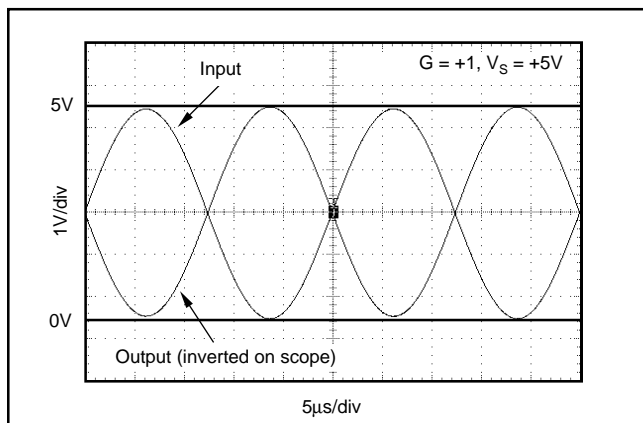


FIGURE 1. Rail-to-Rail Input and Output.

## OPERATING VOLTAGE

OPA344 and OPA345 series op amps are fully specified and ensured from  $+2.7V$  to  $+5.5V$ . In addition, many specifications apply from  $-40^\circ C$  to  $+85^\circ C$ . Parameters that vary significantly with operating voltages or temperature are shown in the Typical Performance Curves.

## RAIL-TO-RAIL INPUT

The input common-mode voltage range of the OPA344 and OPA345 series extends  $300mV$  beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair (see Figure 2). The N-channel pair is active for input voltages close to the positive rail, typically  $(V+) - 1.3V$  to  $300mV$  above the positive supply, while the P-channel pair is on for inputs from  $300mV$  below the negative supply to approximately  $(V+) - 1.3V$ . There is a small transition region, typically  $(V+) - 1.5V$  to  $(V+) - 1.1V$ , in which both pairs are on. This  $400mV$  transition region can vary  $300mV$  with process variation. Thus, the transition region (both stages on) can range from  $(V+) - 1.8V$  to  $(V+) - 1.4V$  on the low end, up to  $(V+) - 1.2V$  to  $(V+) - 0.8V$  on the high end. Within the  $400mV$  transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region. For more information on designing with rail-to-rail input op amps, see Figure 3 “Design Optimization with Rail-to-Rail Input Op Amps.”

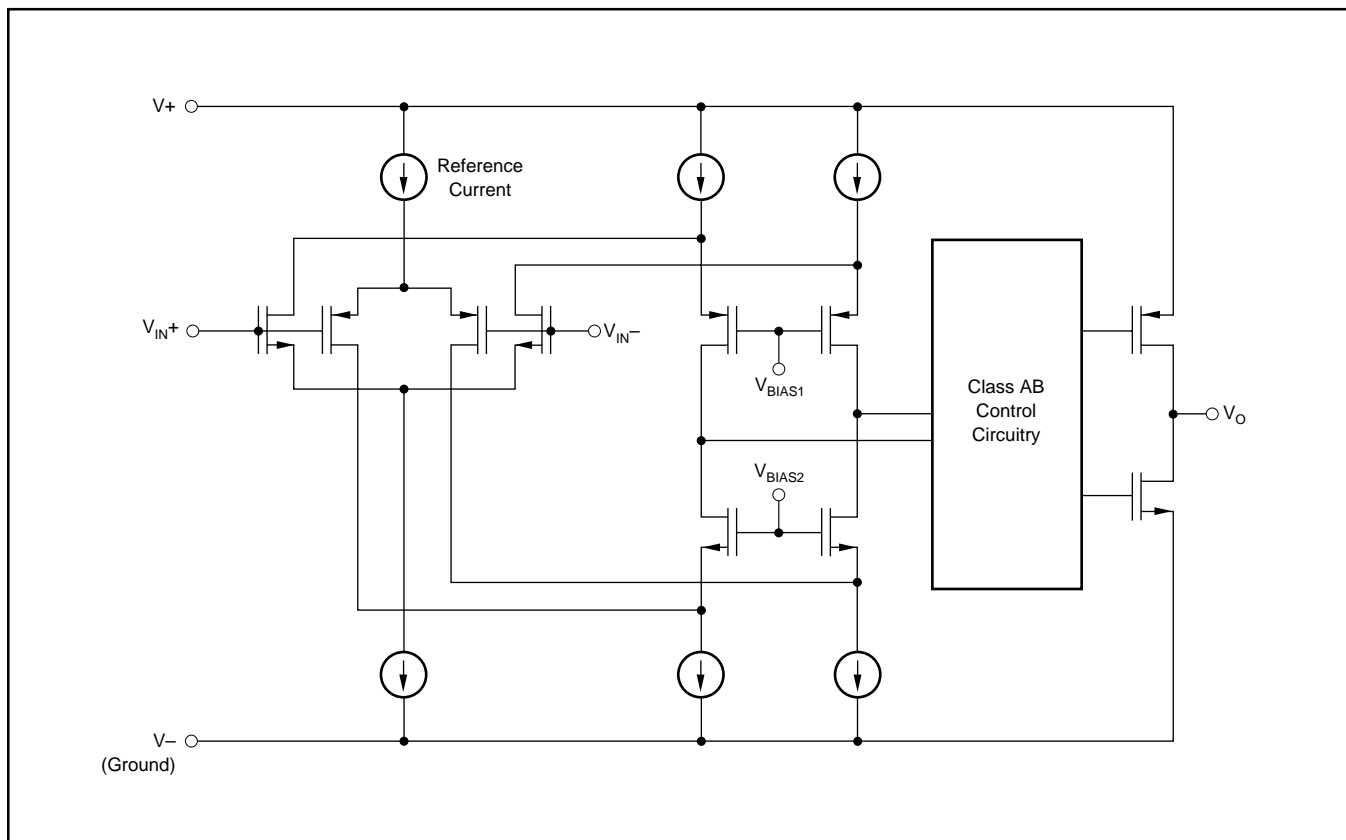


FIGURE 2. Simplified Schematic.

## DESIGN OPTIMIZATION WITH RAIL-TO-RAIL INPUT OP AMPS

Rail-to-rail op amps can be used in virtually any op amp configuration. To achieve optimum performance, however, applications using these special double-input-stage op amps may benefit from consideration of their special behavior.

In many applications, operation remains within the common-mode range of only one differential input pair. However some applications exercise the amplifier through the transition region of both differential input stages. Although the two input stages are laser trimmed for excellent matching, a small discontinuity may occur in this transition. Careful selection of the circuit configuration, signal levels and biasing can often avoid this transition region.

With a unity-gain buffer, for example, signals will traverse this transition at approximately 1.3V below  $V_+$  supply and may exhibit a small discontinuity at this point.

The common-mode voltage of the non-inverting amplifier is equal to the input voltage. If the input signal always remains less than the transition voltage, no discontinuity will be created. The closed-loop gain of this configuration can still produce a rail-to-rail output.

Inverting amplifiers have a constant common-mode voltage equal to  $V_B$ . If this bias voltage is constant, no discontinuity will be created. The bias voltage can generally be chosen to avoid the transition region.

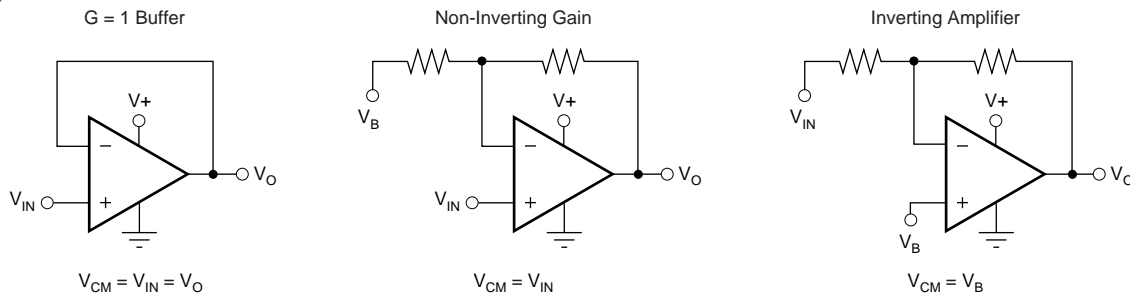


FIGURE 3. Design Optimization with Rail-to-Rail Input Op Amps.

### COMMON-MODE REJECTION

The CMRR for the OPA344 and OPA345 is specified in several ways so the best match for a given application may be used. First, the CMRR of the device in the common-mode range below the transition region ( $V_{CM} < (V_+) - 1.8V$ ) is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR at  $V_S = 5.5V$  over the entire common-mode range is specified. Third, the CMRR at  $V_S = 2.7V$  over the entire common-mode range is provided. These last two values include the variations seen through the transition region.

### INPUT VOLTAGE BEYOND THE RAILS

If the input voltage can go more than 0.3V below the negative power supply rail (single-supply ground), special precautions are required. If the input voltage goes sufficiently negative, the op amp output may lock up in an inoperative state. A Schottky diode clamp circuit will prevent this—see Figure 4. The series resistor prevents excessive current (greater than 10mA) in the Schottky diode and in the internal ESD protection diode, if the input voltage can exceed the positive supply voltage. If the signal source is limited to less than 10mA, the input resistor is not required.

### RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving 600Ω loads connected to any potential

between  $V_+$  and ground. For light resistive loads ( $> 50k\Omega$ ), the output voltage can typically swing to within 1mV from supply rail. With moderate resistive loads ( $2k\Omega$  to  $50k\Omega$ ), the output can swing to within a few tens of millivolts from the supply rails while maintaining high open-loop gain. See the typical performance curve “Output Voltage Swing vs Output Current.”

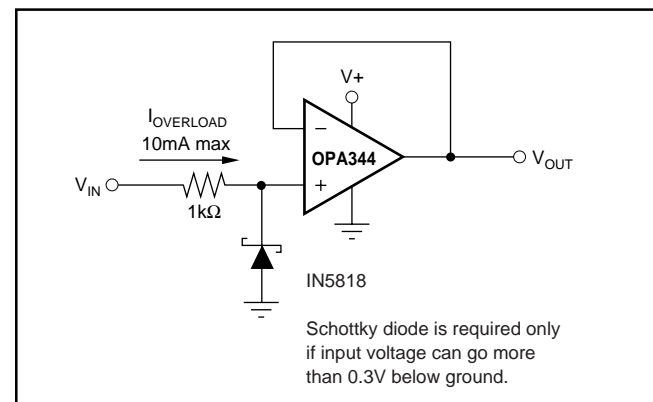


FIGURE 4. Input Current Protection for Voltages Exceeding the Supply Voltage.

### CAPACITIVE LOAD AND STABILITY

The OPA344 in a unity-gain configuration and the OPA345 in gains greater than 5 can directly drive up to 250pF pure capacitive load. Increasing the gain enhances the amplifier's ability to drive greater capacitive loads. See the typical

performance curve “Small-Signal Overshoot vs Capacitive Load.” In unity-gain configurations, capacitive load drive can be improved by inserting a small ( $10\Omega$  to  $20\Omega$ ) resistor,  $R_S$ , in series with the output, as shown in Figure 5. This significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a dc error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio  $R_S/R_L$ , and is generally negligible.

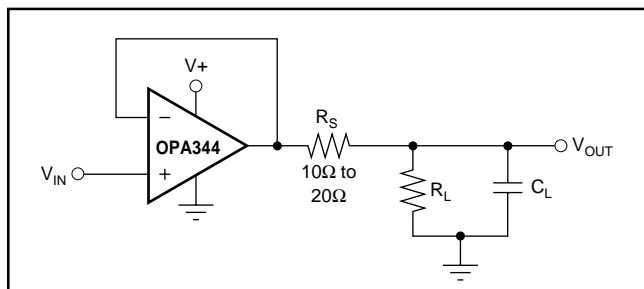


FIGURE 5. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive.

## DRIVING A/D CONVERTERS

The OPA344 and OPA345 series op amps are optimized for driving medium-speed sampling A/D converters. The OPA344 and OPA345 op amps buffer the A/D’s input capacitance and resulting charge injection while providing signal gain.

Figure 6 shows the OPA344 in a basic noninverting configuration driving the ADS7822. The ADS7822 is a 12-bit, micro-power sampling converter in the MSOP-8 package. When used with the low-power, miniature packages of the OPA344, the combination is ideal for space-limited, low-power applications. In this configuration, an RC network at the A/D’s input can be used to filter charge injection.

Figure 7 shows the OPA2344 driving an ADS7822 in a speech bandpass filtered data acquisition system. This small, low-cost solution provides the necessary amplification and signal conditioning to interface directly with an electret microphone. This circuit will operate with  $V_S = +2.7V$  to  $+5V$  with less than  $500\mu A$  quiescent current.

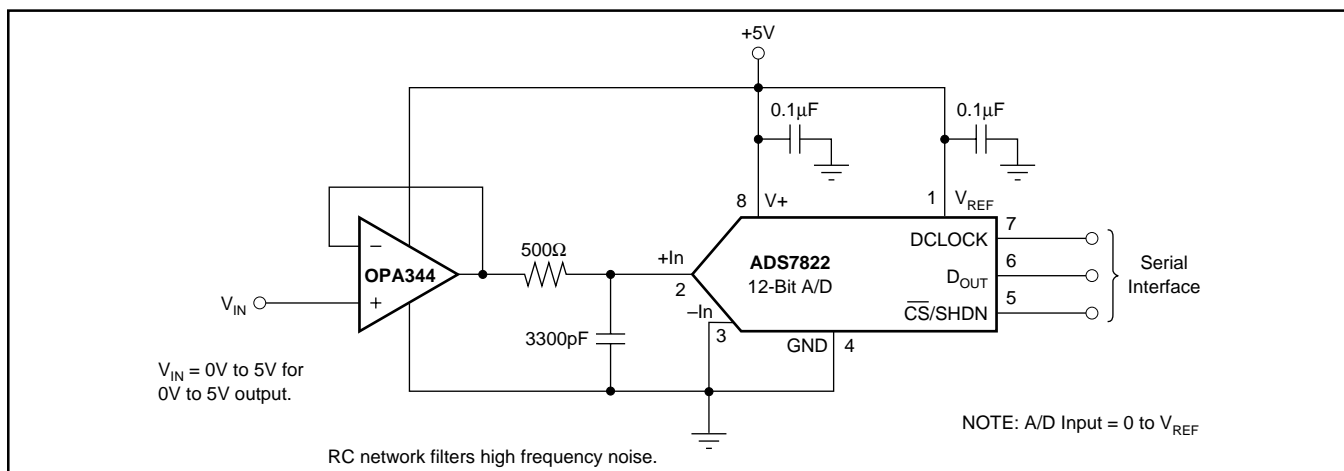


FIGURE 6. OPA344 in Noninverting Configuration Driving ADS7822.

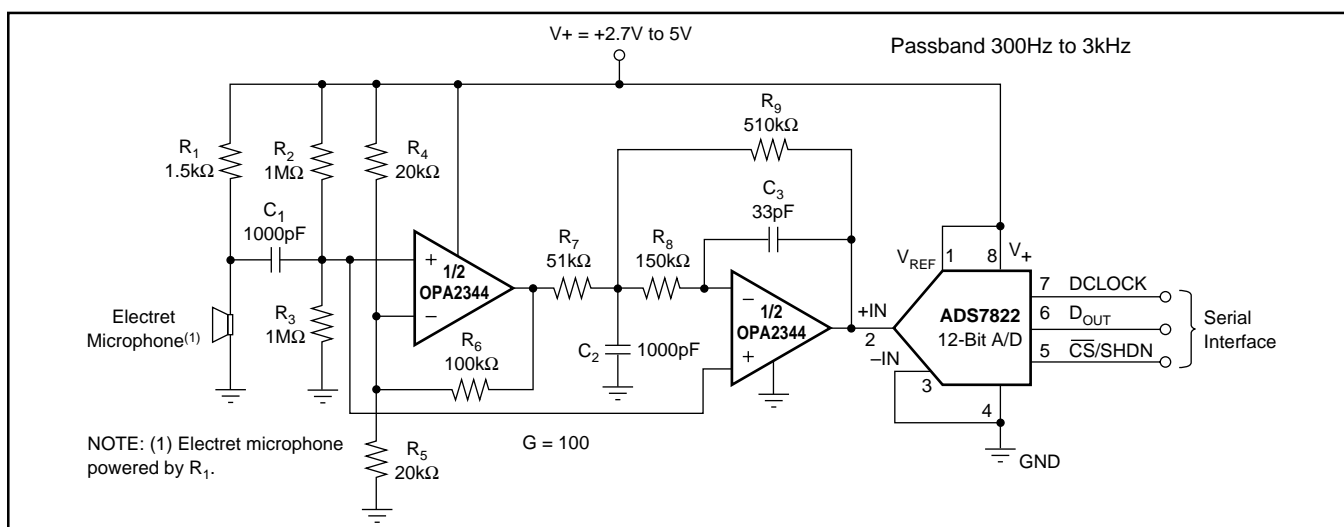


FIGURE 7. Speech Bandpass Filtered Data Acquisition System.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2344EA/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	C44	<a href="#">Samples</a>
OPA2344EA/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	C44	<a href="#">Samples</a>
OPA2344UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2344UA	<a href="#">Samples</a>
OPA2344UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2344UA	<a href="#">Samples</a>
OPA2344UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2344UA	<a href="#">Samples</a>
OPA2345EA/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B45	<a href="#">Samples</a>
OPA2345UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2345UA	<a href="#">Samples</a>
OPA2345UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2345UA	<a href="#">Samples</a>
OPA344NA/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B44	<a href="#">Samples</a>
OPA344NA/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B44	<a href="#">Samples</a>
OPA344NA/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B44	<a href="#">Samples</a>
OPA344NA/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B44	<a href="#">Samples</a>
OPA344PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	OPA344PA	<a href="#">Samples</a>
OPA344UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 344UA	<a href="#">Samples</a>
OPA344UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 344UA	<a href="#">Samples</a>
OPA344UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 344UA	<a href="#">Samples</a>
OPA345NA/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A45	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA345NA/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A45	<a href="#">Samples</a>
OPA345UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 345UA	<a href="#">Samples</a>
OPA4344EA/250	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 4344EA	<a href="#">Samples</a>
OPA4344EA/2K5	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 4344EA	<a href="#">Samples</a>
OPA4344UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4344UA	<a href="#">Samples</a>
OPA4344UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4344UA	<a href="#">Samples</a>
OPA4344UAG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4344UA	<a href="#">Samples</a>
OPA4345UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4345UA	<a href="#">Samples</a>
OPA4345UAG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4345UA	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2344EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2344EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2344UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2345EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2345UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA344NA/250	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA344NA/3K	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA344UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA345NA/250	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA345NA/3K	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA4344EA/250	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4344EA/2K5	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4344UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2344EA/250	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2344EA/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2344UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA2345EA/250	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2345UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA344NA/250	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA344NA/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA344UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA345NA/250	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA345NA/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA4344EA/250	TSSOP	PW	14	250	210.0	185.0	35.0
OPA4344EA/2K5	TSSOP	PW	14	2500	367.0	367.0	35.0
OPA4344UA/2K5	SOIC	D	14	2500	367.0	367.0	38.0



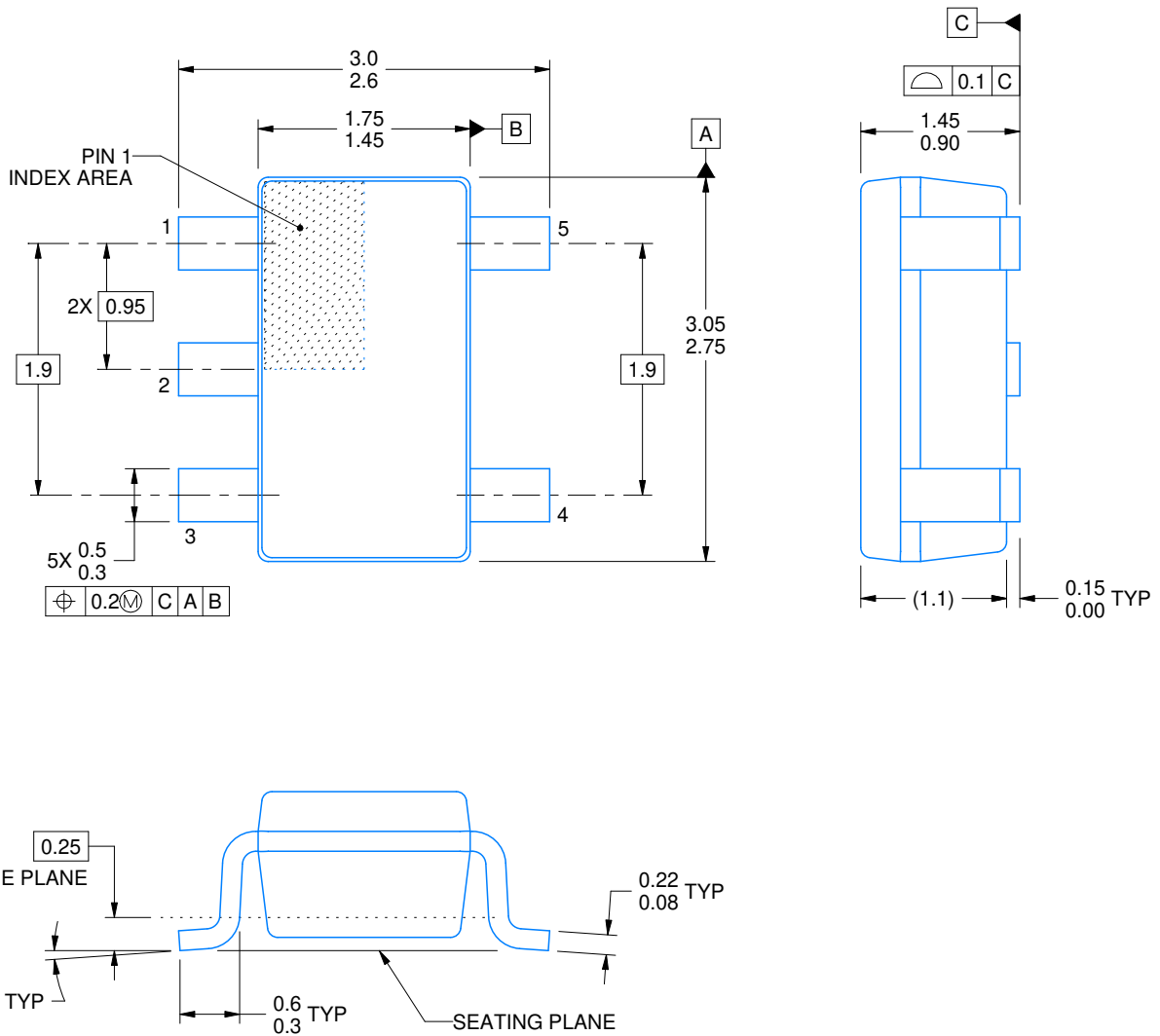
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/E 09/2019

NOTES:

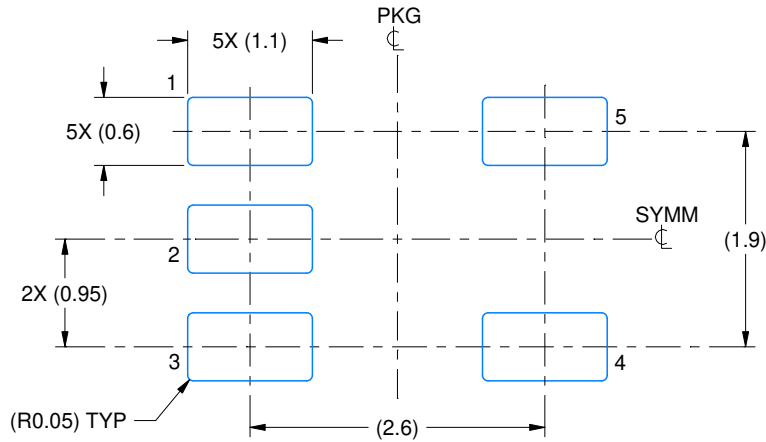
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

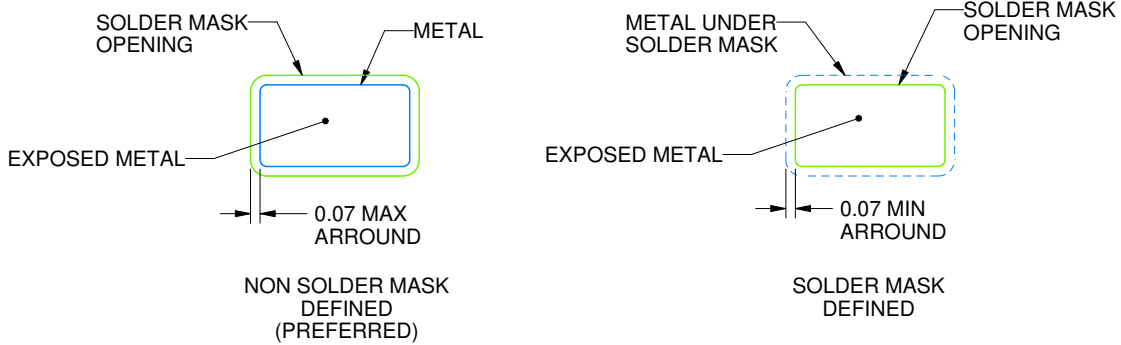
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

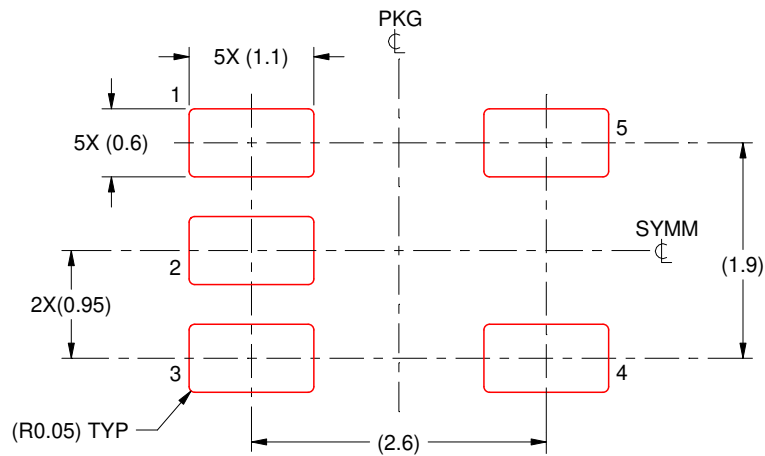
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

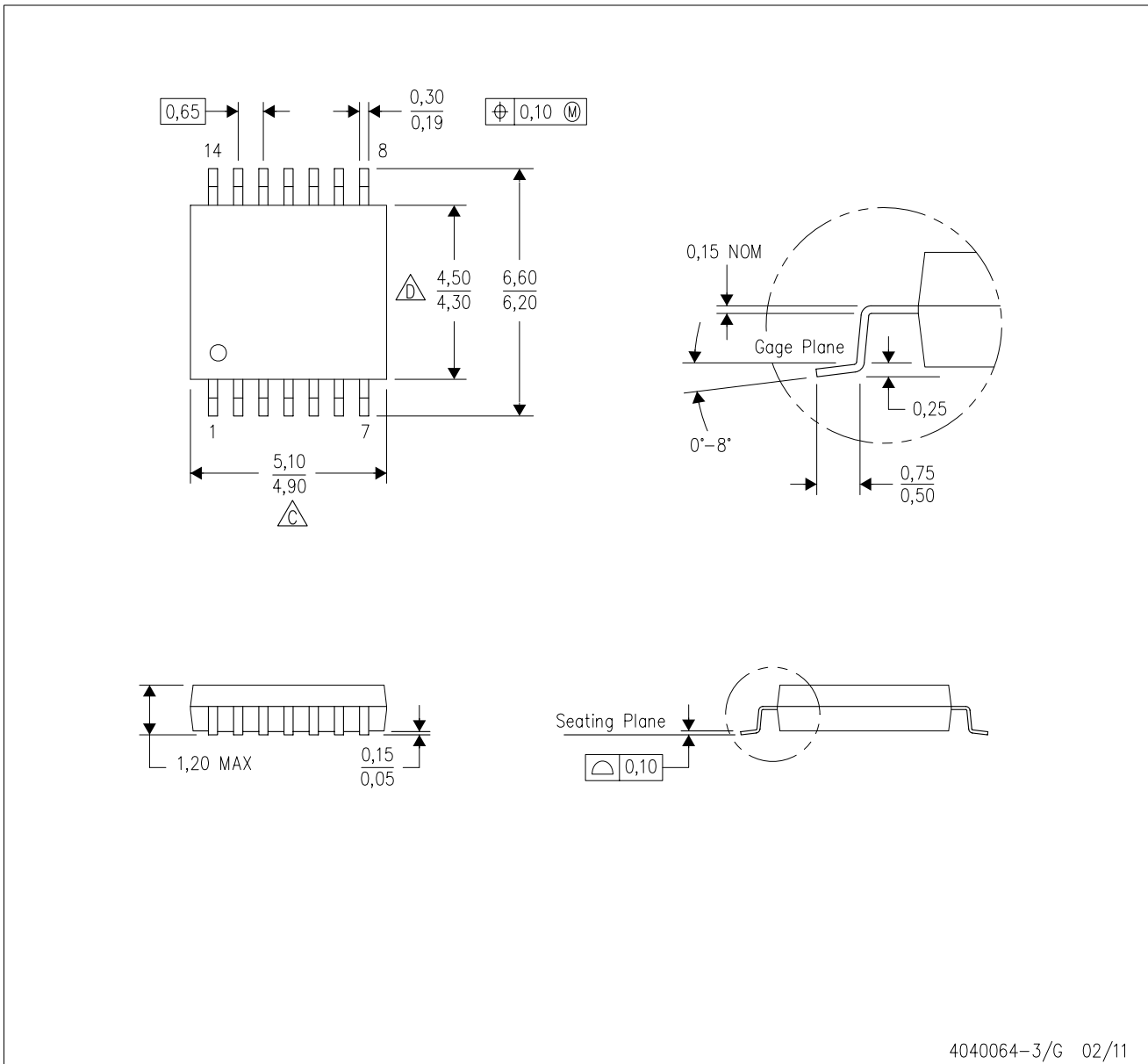
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

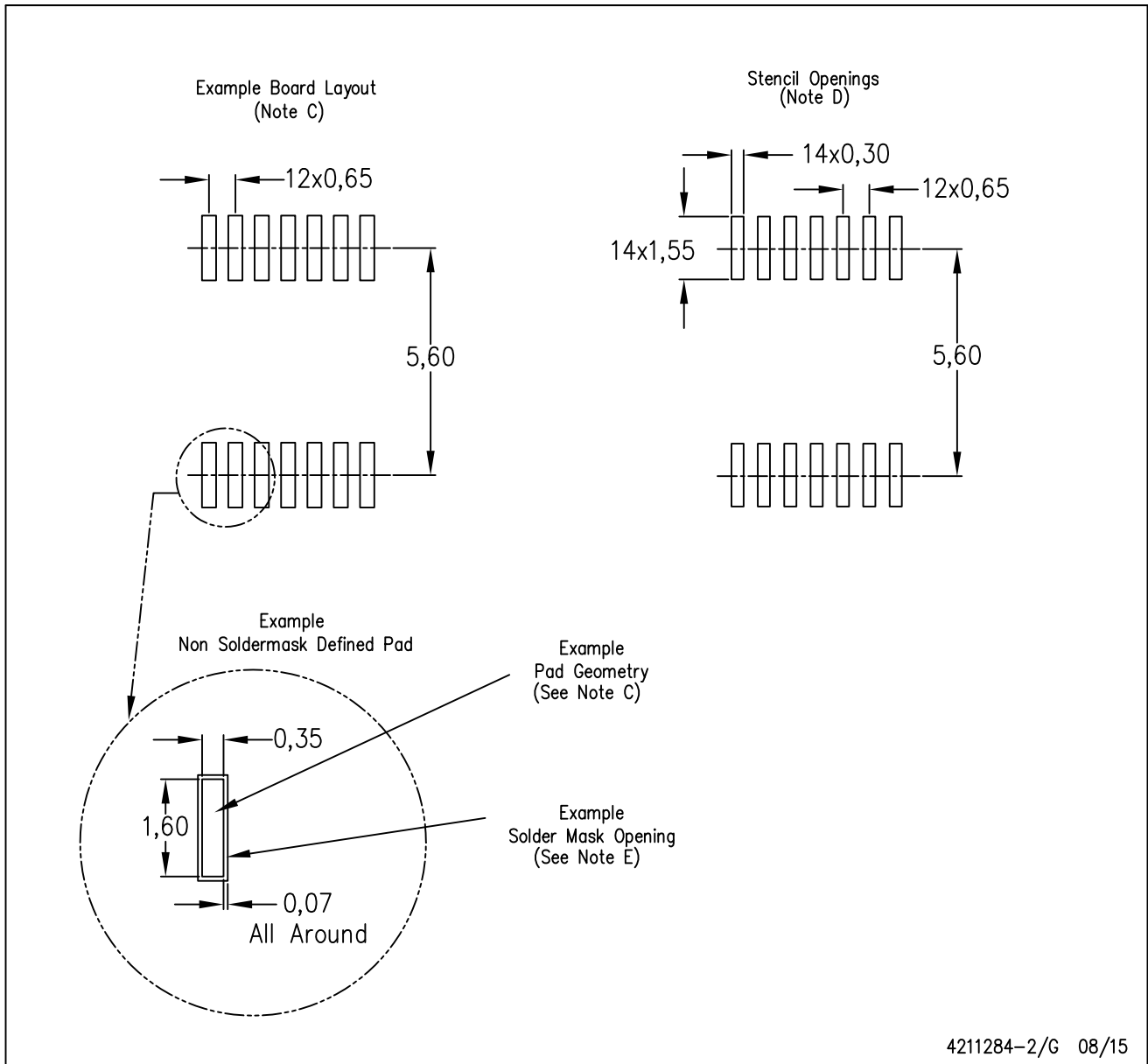
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



# D0008A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



**NOTES:**

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

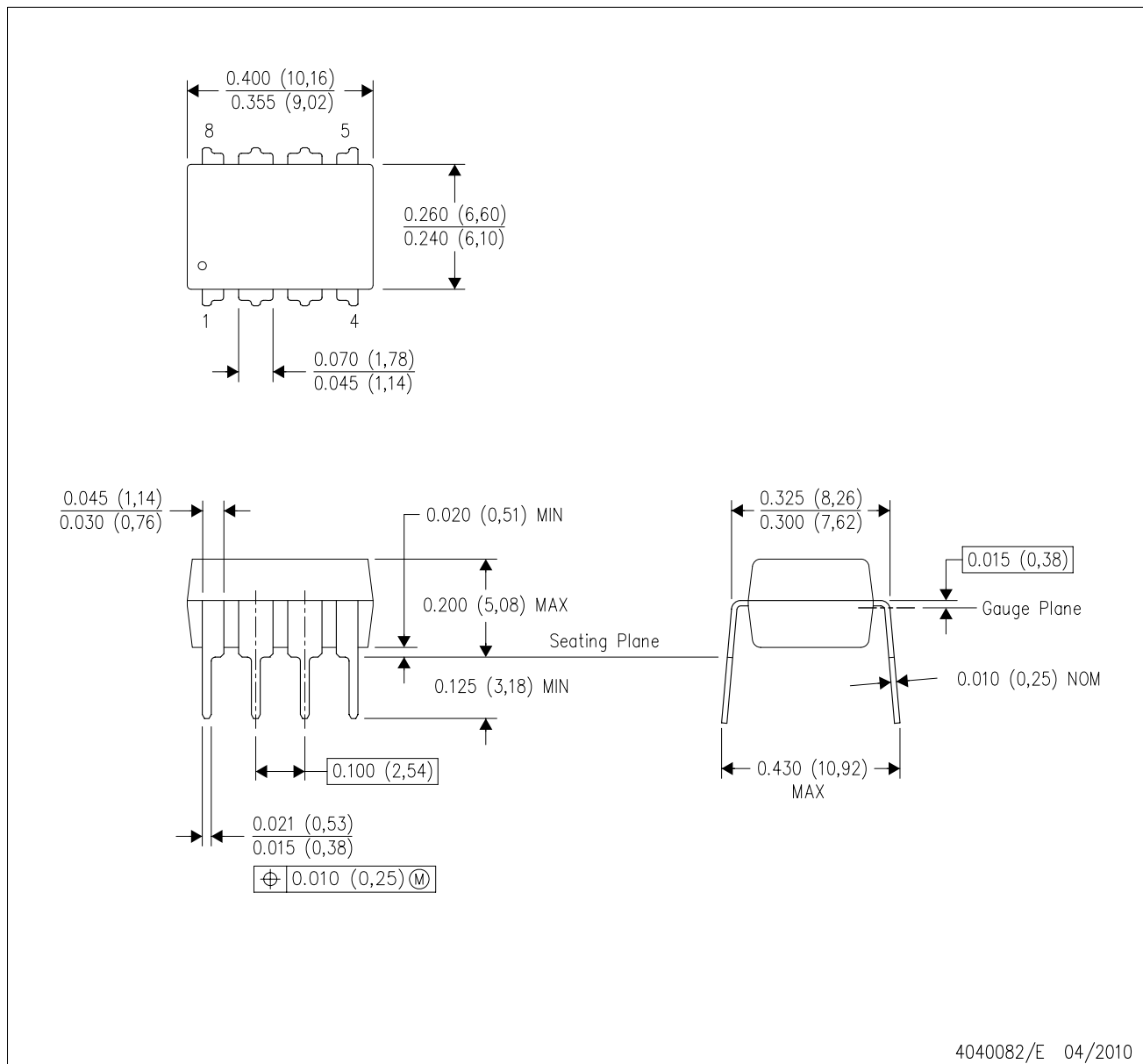
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

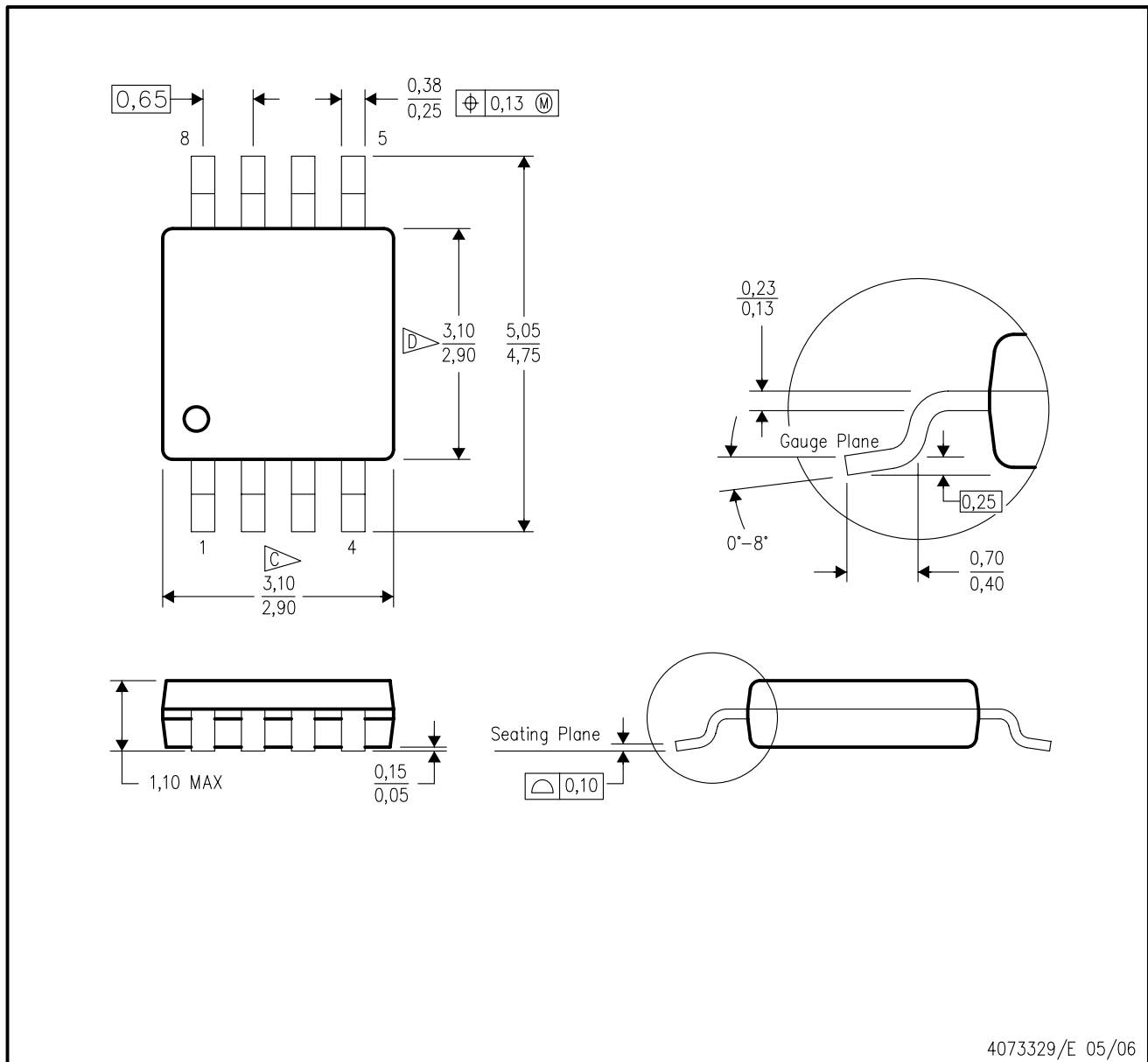
PLASTIC DUAL-IN-LINE PACKAGE



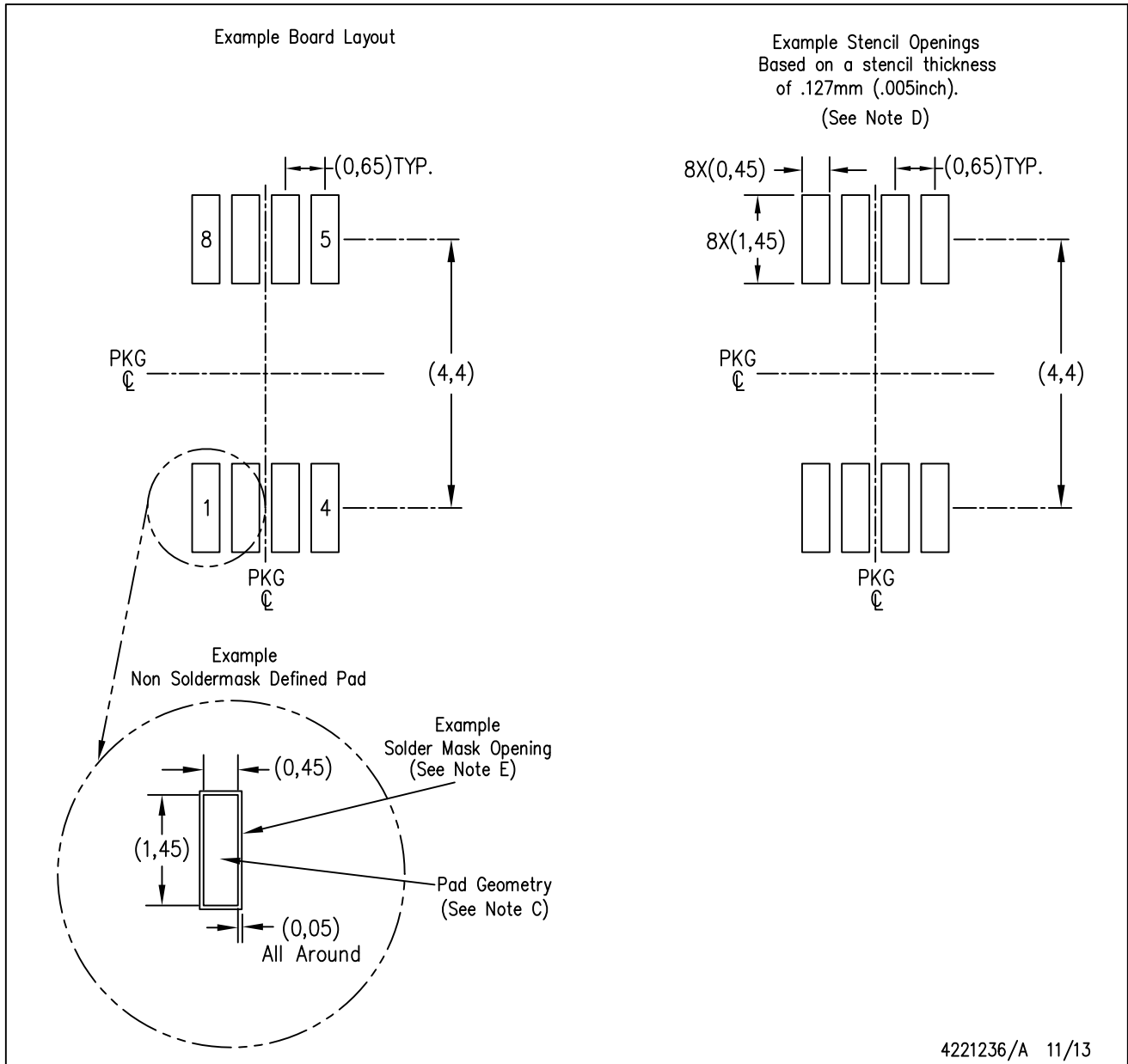
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated