

ISL91211AIK, ISL91211BIK

Triple/Quad Output Power Management IC for Industrial and Computing Applications

The [ISL91211AIK](#) is a 4-phase, three output programmable Power Management IC (PMIC) and the [ISL91211BIK](#) is a 4-phase, four output programmable PMIC. Optimized with highly efficient synchronous buck converters for multiphase and single-phase operations, these converters deliver up to 5A per phase maximum output current. Featuring four buck controllers that can reconfigure their power stages to the controllers, both PMICs offer flexibility and allow seamless, design-in for a wide range of applications that need high output power and a small solution size.

ISL91211AIK and ISL91211BIK integrate low ON-resistance MOSFETs at 2MHz switching frequency, allowing smaller external inductors and capacitors to be used. With automatic Diode Emulation and Pulse Skipping modes under light-load conditions, this feature improves efficiency and maximizes battery life. The ISL91211AIK and ISL91211BIK deliver a highly robust power solution through a controller based on the Renesas proprietary Rapid Robust Ripple Regulator (R5) technology, offering tight output accuracy and load regulation, ultra-fast transient response, seamless DCM/CCM transitions, and no required external compensation.

In addition to the standard interrupt, chip enable, and watchdog reset functions, the ISL91211AIK and ISL91211BIK also feature four MPIOs and three GPIOs that supports SPI, I²C communication protocol, and various other pin mode functions.

Features

- Triple output 2+1+1 phases (ISL91211AIK) or quad output, four single phases (ISL91211BIK)
- 2.7V to 5.5V supply voltage
- 5A per phase peak current capability
- Small solution size (for four phase design)
- High efficiency (92.2%, L = 220nH for 3.8V_{IN}/1.8V_{OUT})
- Low I_Q in low power mode
- Proprietary control scheme reduces output capacitor and supports fast load transient (such as >50A/μs per phase)
- ±0.7% system accuracy, remote voltage sensing
- I²C programmable output from 0.3V to 2V
- Independent Dynamic Voltage Scaling (DVS) for each output
- Soft-start and fault detection (UV, OV, OC, OT), short-circuit protection
- 4.70mmx6.30mm 35 ball BGA with 0.8mm pitch

Applications

- Industrial controls and FPGAs
- Computing servers and systems
- Home gateways and appliances

Related Literature

For a full list of related documents, visit our website:

[ISL91211AIK](#) and [ISL91211BIK](#) device pages

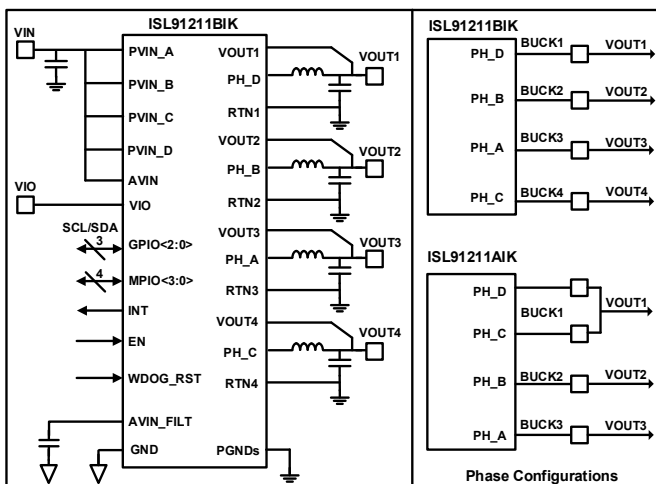


Figure 1. Simplified Block Diagram

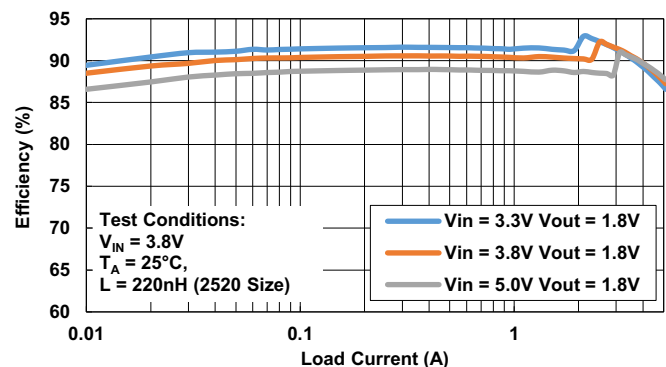


Figure 2. Single-Phase Efficiency vs Load Current

Contents

1. Overview	3
1.1 Typical Application Diagrams	3
1.2 Block Diagram	4
1.3 Ordering Information	5
1.4 Pin Configuration	6
1.5 Pin Descriptions	6
1.6 I/O Pin Configurations	8
2. Specifications	9
2.1 Absolute Maximum Ratings	9
2.2 Thermal Information	9
2.3 Recommended Operation Conditions	9
2.4 Analog Specifications	10
3. Output Configurations	12
4. Typical Operating Performance	14
5. Applications Information	20
5.1 Inductor Selection	20
5.2 Output Capacitor Selection	20
5.3 Input Capacitor Selection	20
5.4 Dynamic Voltage Scaling (DVS)	21
5.5 Configuring DVS Speed	23
5.6 Output Voltage Setting	23
5.7 Power Sequencing	24
5.8 Watchdog Time (WDOG_RST Pin)	25
5.9 Interrupt Pin	26
6. Protection Features (FAULTS)	27
6.1 Over-Temperature Protection	27
6.2 Overcurrent Protection Mode	27
6.3 Overvoltage (OV)/Undervoltage (UV) Protection	27
7. Serial Communication Interface	28
7.1 SPI Interface	28
7.2 I ² C Interface	31
8. Board Layout Recommendations	35
8.1 PCB Layout Summary	36
8.2 PCB Design for TFBGA Recommendations	37
9. Register Address Map	38
10. Register Description by Address	39
11. Revision History	52
12. Package Outline Drawing	53

1. Overview

1.1 Typical Application Diagrams

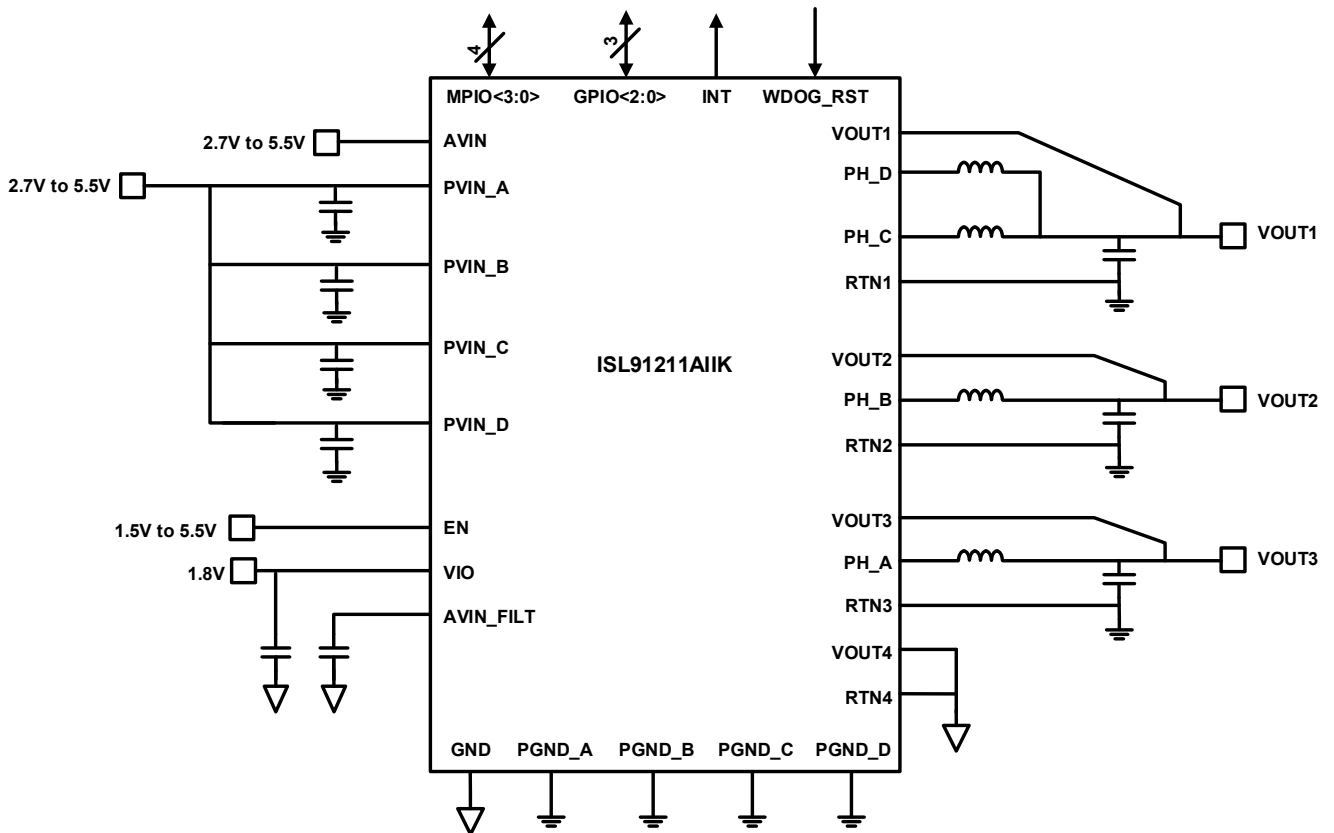


Figure 3. 2 Phase + 1 Phase + 1 Phase

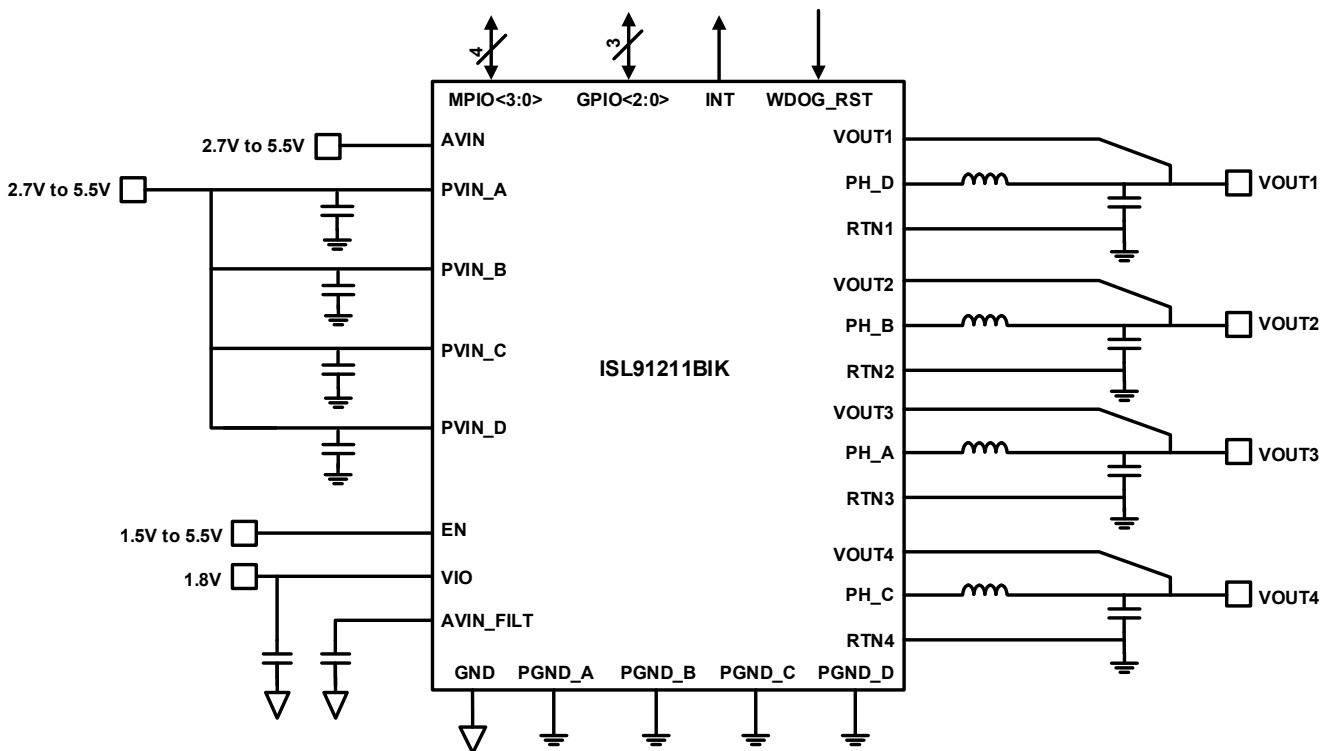


Figure 4. 1 Phase + 1 Phase + 1 Phase + 1 Phase

1.2 Block Diagram

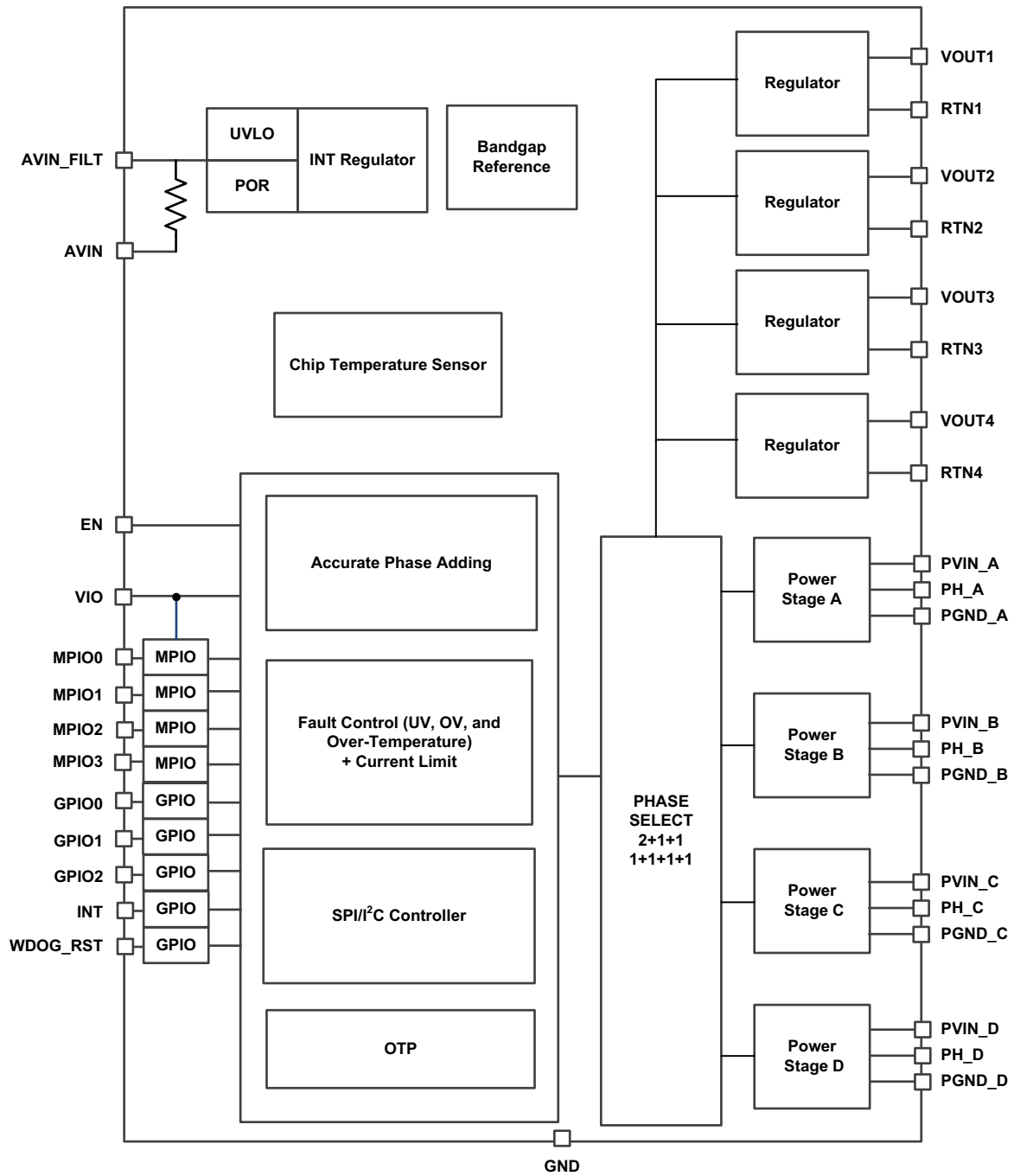


Figure 5. Block Diagram

1.3 Ordering Information

Part Number (Notes 1, 3, 4)	Part Marking	Temp Range (°C)	Tape and Reel (Units) (Note 2)	Package (RoHS Compliant)	Pkg. Dwg #
ISL91211AIKZ-T	211AK	-40 to +85	3k	4.70mmx6.30mm, 35 Ball TFBGA	V35.4.7x6.3
ISL91211BIKZ-T	211BK	-40 to +85	3k	4.70mmx6.30mm, 35 Ball TFBGA	V35.4.7x6.3
ISL91211AIK-EV1Z	Evaluation board				
ISL91211BIK-EV1Z	Evaluation board				

Notes:

- For additional part options contact your local sales office.
- See [TB347](#) for details about reel specifications.
- These Pb-free TFBGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu -e6 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free TFBGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
- For Moisture Sensitivity Level (MSL), see the [ISL91211AIK](#) and [ISL91211BIK](#) product information page. For more information about MSL, see [TB363](#).

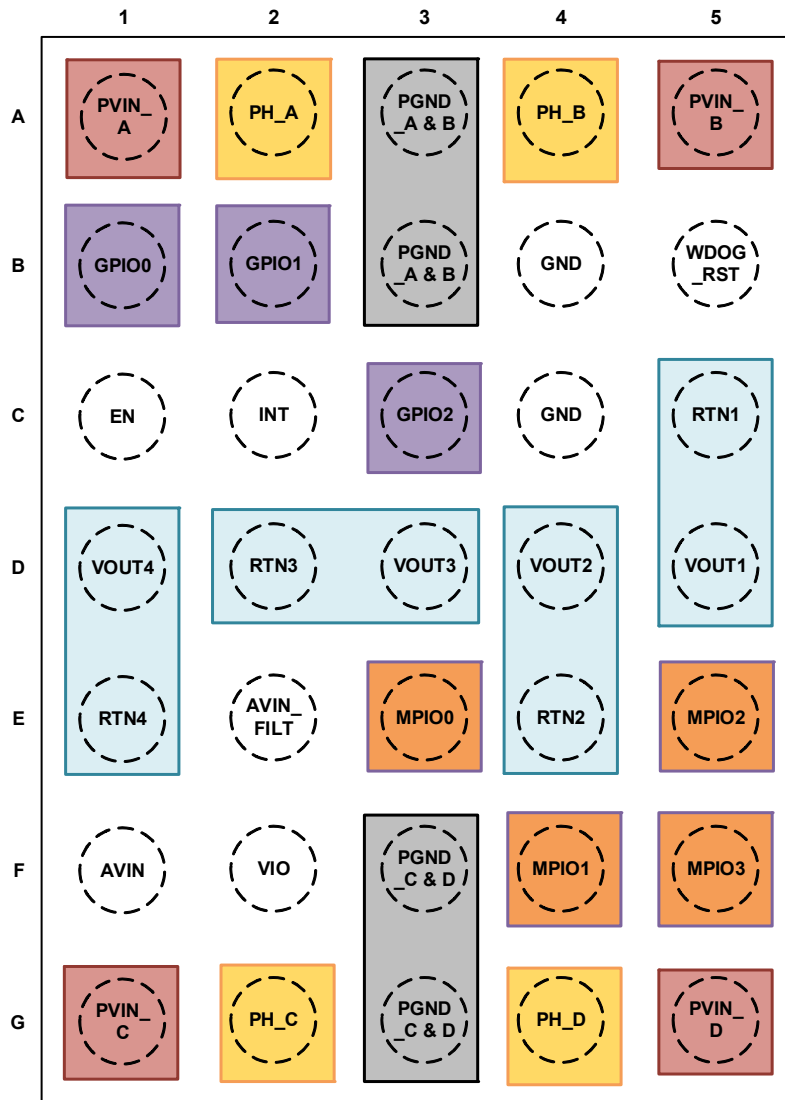
Table 1. Key Differences Between Family of Parts

Part Number	Pin Configuration	Pitch	Output Configuration	Max Load Per Phase
ISL91211AIK	35 Ball 5x7 TFBGA	0.8mm	Triple Output (2+1+1 Phase)	5A
ISL91211BIK	35 Ball 5x7 TFBGA	0.8mm	Quad Output (1+1+1+1 Phase)	5A
ISL91302BIK	35 Ball 5x7 TFBGA	0.8mm	Single Output (4+0 Phase)	5A
	35 Ball 5x7 TFBGA	0.8mm	Dual Output (3+1 Phase)	5A
	35 Ball 5x7 TFBGA	0.8mm	Dual Output (2+2 Phase)	5A

1.4 Pin Configuration

35 Ball 5x7 TFBGA
Top View

JEDEC Standard:
Balls Down, A1 Top Left Corner



1.5 Pin Descriptions

Pin Location	Pin Name	Type	Description
A1	PVIN_A	Input	Power supply for Power Stage A.
A2	PH_A	Output	Switching node for Power Stage A.
A3	PGND_AB	Input	Ground connection for Power Stage A and B.
B3	PGND_AB	Input	Ground connection for Power Stage A and B.
A4	PH_B	Output	Switching node for Power Stage B.
A5	PVIN_B	Input	Power supply for Power Stage B.
B1	GPIO0	Input	GPIO0. See Table 2 . This pin is the I ² C clock for pin modes 0x0, 0x2, and 0x4 through 0x7 and 0xC.
B2	GPIO1	Input/Output	GPIO1. See Table 2 . This pin is the I ² C data for pin modes 0x0, 0x2, and 0x4 through 0x7 and 0xC.

Pin Location	Pin Name	Type	Description
B5	WDOG_RST	Input	Digital input, resets bucks to default output voltage.
C1	EN	Input	Master chip enable input, NMOS logic threshold.
C2	INT	Output	Interrupt line.
C3	GPIO2	Input	GPIO2. See Table 2 .
B4, C4	GND	Input	Analog chip ground.
C5	RTN1	Input	Remote ground sense for Buck1.
D1	VOUT4	Input	Buck4 output voltage sense for the ISL91211BIK. Note: Short to ground for the ISL91211AIK.
D2	RTN3	Input	Remote ground sense for Buck3.
D3	VOUT3	Input	Output voltage sense for Buck3.
D4	VOUT2	Output	Output voltage sense for Buck2.
E4	RTN2	Input	Remote ground sense for Buck2.
D5	VOUT1	Input	Remote output voltage sense for Buck1.
E1	RTN4	Input	Buck4 output voltage sense for the ISL91211BIK. Note: Short to ground for the ISL91211AIK.
E2	AVIN_FILT	Output	Filtered analog supply voltage, 2.5V to 5.5V. Place a decoupling capacitor close to the IC.
F2	VIO	Input	I/O supply voltage for digital communications. Nominally connected to 1.8V supply.
E3	MPIO0	Input/Output	Multipurpose I/O, see Table 2 . Can be NC if not used.
F4	MPIO1	Input/Output	Multipurpose I/O, see Table 2 . Can be NC if not used. Must be pulled up to VIO if using I ² C.
E5	MPIO2	Input/Output	Multipurpose I/O, see Table 2 . Can be NC if not used.
F1	AVIN	Input	Analog supply voltage, 2.5V to 5.5V.
G2	PH_C	Output	Switching node for Power Stage C.
F3	PGND_CD	Input	Ground connection for Power Stage C and D.
G3	PGND_CD	Input	Ground connection for Power Stage C and D.
G5	PH_D	Output	Output switching node for Power Stage D.
F5	MPIO3	Input/Output	Multipurpose I/O, see Table 2 . Can be NC if not used.
G1	PVIN_C	Input	Power supply connection for Power Stage C.
G5	PVIN_D	Input	Power supply connection for Power Stage D.

1.6 I/O Pin Configurations

The ISL91211AIK and ISL91211BIK feature three general-purpose I/O (GPIO) pins for I²C and other functions, along with four multi-purpose I/O (MIO) pins. These pins perform different functions depending on the IO_PINMODE setting. The default factory setting for IO_PINMODE is 0x0. For features requiring IO_PINMODE to be different than the default value, contact Renesas [support](#) for factory OTP programming.

Table 2. I/O Pin Mode

IO_PINMODE	MPIO0	MPIO1	MPIO2	MPIO3	GPIO0	GPIO1	GPIO2	Description
0x0	SCK	SS_B	MOSI	MISO	I2C_CLK	I2C_SDA	N/A	I ² C/SPI both available
0x1	SCK	SS_B	MOSI	MISO	EN_A	EN_B	EN_C	SPI mode with hardware enables for BUCKs 1-4
0x2	PGOOD1	PGOOD2	PGOOD3	PGOOD4	I2C_CLK	I2C_SDA	N/A	I ² C with individual PGOODs for BUCKs 1-4
0x3	SCK	SS_B	MOSI	MISO	DVS_A	DVS_B	DVS_C	SPI with hardware DVS pins
0x4	DVS_PIN1	DVS_PIN0	PGOOD1	PGOOD2	I2C_CLK	I2C_SDA	N/A	I ² C with Global DVS mode with PGOOD1 and PGOOD2
0x5	BUCK1_DVS0	BUCK1_DVS1	BUCK2_DVS0	BUCK2_DVS1	I2C_CLK	I2C_SDA	N/A	I ² C with full pin controlled DVS for Buck1 and Buck2
0x6	BUCK1_DVS0	BUCK1_DVS1	BUCK2_DVS0	BUCK3_DVS0	I2C_CLK	I2C_SDA	N/A	I ² C with full DVS for Buck 1, 1-pin DVS for Buck2 and Buck3
0x7	BUCK1_DVS0	BUCK2_DVS0	BUCK3_DVS0	BUCK4_DVS0	I2C_CLK	I2C_SDA	N/A	I ² C with 1-pin DVS for each buck
0xC	MPIO_DATA [0]	MPIO_DATA [1]	MPIO_DATA [2]	MPIO_DATA [3]	I2C_CLK	I2C_SDA	N/A	I ² C with four parallel controllable data lines.

Note:

5. Pin modes 0x8 through 0xB and 0xD through 0xF are reserved.

Table 3. Pin Mode Descriptions

Name	Definition
SCK	SPI clock
SS_B	SPI/I ² C selector. Low = SPI, High = I ² C
MOSI	SPI master out, slave in
MISO	SPI master in, slave out
I2C_CLK	I ² C clock
I2C_SDA	I ² C data
PGOOD1, PGOOD2, PGOOD3, PGOOD4	Four power-good out pins (one per buck)
EN_A, EN_B, EN_C	Three buck enable input pins. A single buck enable pin can enable/disable up to four bucks. Enable/disable on a buck can be controlled from one enable pin (EN_A, EN_B, or EN_C)
DVS_A, DVS_B, DVS_C	Three DVS input pins. A single DVS pin can control the DVS voltage for up to four bucks. DVS voltage on a buck can be controlled from one DVS pin (DVS_A, DVS_B, or DVS_C).
DVS_PIN1, DVS_PIN0	DVS look-up table allows two pins to control up to four bucks.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
PVIN and AVIN Pins to PGND	-0.3	+6	V
VOUT Pin (BUCKx_VOUTFBDIV[1:0] = 0x00)	-0.3	+2.0	V
VOUT Pin (BUCKx_VOUTFBDIV[1:0] = 0x01)	-0.3	+2.4	V
VOUT Pin (BUCKx_VOUTFBDIV[1:0] = 0x02)	-0.3	+3.0	V
PH to PGND	-0.3	+0.3 + PVIN	V
VIO, EN Pins to GND	-0.3	+0.3 + AVIN	V
RTN, GND to PGND	-0.3	+0.3	V
INT, WDOG_RST, MPIO, GPIO Pins to GND	-0.3	+0.3 + VIO	V
ESD Rating (Note 6)	Value		Unit
Human Body Model (Tested per JS-001-2017)	2		kV
Charged Device Model (Tested per JS-002-2014)	750		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Note:

6. ESD ratings apply to external pins only.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
4.70mmx6.30mm, 35 Ball TFBGA Package (Notes 7, 8)	47	3

Notes:

7. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See [TB379](#).
8. For θ_{JC} , the case temperature location is taken at the package top center.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Junction Temperature	-40	+125	°C
Supply Voltage			
AVIN to GND	2.7	5.5	V
PVIN to PGNDx	2.7	5.5	V
VIO Voltage (VIO to PGND)	1.7	AVIN	V
INT, WDOG_RST, MPIO, GPIO Pins to GND	0	VIO	V

2.4 Analog Specifications

AVIN/PVIN = 3.7V, V_{OUT} = 1V, L = 220nH, Frequency = 2MHz, V_{IO} = 1.8V. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

Parameter	Symbol	Test Conditions	Min (Note 9)	Typ	Max (Note 9)	Unit	
Input Supply							
Supply Voltage	AVIN		2.7		5.5	V	
Supply Voltage	PVIN		2.7		5.5	V	
AVIN Supply Current	I _Q	EN = 0V		0.1	1	μA	
AVIN + PVINx Supply Current		EN = 0V		<1	6	μA	
AVIN + PVINx Supply Current EN = AVIN = PVINx = 3.7V		All Buck EN[0] = 0x0			17		μA
		BUCK1_EN[0] = 0x1, all other BUCK EN[0] = 0x0, not switching DCM operation			82		μA
		BUCK2, 3 or 4_EN[0] = 0x1, all other BUCK EN[0] = 0x0, not switching DCM operation			62		μA
		BUCK1_EN[0] = 0x1, all other BUCK EN[0] = 0x0, not switching, forced CCM operation			1.2		mA
	BUCK2, 3 or 4_EN[0] = 0x1, all other BUCK EN[0] = 0x0, not switching, forced CCM operation			1		mA	
AVIN UVLO Rising Threshold	VUVLOR		2.50	2.58	2.65	V	
AVIN UVLO Falling Threshold	VUVLOF		2.28	2.34	2.39	V	
Buck Regulation							
Buck Output Voltage Range (Each Output)	V _{OUT}	BUCKx_VOUTFBDIV[1:0] = 0x00	0.3		1.2	V	
		BUCKx_VOUTFBDIV[1:0] = 0x01	0.375		1.5	V	
		BUCKx_VOUTFBDIV[1:0] = 0x02	0.500		2.0	V	
Output Voltage Step Size	V _{STEP}	10-bit control, BUCKx_VOUTFBDIV[1:0] = 0x00		1.2		mV	
		10-bit control, BUCKx_VOUTFBDIV[1:0] = 0x01		1.5		mV	
		10-bit control, BUCKx_VOUTFBDIV[1:0] = 0x02		2.0		mV	
Output Voltage Accuracy (Note 10)	V _{ACC}	CCM, V _{OUT} > 0.6V	-0.3		0.3	%	
		CCM, V _{OUT} > 0.6V T _A = -10°C to +85°C	-0.7		0.7	%	
		CCM, V _{OUT} < 0.6V	-4		4	mV	
		CCM, V _{OUT} < 0.6V T _A = -10°C to +85°C	-5.5		5.5	mV	
Current Matching	I _{MATCH}	I _{OUT} = 5A per phase in ISL91211AIK		10		%	
Dynamic Response							
Boot-Up Time	V _{BT}	Delay time from when PVIN, AVIN, and EN assert to Buck1 PWM switching. This time includes the internal reference startup, OTP load, and the Buck controller calibration time		1.4		ms	
Dynamic Voltage Scaling (Output Slew Rate)	V _{DVS}	2.7V < V _{IN} < 5.5V 3mV/μs	-15		15	%	

AVIN/PVIN = 3.7V, V_{OUT} = 1V, L = 220nH, Frequency = 2MHz, V_{IO} = 1.8V. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 9)	Typ	Max (Note 9)	Unit
Frequency						
Switching Frequency (CCM)	f _{sw}			2		MHz
CCM Frequency Tolerance	f _{sw_TOL}		-15		15	%
Power Stage						
Buck Output Current (Each Phase)		2.7V < V _{IN} < 5.5V			5	A
High-Side Switch ON-Resistance	HS r _{DS(ON)}			32		mΩ
Low-Side Switch ON-Resistance	LS r _{DS(ON)}			17.5		mΩ
MPIO/GPIO						
MPIO/GPIO Operating Conditions						
Allowable Range of Supply for Operation	V _{IO}		1.7	1.8	AVIN	V
Chip Enable Logic Threshold Level						
Low-Level Input Voltage Range	V _{IL}				0.5	V
High-Level Input Voltage	V _{IH}		1.35			V
MPIO/GPIO Logic Threshold Levels						
Low-Level Input Voltage Range	V _{IL}				0.25 * V_{IO}	V
High-Level Input Voltage	V _{IH}		0.75 * V_{IO}			V
Hysteresis On Input	V _{HYS}		0.1 * V_{IO}			V
Low-Level Output	V _{OL}	1mA			0.4	V
High-Level Output	V _{OH}	1mA (250μA for 20% drive configuration)	V_{IO} - 0.4			V
Serial Interfaces						
I ² C Frequency Capability	f _{I2C}				3.4	MHz
SPI Frequency Capability	f _{SPI}			26		MHz
Protection						
HSD Current Limit	I _{LIMIT}	2.7V < V _{IN} < 5.5V ISL91211AIK Phase D, OC = 12A	-10		10	%
		2.7V < V _{IN} < 5.5V ISL91211AIK Phase A, B, OC = 8A	-10		10	%
		2.7V < V _{IN} < 5.5V ISL91211BIK Phase A, B, C, D, OC = 8A	-10		10	%
Output UVP Threshold Accuracy	V _{UVP}	Thresholds: -250mV	-35		40	mV
Output OVP Threshold Accuracy	V _{OVP}	Thresholds: +250mV	-35		35	mV
Thermal Shutdown Threshold	T _{SPS}	2.7V < V _{IN} < 5.5V	143		162	°C
		Hysteresis		55		°C

Notes:

- Parameters with MIN and/or MAX limits established by test, characterization, and/or design.
- V_{OUT} feedback divider ratio equals 1 (BUCKx_VOUTFBDIV[1:0] = 0x00).

3. Output Configurations

Table 4. Output Configurations

Output Configuration	Power Stage Assignment	Diagram
2-phase + 1-phase + 1-phase Connect: VOUT4/RTN4 to PGND Plane	2-phase: Controller #1 (VOUT1) • Ph1: PH_D • Ph2: PH_C 1-phase: Controller #2 (VOUT2) • Ph1: PH_B 1-phase: Controller #3 (VOUT3) • Ph1: PH_A	<p style="text-align: center;">ISL91211AIK Configuration</p>

Table 4. Output Configurations (Continued)

Output Configuration	Power Stage Assignment	Diagram
1-phase + 1-phase + 1-phase + 1-phase	1-phase: Controller #1 (VOUT1) • Ph1: PH_D 1-phase: Controller #2 (VOUT2) • Ph1: PH_B 1-phase: Controller #3 (VOUT3) • Ph1: PH_A 1-phase: Controller #4 (VOUT4) • Ph1: PH_C	<p style="text-align: center;">ISL91211BIK Configuration</p> <p>The diagram shows a 7x5 grid of pins for the ISL91211BIK. The pins are: Row 1: PVIN_A, PH_A, PGND_AB, PH_B, PVIN_B; Row 2: GPIO0, GPIO1, PGND_AB, GND, WDOG_RST; Row 3: EN, INT, GPIO2, GND, RTN1; Row 4: VOUT4, RTN3, VOUT3, VOUT2, VOUT1; Row 5: RTN4, AVIN_FILT, MPIO0, RTN2, MPIO2; Row 6: AVIN, VIO, PGND_CD, MPIO1, MPIO3; Row 7: PVIN_C, PH_C, PGND_CD, PH_D, PVIN_D.</p> <p>Four output stages are shown with external components:</p> <ul style="list-style-type: none"> Green Stage (VOUT3): Inductor labeled VOUT3, capacitor labeled PH1, and return pin RTN3. Red Stage (VOUT2): Inductor labeled VOUT2, capacitor labeled PH1, and return pin RTN2. Purple Stage (VOUT4): Inductor labeled VOUT4, capacitor labeled PH1, and return pin RTN4. Blue Stage (VOUT1): Inductor labeled VOUT1, capacitor labeled PH1, and return pin RTN1. <p>Internal connections from the chip pins to these external components are shown with colored lines: green for VOUT3, red for VOUT2, purple for VOUT4, and blue for VOUT1.</p>

4. Typical Operating Performance

Unless otherwise noted, operating conditions are: $V_{IN} = 3.8V$, $V_{OUT} = 1V$, V_{IO} and Enable = 1.8V, $T_A = +25^\circ C$, $f_{SW} = 2MHz$, 2+1+1 configuration, L = 220nH per phase, SW1: $C_{OUT} = 2x22\mu F + 2x4.3\mu F + 4x1\mu F$, SW2-3: $C_{OUT} = 1x22\mu F + 4x4.3\mu F$.

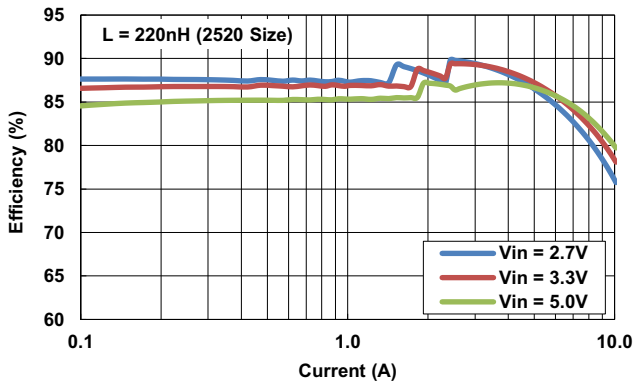


Figure 6. Dual-Phase Efficiency ($V_{OUT} = 0.9V$), Continuous Load Sweep (0.1A to 10A)

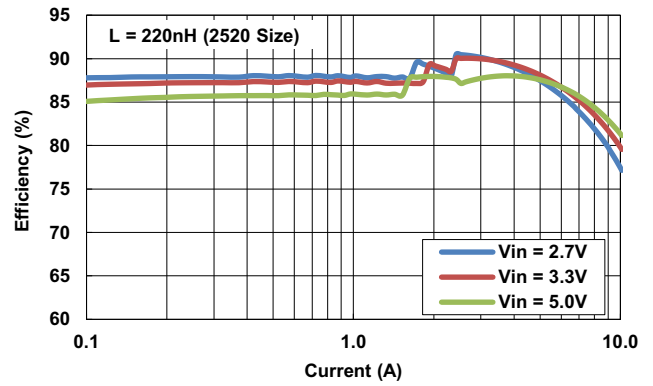


Figure 7. Dual-Phase Efficiency ($V_{OUT} = 1V$), Continuous Load Sweep (0.1A to 10A)

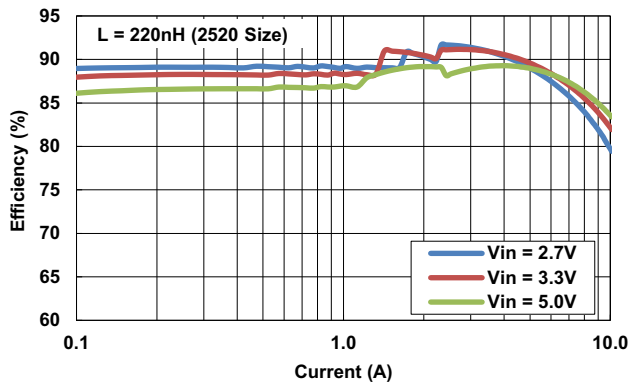


Figure 8. Dual-Phase Efficiency ($V_{OUT} = 1.2V$), Continuous Load Sweep (0.1A to 10A)

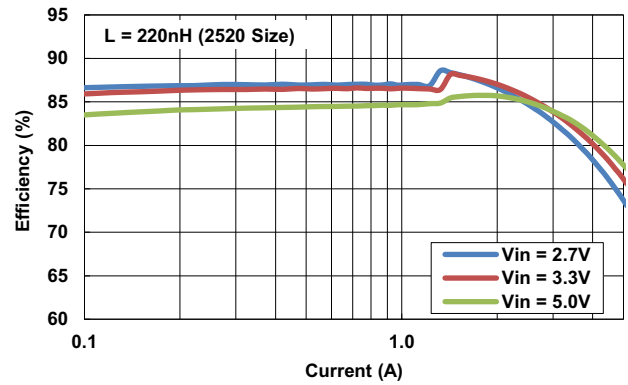


Figure 9. Single-Phase Efficiency ($V_{OUT} = 0.8V$), Continuous Load Sweep (0.1A to 5A)

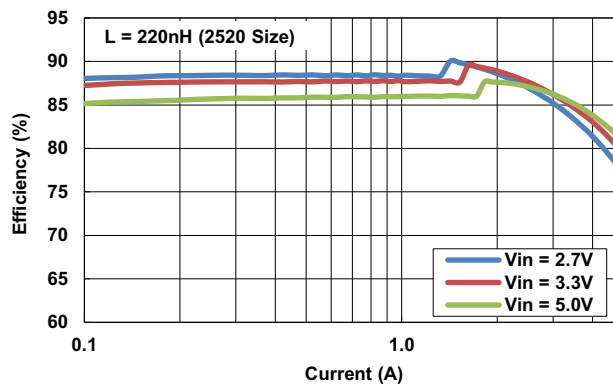


Figure 10. Single-Phase Efficiency ($V_{OUT} = 1V$), Continuous Load Sweep (0.1A to 5A)

Unless otherwise noted, operating conditions are: $V_{IN} = 3.8V$, $V_{OUT} = 1V$, V_{IO} and Enable = 1.8V, $T_A = +25^\circ C$, $f_{SW} = 2MHz$, 2+1+1 configuration, $L = 220nH$ per phase, SW1: $C_{OUT} = 2 \times 22\mu F + 2 \times 4.3\mu F + 4 \times 1\mu F$, SW2-3: $C_{OUT} = 1 \times 22\mu F + 4 \times 4.3\mu F$. (Continued)

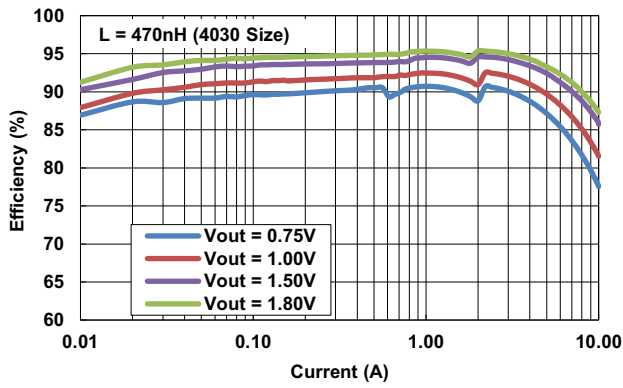


Figure 11. 2-Phase Efficiency $V_{IN} = 3.3V$

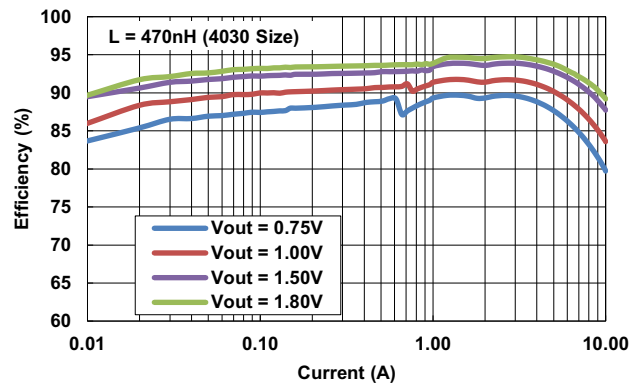


Figure 12. 2-Phase Efficiency $V_{IN} = 3.8V$

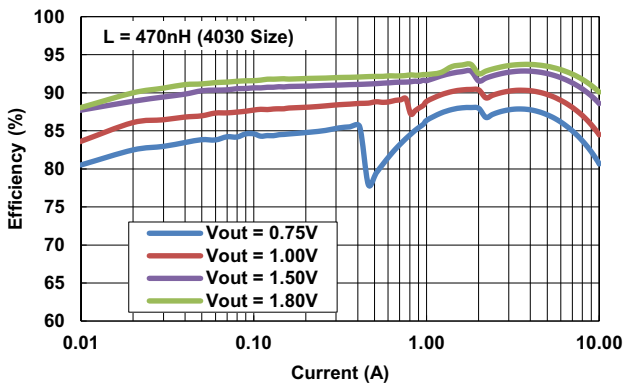


Figure 13. 2-Phase Efficiency $V_{IN} = 5.0V$

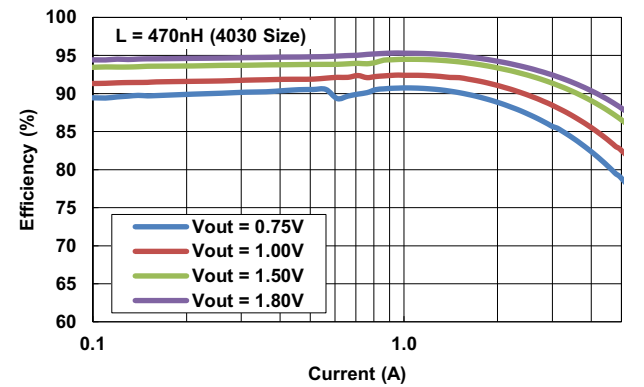


Figure 14. Single-Phase Efficiency $V_{IN} = 3.3V$

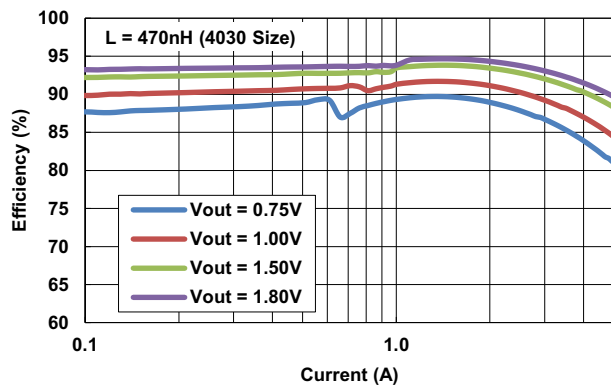


Figure 15. Single Phase Efficiency $V_{IN} = 3.8V$

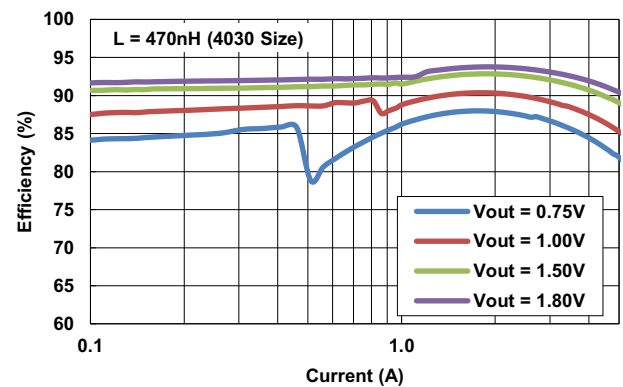
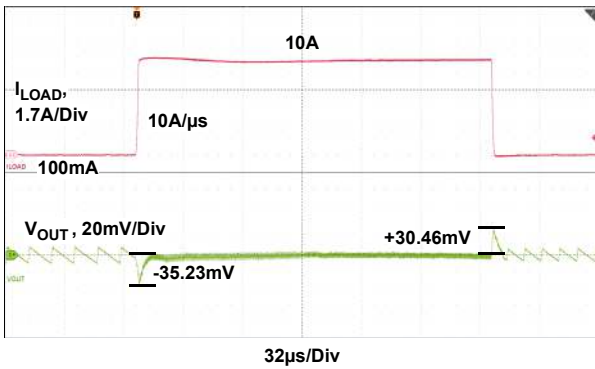


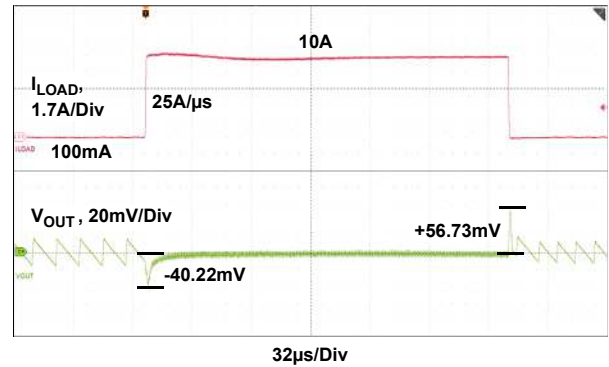
Figure 16. Single Phase Efficiency $V_{IN} = 5.0V$

Unless otherwise noted, operating conditions are: $V_{IN} = 3.8V$, $V_{OUT} = 1V$, V_{IO} and Enable = 1.8V, $T_A = +25^\circ C$, $f_{SW} = 2MHz$, 2+1+1 configuration, L = 220nH per phase, SW1: $C_{OUT} = 2 \times 22\mu F + 2 \times 4.3\mu F + 4 \times 1\mu F$, SW2-3: $C_{OUT} = 1 \times 22\mu F + 4 \times 4.3\mu F$. (Continued)



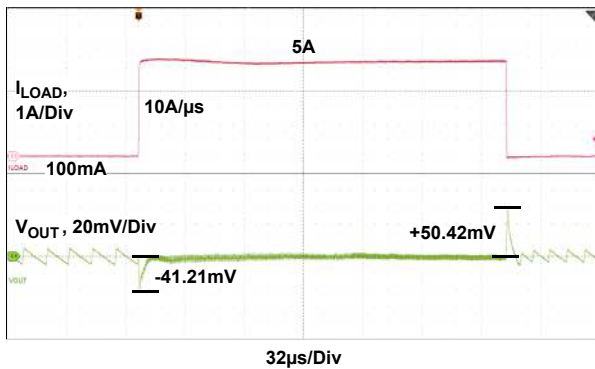
$V_{IN} = 3.8V$, $V_{OUT} = 1V$
 Load Step Slew Rate: 10A/μs, 0.1A to 10A
 220nH Inductor (Cyttec)
 5x22μF Capacitor (0603 6.3V Murata)
 2x4.3μF Capacitor (Low ESL)

Figure 17. Dual-Phase Load Transient (10A/μs)



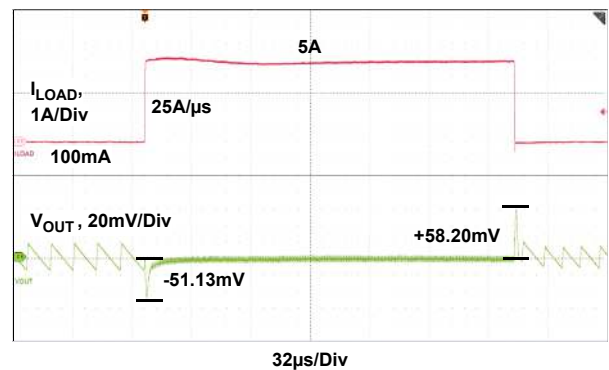
$V_{IN} = 3.8V$, $V_{OUT} = 1V$
 Load Step Slew Rate: 25A/μs, 0.1A to 5A
 220nH Inductor (Cyttec)
 5x22μF Capacitor (0603 6.3V Murata)
 2x4.3μF Capacitor (Low ESL)

Figure 18. Dual-Phase Load Transient (25A/μs)



$V_{IN} = 3.8V$, $V_{OUT} = 1V$
 Load Step Slew Rate: 10A/μs, 0.1A to 5A
 220nH Inductor (Cyttec)
 2x22μF Capacitor (0603 6.3V Murata)
 4x4.3μF Capacitor (Low ESL)

Figure 19. Single-Phase Load Transient (10A/μs)



$V_{IN} = 3.8V$, $V_{OUT} = 1V$
 Load Step Slew Rate: 25A/μs, 0.1A to 5A
 220nH Inductor (Cyttec)
 2x22μF Capacitor (0603 6.3V Murata)
 4x4.3μF Capacitor (Low ESL)

Figure 20. Single-Phase Load Transient (25A/μs)

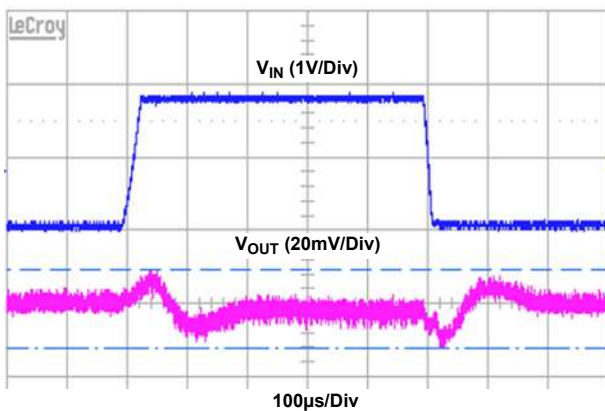


Figure 21. Dual-Phase Line Transient, $V_{OUT} = 1V$, $V_{IN} = 3.1V$ to 4.8V, Load = 8A, TR and TF = 15μs

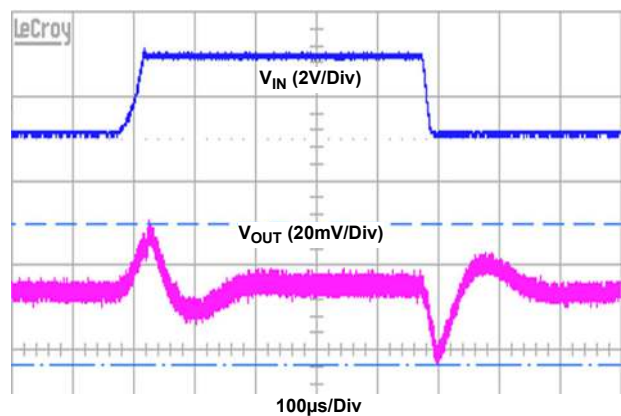


Figure 22. Single-Phase Line Transient, $V_{OUT} = 1V$, $V_{IN} = 3.1$ to 4.8V, Load = 5A, TR and TF = 15μs

Unless otherwise noted, operating conditions are: $V_{IN} = 3.8V$, $V_{OUT} = 1V$, V_{IO} and Enable = 1.8V, $T_A = +25^\circ C$, $f_{SW} = 2MHz$, 2+1+1 configuration, $L = 220nH$ per phase, SW1: $C_{OUT} = 2 \times 22\mu F + 2 \times 4.3\mu F + 4 \times 1\mu F$, SW2-3: $C_{OUT} = 1 \times 22\mu F + 4 \times 4.3\mu F$. (Continued)

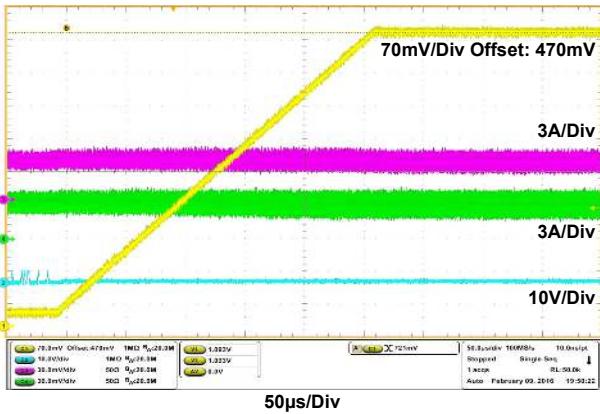


Figure 23. 0.5V to 1.1V DVS, Load = 5A, Slew Rate = 3mV/µs, CH1 - V_{OUT} , CH4 - I_{LX1} , CH3 - I_{LX2} , CH2 - DVS Command

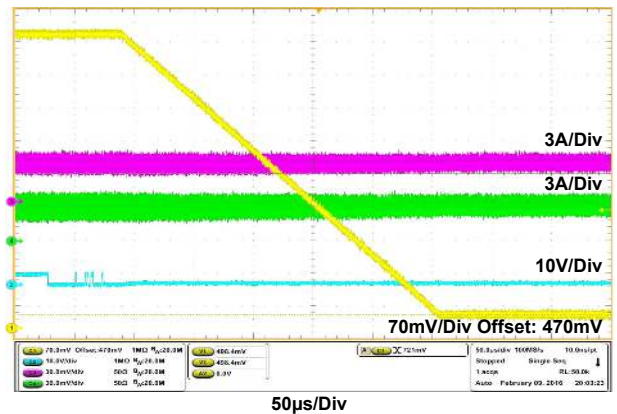


Figure 24. 1.1V to 0.5V DVS, Load = 5A, Slew Rate = 3mV/µs, CH1 - V_{OUT} , CH4 - I_{LX1} , CH3 - I_{LX2} , CH2 - DVS Command

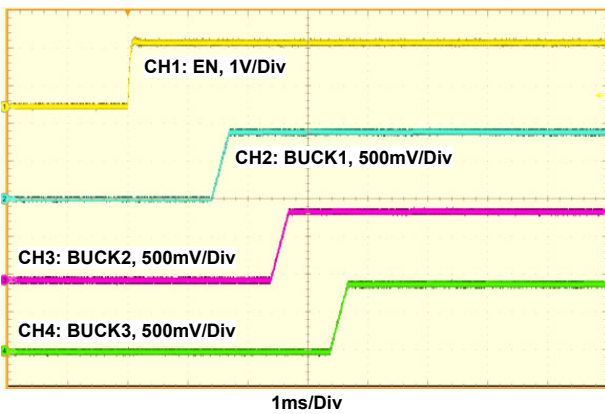


Figure 25. ISL91211AIK Startup by EN, $V_{OUT1, 2, 3} = 0.9V$

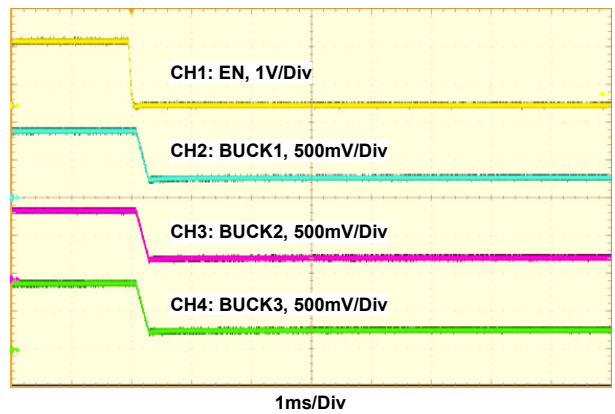


Figure 26. ISL91211AIK Shutdown by EN, $V_{OUT1, 2, 3} = 0.9V$

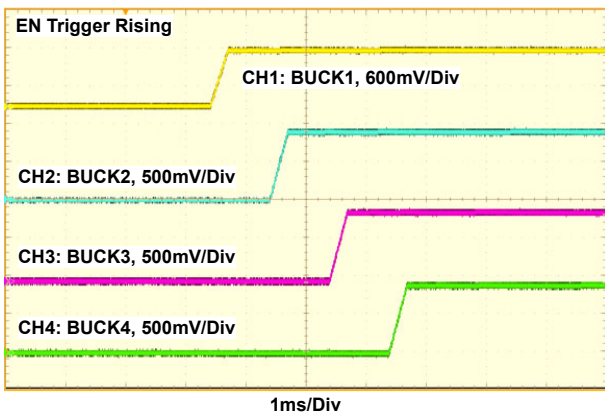


Figure 27. ISL91211BIK Startup-Up BY EN, $V_{OUT1, 2, 3, 4} = 0.9V$

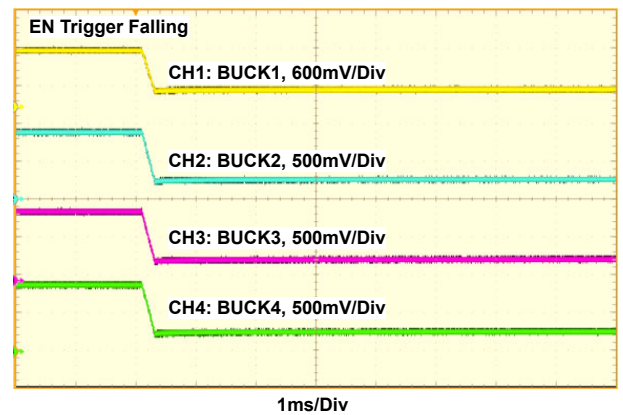


Figure 28. ISL91211BIK Shutdown by EN, $V_{OUT1, 2, 3, 4} = 0.9V$

Unless otherwise noted, operating conditions are: $V_{IN} = 3.8V$, $V_{OUT} = 1V$, V_{IO} and $Enable = 1.8V$, $T_A = +25^\circ C$, $f_{SW} = 2MHz$, 2+1+1 configuration, $L = 220nH$ per phase, SW1: $C_{OUT} = 2 \times 22\mu F + 2 \times 4.3\mu F + 4 \times 1\mu F$, SW2-3: $C_{OUT} = 1 \times 22\mu F + 4 \times 4.3\mu F$. (Continued)

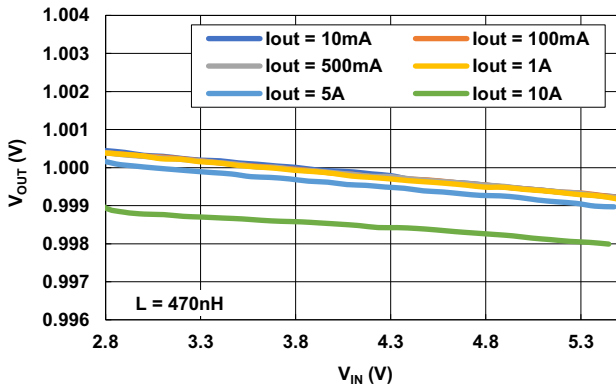


Figure 29. Dual Phase, V_{OUT} vs V_{IN} (10mA to 10A)

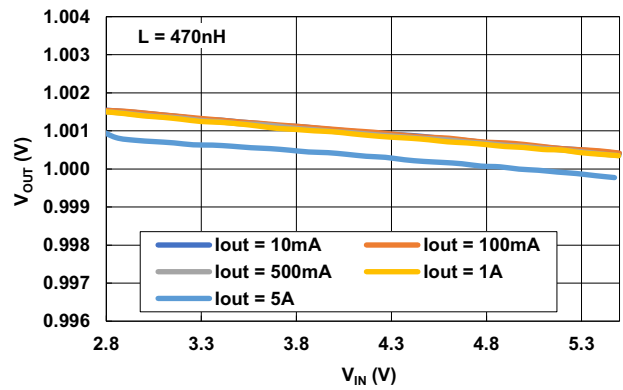


Figure 30. Single Phase, V_{OUT} vs V_{IN} (10mA to 5A)

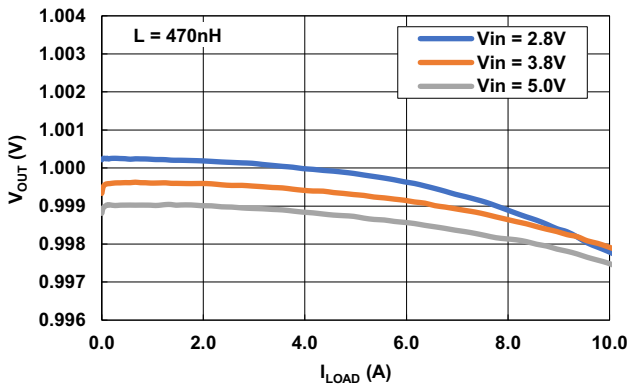


Figure 31. Dual Phase, V_{OUT} vs Load (10mA to 10A)

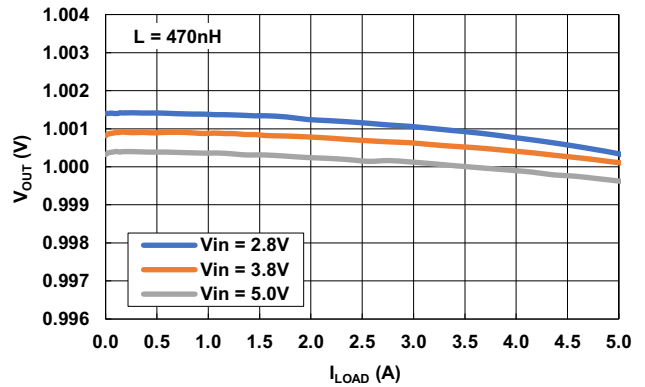


Figure 32. Single Phase, V_{OUT} vs Load (10mA to 5A)

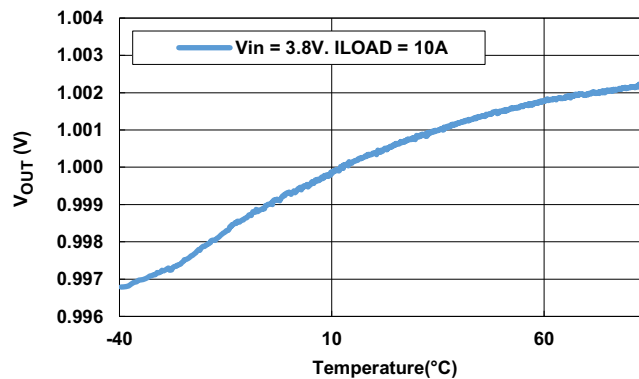


Figure 33. Dual-Phase Forced CCM, V_{OUT} vs Temperature ($-40^\circ C$ to $+85^\circ C$)

Unless otherwise noted, operating conditions are: $V_{IN} = 3.8V$, $V_{OUT} = 1V$, V_{IO} and Enable = 1.8V, $T_A = +25^\circ C$, $f_{SW} = 2MHz$, 2+1+1 configuration, $L = 220nH$ per phase, SW1: $C_{OUT} = 2 \times 22\mu F + 2 \times 4.3\mu F + 4 \times 1\mu F$, SW2-3: $C_{OUT} = 1 \times 22\mu F + 4 \times 4.3\mu F$. (Continued)

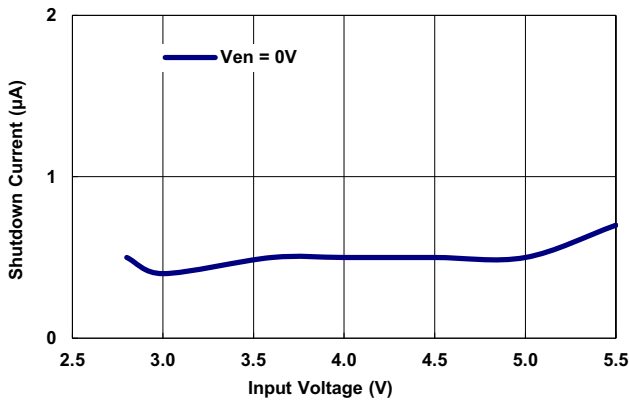


Figure 34. Shutdown Current vs V_{IN}

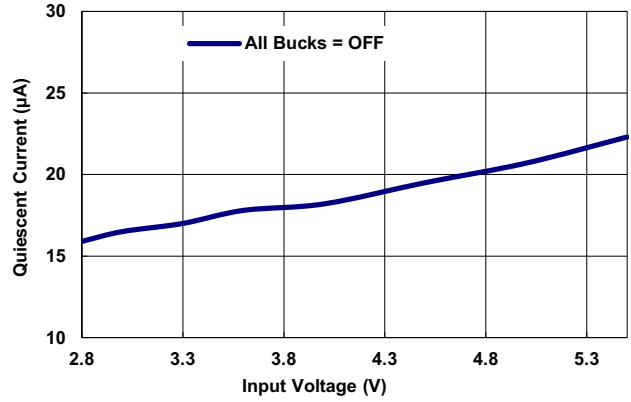


Figure 35. Quiescent Current (All Bucks Off) vs V_{IN}

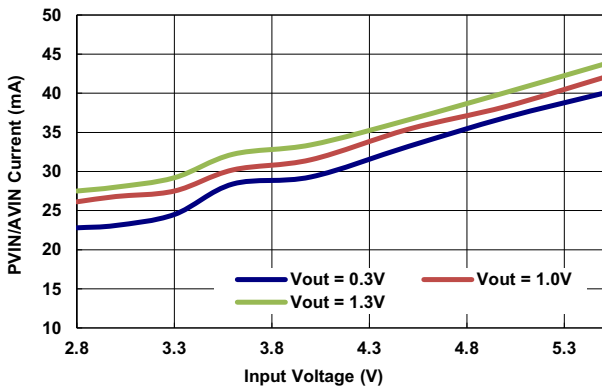


Figure 36. Single-Phase PVIN/AVIN Current (PWM Switching) vs V_{IN}

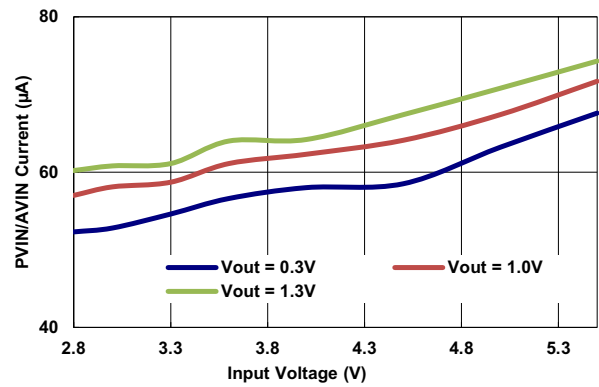


Figure 37. Single-Phase PVIN/AVIN Current (PFM Switching) vs V_{IN}

5. Applications Information

5.1 Inductor Selection

The ISL91211AIK and ISL91211BIK high-performance PMICs are integrated with synchronous buck converters delivering up to 5A of peak current per phase at 0.3V to 2.0V regulated voltage. The ISL91211BIK operates with up to four single phases (1+1+1+1 configuration), while the ISL91211AIK works with one dual phase and two single phases (2+1+1 configuration) at a switching frequency of 2MHz. In the dual phase configuration, each channel requires an inductor of equal value that can deliver up to the maximum load divided by two.

Table 5. Recommended Output Inductors

Manufacturer	Part Number	L x W x H (mm)	VALUE (nH)	DCR mΩ (Typ)	ISAT (Typ)
Cyntec	HMLB25201T	2.5x2.0x1.0	220	9.4	7.0
Taiyo Yuden	MAKK2520HR22M	2.5x2.0x1.0	220	16	8.5
Cyntec	HTTN2016T	2.0x1.6x1.0	220	13	7.2
Murata	DFE2016E	2.0x1.6x1.0	240	16	7.0
Murata	DFE252012F	2.5x2.0x1.2	470	23	6.7

5.2 Output Capacitor Selection

Output capacitors filter the switching voltage at the phase node into a regulated output voltage. The amount of output capacitance required is based on maximum load step, the slew rate of the load step, and the maximum allowable voltage regulation tolerance during the transient. The amount of ripple voltage at the output capacitor is also a design constraint; the total peak-to-peak ripple voltages produced from the output capacitor is equal to its ESR multiplied by the worst-case inductor ripple current.

Use ceramic capacitors due to their low ESR and ESL properties. Select X7R type capacitors and consider DC bias effects. A wide range of output capacitor values can be used.

Table 6. Recommended Output Capacitors

Manufacturer	Part Number	Case Size	Value (μF)	Voltage (V)
TDK	C1608X5R1A226M080AC	0603	22	10
TDK	C0510X6S0G105M030AC	0204	1	4
Murata	LLD154R60G435ME01	0402	4.3	4
Murata	LLL1U4R60G435ME22	0204	4.3	4

5.3 Input Capacitor Selection

Ceramic input capacitors source the AC component of the input current flowing into the high-side MOSFETs. Place them as close to the IC as possible. A 10μF local decoupling capacitor is recommended for each phase PVIN. If long wires are used to bring power to the IC, use additional bulk capacitors between CIN and the battery/power supply to dampen ringing and overshoot at start-up.

Internal analog reference circuits also require additional filtering at the AVIN_FILTER pin.

Table 7. Recommended Input Capacitors

Mfr	Part Number	Case Size	Value (μF)	Volt (V)	Input
TDK	CGB2A1X5R1A105M033BC	0402	1	10	AVIN_FILTER
Kemet	C0402C104K8RACTU	0402	0.1	10	AVIN_FILTER
Samsung	CL05A10MP5NUNC	0402	10	10	PVIN

5.4 Dynamic Voltage Scaling (DVS)

The ISL91211AIK and ISL91211BIK have several options to achieve Dynamic Voltage Scaling (DVS). Each buck controller has four independently programmable voltage settings to set the output voltage. The settings are DVS0, DVS1, DVS2, and DVS3. Changing the selected DVS number selects the corresponding output voltage. The two methods to select the DVS are as follows:

Method 1: Use internal registers to select DVS by writing to the BUCKx_DVSSELECT[1:0] bits in the BUCKx_DVSSEL register for each respective buck using SPI or I²C.

To use this method, the BUCKx_DVSCTRL[0] bit must be set to 0x0 for the corresponding buck. The BUCKx_DVSSELECT[1:0] setting allows you to switch between the four different DVS settings, each corresponding to a set of DVS registers holding the DVS information.

For example, DVS0 corresponds to BUCKx_DVS0VOUT92[7:0] and BUCKx_DVS0VOUT10[1:0]. The two register values combined represent the complete 10-bit DAC code for DVS0.

Table 8. DVS Method Selection

BUCK1_DVSCTRL[0]	
0x0	Use BUCKx_DVSSELECT[1:0] to select the active DVS configuration
0x1	Use the DVS pin(s) to control DVS selection

Table 9. DVS Pointers

BUCKx_DVSSELECT[1:0]	Active DVS for BUCKx
0x0	DVS0
0x1	DVS1
0x2	DVS2
0x3	DVS3

Each output voltage is set writing a 10-bit word to DVS Configuration 1 (BUCKx_DVS0CFG1 register) and DVS Configuration 0 (BUCKx_DVS0CFG0 register) in each buck. Configuration 1 holds the eight most significant bits, and Configuration 0 holds the last two bits of the 10-bit word. The output voltage does not change until the LSB register has been written. [Table 10](#) shows the relationship between the DVS word and V_{OUT}.

Table 10. 10-Bit DVS Code to Voltage Translation

FBDIV	1.0	0.8	0.6
DAC [9:0]	V _{OUT} (V)	V _{OUT} (V)	V _{OUT} (V)
0x000	0.0000	0.0000	0.0000
0x001	0.0012	0.0015	0.0020
...			
0x200	0.6144	0.768	1.024
0x201	0.6156	0.7695	1.026
...			
0x3E8	1.2	1.5	2.0

Method 2: Use the GPIO/MPIO pins to configure DVS. There are five variations depending on the IO_PINMODE register setting. See [Table 2](#) for information about the variations.

Note: To use DVS with the GPIO/MPIO pins, IO_PINMODE must be OTP programmed before a startup boot sequence is initiated. On-the-fly programming is not recommended for the following configurations.

(i) IO_PINMODE = 0x3: SPI with multiple Buck DVS pins.

MPIO0	MPIO1	MPIO2	MPIO3	GPIO0	GPIO1	GPIO2
SCK	SS_B	MOSI	MISO	DVS_A	DVS_B	DVS_C

BUCKx_DVSPIN_CFG[1:0] bits in BUCKx_SHUTDOWN_DLY registers maps the particular buck DVS to DVS_x GPIO pin. Use the same pin to control DVS for all buck controllers. BUCKx_DVSCTRL[0] should be OTP programmed high before the startup sequence. The active DVS follows the DVS_x pin logic for the respective buck. See [Table 11](#) for more information.

Table 11.

BUCKx_DVSPIN_CFG[1:0]	Function	
0x0	DVS_A pin	Active DVS for BUCKx
	0	DVS0
	1	DVS1
0x1	DVS_B pin	Active DVS for BUCKx
	0	DVS0
	1	DVS1
0x2	DVS_C pin	Active DVS for BUCKx
	0	DVS0
	1	DVS1
0x3	BUCKx DVS0 pointer follows I ² C/SPI programmed register setting.	

(ii) IO_PINMODE = 0x4: I²C with Global DVS and PGOOD pins.

MPIO0	MPIO1	MPIO2	MPIO3	GPIO0	GPIO1
DVS_PIN1	DVS_PIN0	PGOOD1	PGOOD2	I2C_CLK	I2C_SDA

The BUCKx_DVSPIN_CTRL[1:0] bits in the BUCKx_DVSCFG register in combination with the DVS_PIN1 and DVS_PIN0 set the active DVS for the respective BUCK. See [Table 12](#) for more information. BUCKx_DVSCTRL[0] should be OTP programmed high before the startup sequence.

Table 12. Global DVS Pin Logic

BUCKx_DVSPIN_CTRL[1:0]	DVS_PIN1	DVS_PIN0	Active DVS
0x0	X	X	DVS0
0x1	X	0	DVS0
	X	1	DVS1
0x2	0	X	DVS0
	1	X	DVS2
0x3	0	0	DVS0
	0	1	DVS1
	1	0	DVS2
	1	1	DVS3

Note: The 'X' indicates that either a 0 or 1 is acceptable.

(iii) IO_PINMODE = 0x5: I²C with two DVS pins for Buck1 and two DVS pins for Buck2.

MPIO0	MPIO1	MPIO2	MPIO3	GPIO0	GPIO1
BUCK1_DVS0	BUCK1_DVS1	BUCK2_DVS0	BUCK2_DVS1	I2C_CLK	I2C_SDA

The active DVS is selected based on the combined BUCKx_DVS0 and BUCKx_DVS1 input pin logic. See [Table 13](#) for more information. BUCKx_DVSCTRL[0] should be OTP programmed high before the startup sequence.

Table 13. Active DVS for 2 DVS Pins Configuration

BUCKx_DVS1	BUCKx_DVS0	Active DVS for BUCKx
0	0	DVS0
0	1	DVS1
1	0	DVS2
1	1	DVS3

(iv) IO_PINMODE = 0x6: I²C with full 2 pin DVS control for Buck1 and 1 pin DVS control for Buck2 and Buck3.

MPIO0	MPIO1	MPIO2	MPIO3	GPIO0	GPIO1
BUCK1_DVS0	BUCK1_DVS1	BUCK2_DVS0	BUCK3_DVS0	I2C_CLK	I2C_SDA

BUCKx_DVSCTRL[0] should be OTP programmed high before the startup sequence. BUCK1_DVS0 and BUCK1_DVS1 follow the same active DVS table as in IO_PINMODE = 0x5. See [Table 14](#) for more information.

Table 14. Active DVS for 1 DVS Pin Configuration

BUCKx_DVS1	BUCKx_DVS0	Active DVS for BUCKx
0	0	DVS0
0	1	DVS1

(v) IO_PINMODE = 0x7: I²C with 1 pin DVS control for each buck.

MPIO0	MPIO1	MPIO2	MPIO3	GPIO0	GPIO1
BUCK1_DVS0	BUCK2_DVS0	BUCK3_DVS0	BUCK4_DVS0	I2C_CLK	I2C_SDA

BUCKx_DVSCTRL[0] should be OTP programmed high before the startup sequence. BUCKx_DVS0 follows the same active DVS table for 1 DVS pin configuration as in IO_PINMODE = 0x6. See [Table 3](#) for more information.

5.5 Configuring DVS Speed

5.5.1 Power-Up and Shutdown Slew Rate Setting

The BUCKx_RSPPUP[2:0] bits in the BUCKx_RSPCFG0 register set the slew rates (DVS speed) in BUCKx only during VOUTx power-up. Similarly, the BUCKx_RSPPDN[2:0] bits in the BUCKx_RSPCFG0 register set the slew rates in BUCKx during normal VOUTx shutdown. The achievable slew rates vary with different FBDIV settings (factory OTP programmed). For more details, see Register [BUCK1_RSPCFG0](#).

5.5.2 DVS Transition Slew Rate Setting

The BUCKx_RSPUP[2:0] and BUCKx_RSPDN[2:0] bits in the BUCKx_RSPCFG1 register set the slew rates (DVS speed) in BUCKx during normal DVS transition. The achievable slew rates vary with different FBDIV settings (factory OTP programmed). For more details, see Register [BUCK1_RSPCFG1](#).

5.6 Output Voltage Setting

Each output voltage is set by writing a 10-bit word to DVS Configuration 1 (BUCKx_DVS0CFG1 register) and DVS Configuration 0 (BUCKx_DVS0CFG0 register) in each buck. Configuration 1 holds the MSB and Configuration 0 holds the last two bits of the 10-bit word. The output voltage does not change until the LSB register is written. [BUCK1_DVS0CFG1](#) shows the relationship between the DVS word and V_{OUT}.

5.7 Power Sequencing

When the master chip Enable (EN) pin is above an NMOS threshold, the ISL91211AIK and ISL91211BIK powers up its key biasing circuits, loads the OTP configuration registers, and performs one of the following actions based on the preprogrammed OTP setting.

5.7.1 Manual Buck Start-Up

Program the internal IO_BUCKx_EN bits to 1 from I²C/SPI to enable the respective buck. When IO_PINMODE = 0x1, the EN_A, EN_B, and EN_C pins can also be used to enable the respective bucks. If using this pin mode, the internal IO_BUCKx_EN bits should be set high in OTP. The slew rate of each buck during its soft-start is specified by the BUCKx_RSPPUP[2:0] bits.

Note: The programmable delay (1ms to 63ms) using BUCKx_EN_DLY[5:0] is not used for Manual Buck startup.

5.7.2 Auto Buck Start-Up from Master Chip Enable Pin

Run a predetermined startup sequence for the buck outputs as soon as BOOT is complete. The slew rate of each buck during its soft-start is specified in BUCKx_RSPPUP[2:0].

[Figure 38](#) provides an example of power-up configurability. The master chip enable pin (EN) transitions from 0 to 1, and OTP is loaded over 1.4ms. After the initial 1.4ms boot interval, the buck output start-up sequence begins. In the [Figure 38](#) example, BUCK1_EN_DLY is set for 0ms, BUCK2_EN_DLY is set for 1ms, BUCK3_EN_DLY is set for 2ms, and BUCK4_EN_DLY is set for 3ms.

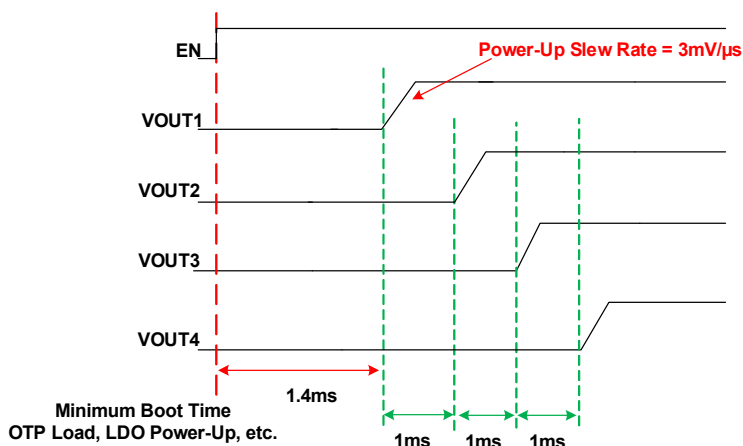


Figure 38. Master Chip Enable Power-Up Example

The buck outputs can also be programmed to execute a controlled shutdown in two ways.

5.7.3 Manual Buck Power-Down

Program the internal IO_BUCKx_EN bit to 0 through I²C/SPI or lower the Buck Enable pin (EN_A, EN_B, and EN_C when IO_PINMODE = 0x1). The manual method can be used to power down a specific buck (with a controlled slew rate) while keeping the rest of the chip alive.

Note: The programmable (0ms to 63ms) delay from BUCKx_SHUTDN_DLY[5:0] is not used for manual buck power-down.

5.7.4 Auto Buck Power-Down from Master Chip Enable Pin

When the master chip Enable pin (EN) is below the falling threshold of the comparator, the Bucks are ramped down at a controlled rate using preprogrammed delays. The bias circuits then power down, forcing the chip into shutdown. The slew rate of each buck during its power-down (down to ~250mV) is specified in BUCKx_RSPPDN[2:0].

Figure 39 provides an example of power-down configurability. The master chip enable pin (EN) transitions from logic 1 to 0. In the Figure 39 example, BUCK1_SHUTDOWN_DLY is set for 1ms, BUCK2_SHUTDOWN_DLY is set for 1ms, BUCK3_SHUTDOWN_DLY is set for 1ms, and BUCK4_SHUTDOWN_DLY is set for 1ms.

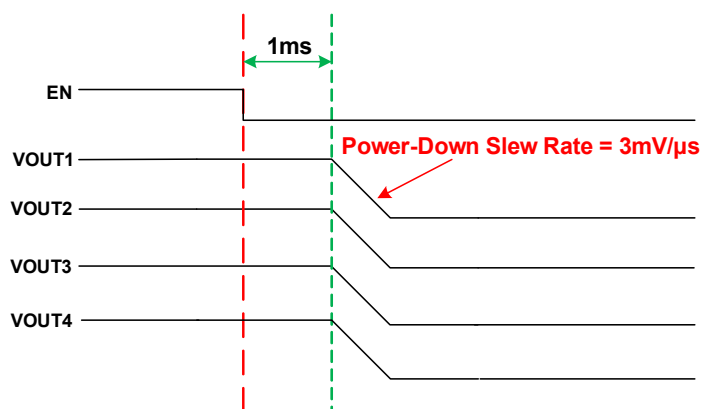


Figure 39. Auto Chip Power-Down Example

The actual slew rate that each buck ramps down to is specified by the register BUCKx_RSPPDN. The default slew rate for each buck discharging during power-down sequence is 3mV/µs. This slew rate is controlled until the output voltage is ~250mV. Below 250mV, there are two output voltage decay options:

Option 1: If the disable event for a buck output is the master chip enable pin (EN) falling below its logic high threshold, then when the output falls below 250mV, the output voltage decay is dictated by the system load passively discharging the buck output capacitance. PULL_DOWN_DISCHARGE bit per the BUCK2_CFG2 register is **not** used in this method.

Option 2: If the disable event for a buck output is the master chip enable pin (EN) remaining high and the enable register bit (IO_BUCKx_EN) transitioning from a logic 1 to a logic 0, then PULL_DOWN_DISCHARGE bit per the BUCK2_CFG2 register is used enabling an internal weak pull down.

Note: The weak pull-down can be disabled using factory OTP.

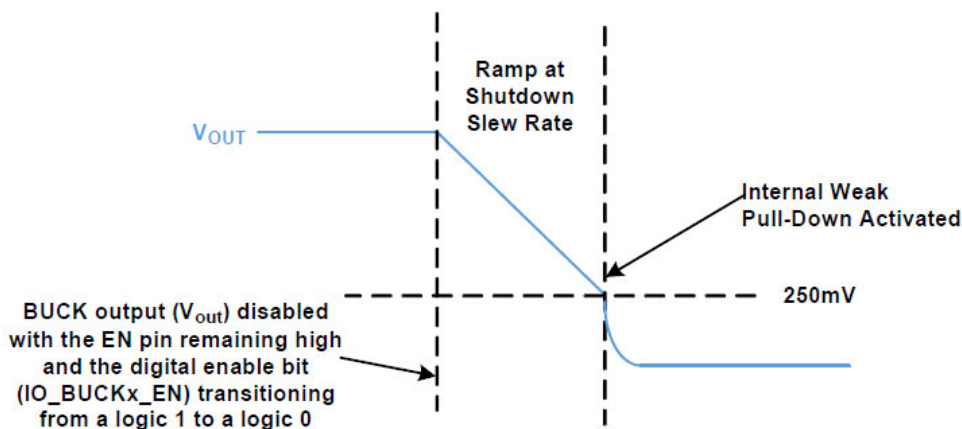


Figure 40. Buck Disable Waveform

5.8 Watchdog Time (WDOG_RST Pin)

The ISL91211AIK and ISL91211BIK implement a watchdog function that allows the output voltages to return to a safe OTP default when communication to the processor host is lost. This is determined by monitoring the state of the WDOG_RST pin. If the pin goes low for greater than 10ms, the default voltages from OTP are restored.

All four bucks respond to the WDOG_RST pin. The polarity of the WDOG_RST pin is active low.

Table 15. WDOG_RST Function

Action	
At Boot Up	DVS registers are loaded with values stored in OTP
After Debounce Time	Restores selected output voltages to their original values stored in OTP (DVS0), and slews the buck outputs to that voltage

Total recovery time for the buck is the sum of the t_{SLEW} and $t_{DEBOUNCE}$. The WDOG_RST pin resets the ISL91211AIK and ISL91211BIK buck outputs to the target voltage set by DVS0, which is in the BUCKx_DVS0CFG1 and BUCKx_DVS0CFG0 registers.

t_{SLEW} is determined by the default output voltage divided by $3mV/\mu s$, while $t_{DEBOUNCE}$ is set at 10ms.

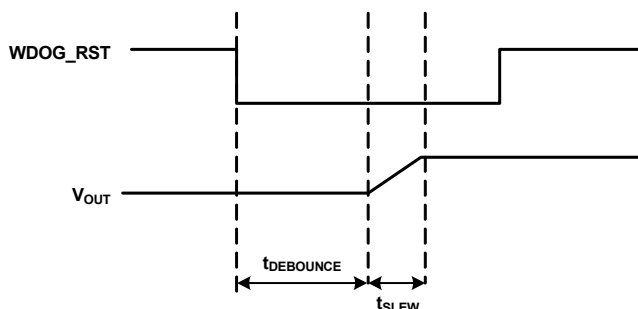


Figure 41. Watchdog Timer Example Case

5.9 Interrupt Pin

The ISL91211AIK and ISL91211BIK alert the host when a warning or a fault has occurred through an IRQ interrupt request signal with configurable masking options that is connected to a configurable interrupt (INT) pin. The interrupt pin can be programmed to be active high, active low, an open drain, or a CMOS output.

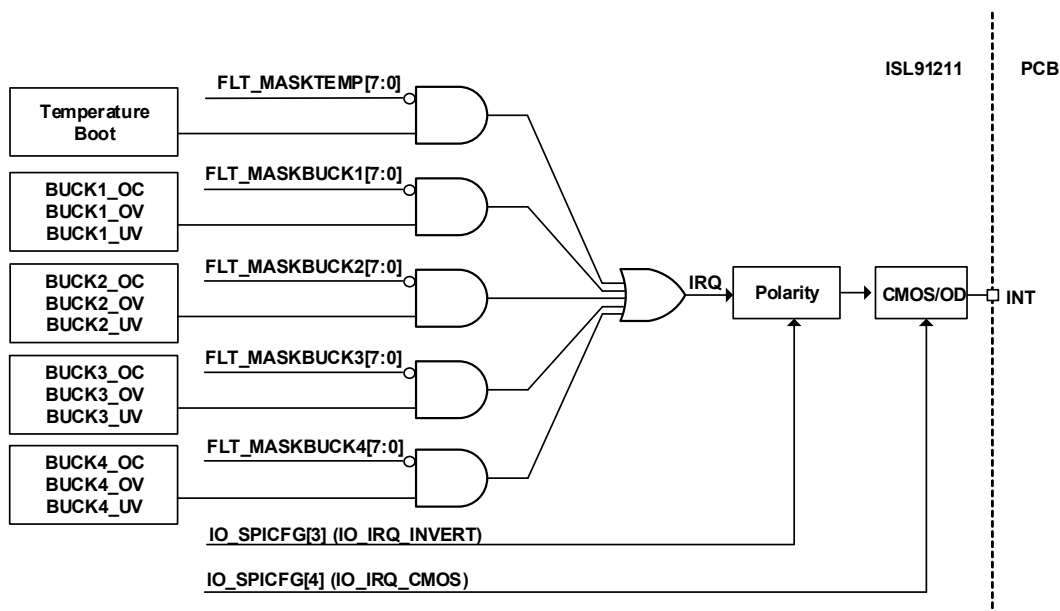


Figure 42. Interrupt Tree

6. Protection Features (FAULTS)

The ISL91211AIK and ISL91211BIK have Overcurrent (OC), overvoltage, undervoltage, and over-temperature protection features.

6.1 Over-Temperature Protection

The ISL91211AIK and ISL91211BIK provide protection against over-temperature conditions. The over-temperature protection circuit continuously monitors the die temperature and raises a fault when the temperature exceeds +150°C. When the over-temperature fault occurs, all the buck converters shut down by default, they are then re-enabled when the OT fault deasserts. Hysteresis enables the circuit to clear the fault when the temperature falls below a predefined safe temperature. Hysteresis is hard-coded as the difference between +95°C and +150°C.

6.2 Overcurrent Protection Mode

The overcurrent protection block has a current comparator that compares the load current through the high-side power FET with the reference current level through a replica device. After RC delay filtering and/or cycle detection filtering, the output of the overcurrent protection block goes to the fault detection block, which makes the decision to disable the buck and latch the power-stage into high impedance mode. The digital core periodically re-enables the buck to detect whether the fault has cleared.

6.3 Overvoltage (OV)/Undervoltage (UV) Protection

The ISL91211AIK and ISL91211BIK protect against output Overvoltage (OV) and Undervoltage (UV) fault conditions. The OV/UV protection circuitry has low power comparators configured with differential input and single-ended outputs capable of working over a large common-mode input range. This comparator monitors the output voltage in both DCM and CCM for faults.

By default, when an OV is triggered, the buck converter crowbars the output by turning on the low-side NMOS for a duration of 32µs to 64µs. After that, the buck shuts down and exits crowbar. The buck tries to start up and if the fault condition still exists, the buck reacts to OV again until the fault is removed. When an UV event is triggered, the buck converter shuts down and restarts until the fault is cleared. The UV/OV threshold is a configurable window around the V_{OUT} DAC target. The default setting is ±250mV.

7. Serial Communication Interface

The ISL91211AIK and ISL91211BIK have two serial interface protocols to read/write the registers.

- SPI
- I²C

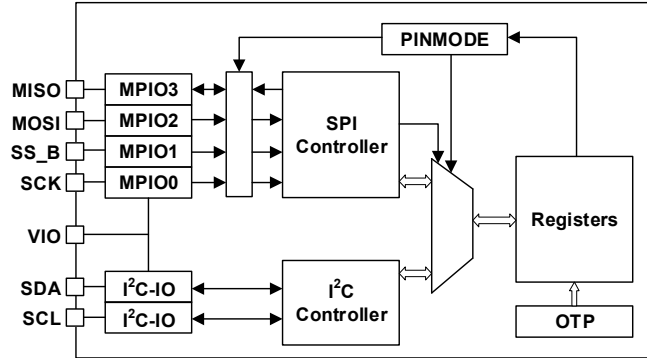


Figure 43. SPI/I²C Interface

The arbitration of the register access bus (between SPI and I²C) is determined by the IO_PINMODE register and the MPIO1 pin as shown in [Table 16](#).

Table 16. SPI/I²C Register Access

Register IO_PINMODE	MPIO_1 Pin (SS_B)	Register Access
0	0	SPI (Read/Write Access (Note 11))
	1	I ² C (Note 12)

Notes:

11. When the device is configured for SPI access, I²C should not be addressed with the device ID.
12. When the device is configured for I²C access, in PINMODE 0, the SS_B line must be held high.

After switching from SPI to I²C or from I²C to SPI, a minimum 50ns wait time is required before starting a transaction.

7.1 SPI Interface

SPI is a 4-wire slave interface that can operate at a clock speed of up to 26MHz. It is based on byte transfers.

7.1.1 SPI Data Protocol

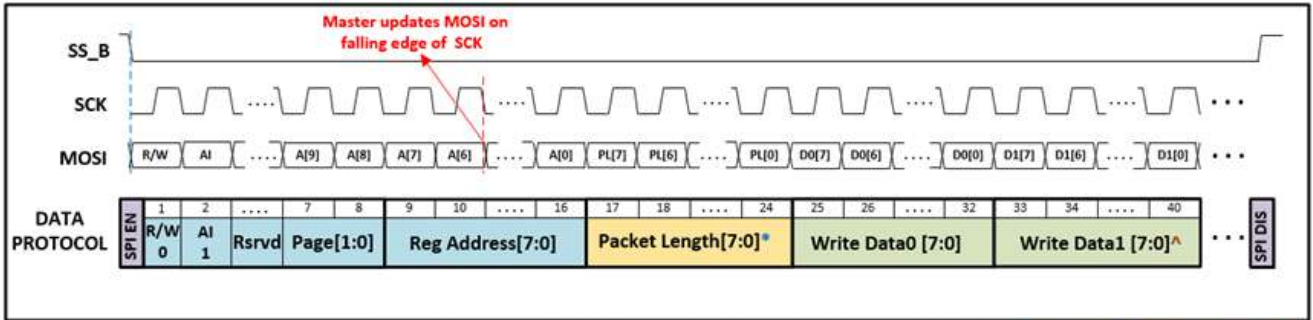
Both Read and Write SPI transactions begin when SS_B goes low and end when SS_B goes high.

Write Operation: To write to the ISL91211AIK and ISL91211BIK, the master (controller) does the following:

1. Drives SS_B low.
2. Sends the Control Byte, followed by the register address, packet length (if IO_SPI MODE = 1), and Data bytes to be written.
3. Drives SS_B high to terminate the transaction as shown in [Figure 44](#).

The MSB of the Control byte is the R/W bit, that must be set to the write operation (see IO_SPI RWPOL). Bit 6, AI (Auto Increment) indicates whether the write is a single byte write operation or a multi-byte write. Bits 1 and 0 of the Control byte indicate the page number of the register location to be written (MSBs of the register address). The register address byte is the 8-bit register address within the page specified by the Page[1:0] bits. If IO_SPI MODE = 1, the register address is followed by the 8-bit packet length, indicating the number of bytes to be written. Following the packet length field, the master sends the data bytes. When all eight bits are received, they are written to the specified register address. ISL91211AIK and ISL91211BIK then increments the register address. In single-byte transactions, (AI = 0 or Packet length = 1), the ISL91211AIK and ISL91211BIK enter the

wait state and wait for SS_B to go high. In multi-byte transactions with IO_SPIMODE = 1, the ISL91211AIK and ISL91211BIK write incoming data bytes to sequentially incrementing addresses when the number of bytes, specified by packet length, are received, ISL91211AIK and ISL91211BIK enter the wait state and wait for SS_B to go high. In multi-byte transactions with IO_SPIMODE = 0 and AI = 1, the ISL91211AIK and ISL91211BIK keep writing the subsequently received data bytes to sequentially incrementing addresses until SS_B goes high. If SS_B goes high in the middle of a transaction, the transaction is terminated. All data bytes that receive all eight bits are written.



* Only present when IO_SPIMODE = 1
 ^ Only present for Multi Word Transactions

Figure 44. SPI Write Transaction with IO_SPIMODE = 1; IO_SPICPOL = 0; IO_SPICPHA = 0

Read Operation: To read from the ISL91211AIK and ISL91211BIK, the master (controller) does the following:

1. Drives SS_B low.
2. Sends the Control Byte, followed by the register address and packet length (if IO_SPIMODE = 1).
3. The ISL91211AIK and ISL91211BIK send the Data bytes from the requested registers.
4. The master drives SS_B high to terminate the transaction as shown in [Figure 45](#).

The MSB of the Control byte is the R/W bit, that must be set to the Read operation (see IO_SPIRWPOL). Bit 6, AI indicates whether the read is a single byte read operation or a multi-byte read. Bits 1 and 0 of the Control byte indicate the page number of the register location desired to be read (MSBs of the register address). The register address byte is the 8-bit register address within the page specified by the Page[1:0] bits. If IO_SPIMODE = 1, the register address is followed by an 8-bit packet length, indicating the number of bytes to be written. Following the packet length field, the ISL91211AIK and ISL91211BIK send the data from the requested register. When all eight bits of data from the requested register address are sent, the ISL91211AIK and ISL91211BIK increment the register address. In a single byte transaction, (AI = 0 or Packet length = 1), the ISL91211AIK and ISL91211BIK go into the wait state and wait for SS_B to go high. In a multi-byte transaction with IO_SPIMODE = 1, the ISL91211AIK and ISL91211BIK send the data bytes from sequentially incrementing addresses until the number of bytes specified by 'packet length' are sent, then enter the wait state and wait for SS_B to go high. In multi-byte transactions with IO_SPIMODE = 0 and AI = 1, the ISL91211AIK and ISL91211BIK keep sending data bytes from sequentially incrementing addresses until SS_B goes high.

Note: The MISO pin is pulled low while SS_B is high.

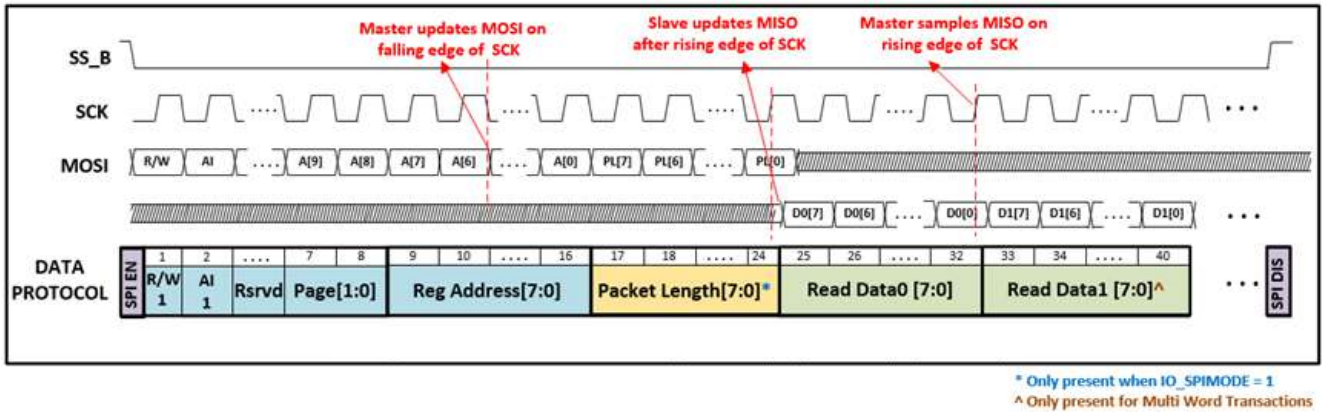


Figure 45. SPI Read Transaction with IO_SPIMODE = 1; IO_SPICPOL = 0; IO_SPICPHA = 0

R/W	Read/Write Bit Indicating Read or Write Operation
AI	Auto Increment. 1 indicates a multi byte transfer. 0 indicates a single byte transfer
Page	2-bit page address of the register to be written/read
Address	8-bit register address of the register to be written/read
Packet Length	8-bit packet length indicating number of data bytes to be transferred. Overrides AI when IO_SPIMODE = 1
Read Datan	Data in the register at Address [7:0] + n
Write Datan	Data to be written to the register at Address [7:0] + n

7.1.2 SPI Configuration

The following register bits configure the SPI operation:

- **IO_SPICPOL**: SPI clock polarity, configures the ISL91211AIK and ISL91211BIK as active high, IO_SPICPOL = 0
- **IO_SPICPHA**: SPI clock phase, ISL91211AIK and ISL91211BIK sample data on rising edge of SPI clock, IO_SPICPHA = 0

The four possible clocking modes are shown in [Figure 46](#).

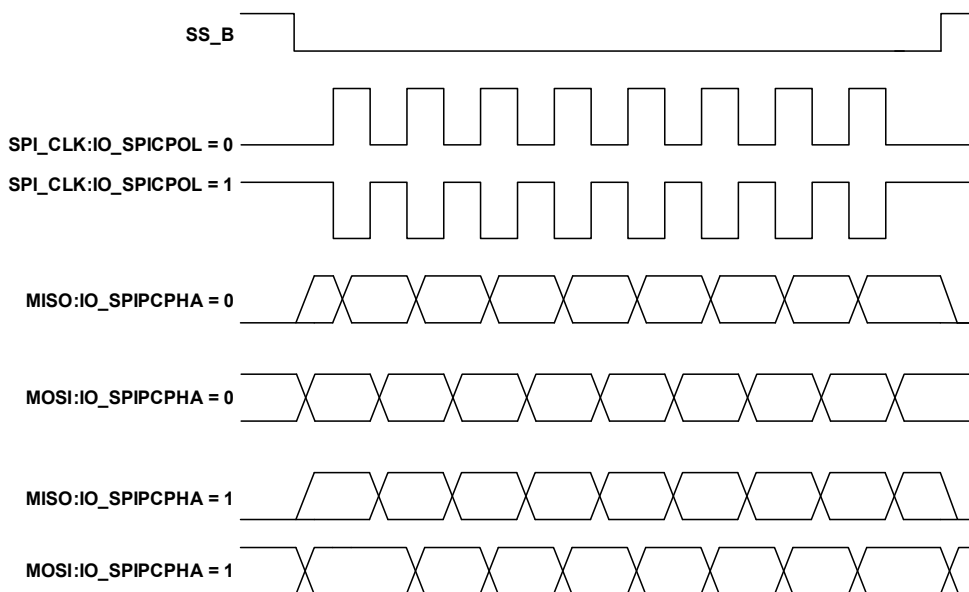


Figure 46. Four Possible Clocking Modes

- **IO_SPIRWPOL:** R/W bit polarity, ISL91211AIK and ISL91211BIK SPI_RWPOL is set to 0, 1: Read, 0: Write.

SPI_RWPOL	R/W	Operation
0	0	Write
0	1	Read

- **IO_SPIMODE:** Packet length enable, ISL91211AIK and ISL91211BIK use packet length mode by default, meaning the third data byte from the master is the packet length and indicates the total number of data words to be sent/received in a burst transaction.

7.1.3 SPI Timing

Figure 47 shows SPI timing for IO_SPICPOL = 0; IO_SPICPHA = 0. The timing values in Table 17 are also true for other values of IO_SPICPOL, IO_SPICPHA.

Table 17. Timing Values

Parameter	Symbol	Min	Typ	Max	Unit
Clock Period	t_1	38.4			ns
Enable Lead Time	t_2	12			ns
Enable Lag Time	t_3	12			ns
Clock High or Low Time	t_4	15			ns
Data Setup Time (Input)	t_5	12			ns
Data Hold Time (Input)	t_6	10			ns
Time MISO will be Stable before the Next Rising Edge of CLK	t_7	5			ns
Data Held after Clock Edge (Output)	t_8	5			ns
Load Capacitance	CL			10	pF

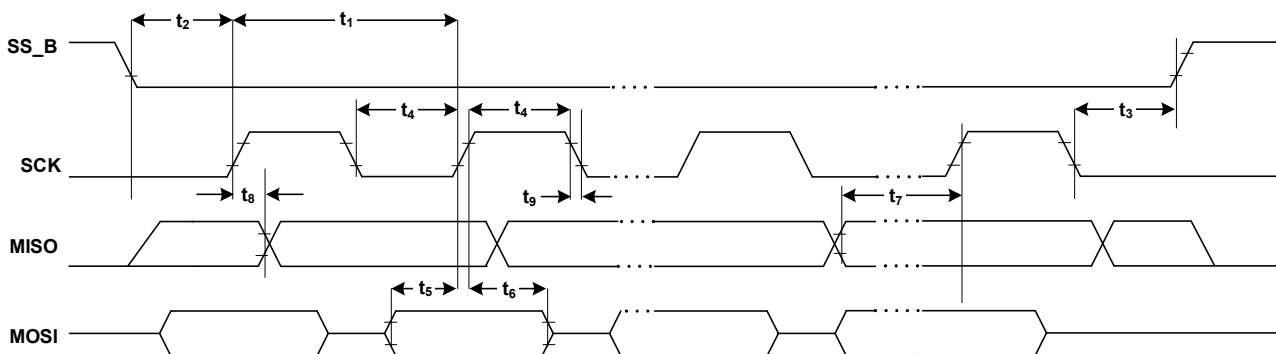


Figure 47. SPI Timing for IO_SPICPHA = 0, IO_SPICPOL = 0

7.2 I²C Interface

The I²C interface is a simple, bidirectional 2-wire bus protocol, with a serial clock control (SCL/I2C_CLK) signal and serial data signal (SDA/I2C_SDA). The ISL91211AIK and ISL91211BIK host a slave I²C interface that supports data speeds up to 3.4Mbps. I2C_CLK is an input to the ISL91211AIK and ISL91211BIK supplied by the controller, while the SDA is bidirectional. The ISL91211AIK and ISL91211BIK have an open-drain output to transmit data on the SDA. Place an external pull-up resistor on the serial data line to pull the drain output high during data transmission.

The ISL91211AIK and ISL91211BIK use a 7-bit hardware address scheme. The default address is set to 0x1E by a onetime programmable fuse.

7.2.1 I²C Bus Operation

The chip supports 7-bit addressing. The ISL91211AIK and ISL91211BIK I²C device address is reconfigurable through the OTP.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first. Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see [Figure 52](#)).

All I²C interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH. The ISL91211AIK and ISL91211BIK continuously monitor the SDA and SCL lines for the START condition and do not respond to any command until this condition is met. All I²C interface operations must be terminated by a STOP condition, which is a LOW-to-HIGH transition of SDA while SCL is HIGH.

An Acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data ([Figure 52](#)). The ISL91211AIK and ISL91211BIK respond with an ACK after recognition of a START condition, followed by a valid Identification (I²C Address) Byte. The ISL91211AIK and ISL91211BIK also respond with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

Write Operation: A Write operation requires a START condition, followed by an ISL91211AIK and ISL91211BIK I²C Address byte with the R/W bit set to 0, a Register Address Byte, Data Bytes, and a STOP condition. The ISL91211AIK and ISL91211BIK respond with an ACK after each byte. After every data byte, the ISL91211AIK and ISL91211BIK auto increment the register address so that subsequent data bytes are written to sequentially incremental register locations. A STOP condition that terminates the write operation must be sent by the master after sending at least one full data byte and its associated ACK signal. If a STOP byte is issued in the middle of a data byte, the write is not performed.

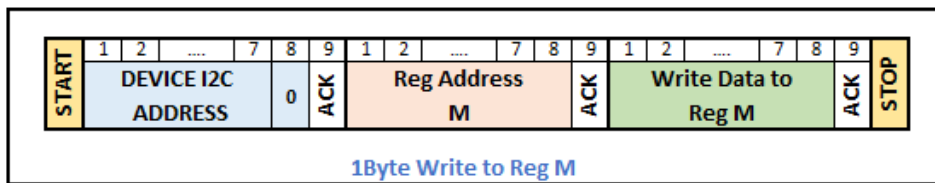


Figure 48. 1-Byte Write to Register M

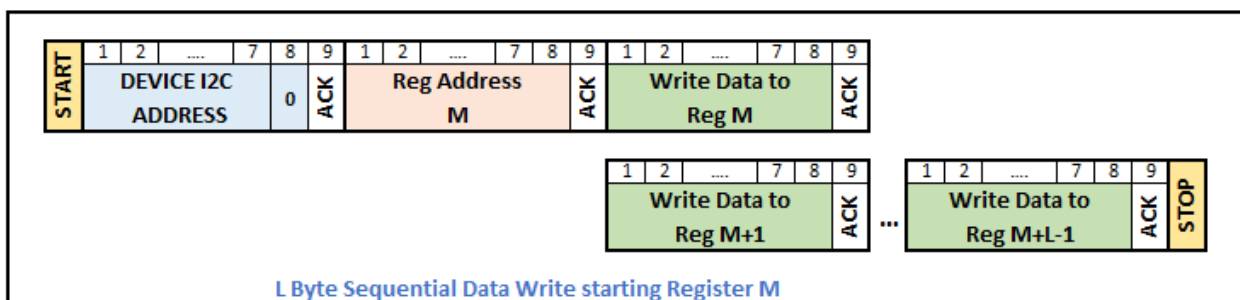


Figure 49. L-Byte Sequential Data Write Starting Register M

Read Operation: A Read operation consists of a three-byte dummy write instruction to send the register address to begin reading from, followed by a Current Address Read operation. The master initiates the operation, issuing the following sequence: a START condition, followed by an ISL91211AIK and ISL91211BIK I²C Address byte with the R/W bit set to 0, a Register Address Byte, a second START, and a second ISL91211AIK and ISL91211BIK I²C Address byte with the R/W bit set to 1. After each of the three bytes, the ISL91211AIK and ISL91211BIK respond with an ACK. The ISL91211AIK and ISL91211BIK then transmit Data Bytes. The master terminates the Read operation from the ISL91211AIK and ISL91211BIK by issuing a STOP condition following the last bit of the last data byte. After every data byte, ISL91211AIK and ISL91211BIK auto increment the register address so subsequent data bytes are sent from sequentially incremental register locations.

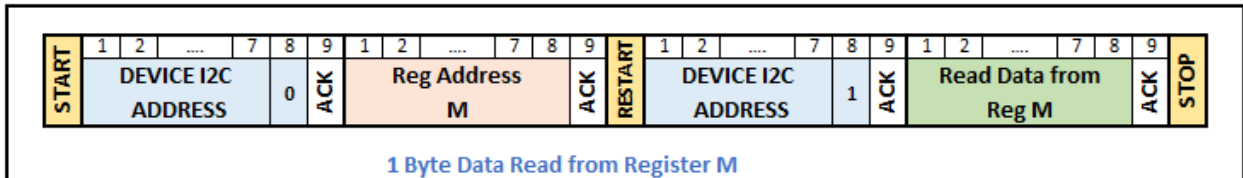


Figure 50. 1-Byte Data Read From Register M

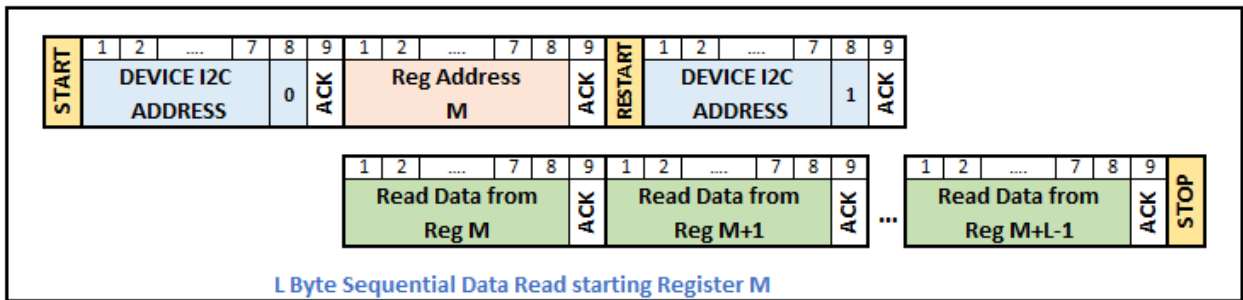


Figure 51. L-Byte Sequential Data Read Starting Register M

7.2.2 I²C Timing

The I²C I/O timing specifications are shown in Figure 52 and Table 18. The I²C controller provides a slave I²C transceiver capable of interpreting I²C protocol in the following modes:

- Standard
- Fast
- Fast+
- High Speed

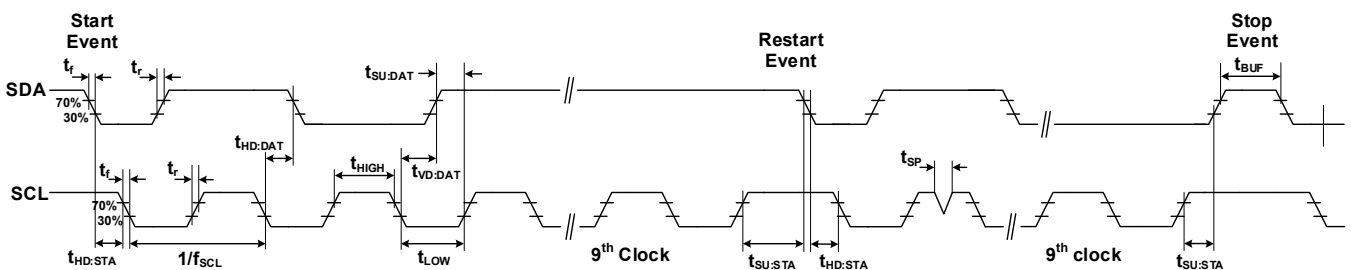


Figure 52. I²C Timing

Table 18. Timing Specifications

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		High Speed Mode		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock Frequency	f_{SCL}	0	100	0	400	0	1000	0	3400	kHz
Hold Time (repeated) START Condition (the first clock pulse is generated after this period)	$t_{HD;STA}$	4000	-	600	-	260	-	160	-	ns
LOW Period of the SCL Clock	t_{LOW}	4700	-	1300	-	500	-	160	-	ns
HIGH Period of the SCL Clock	t_{HIGH}	4000	-	600	-	260	-	60	-	ns
Set-Up Time for a Repeated START Condition	$t_{SU;STA}$	4700	-	600	-	260	-	160	-	ns
Data Hold Time	$t_{HD;DAT}$	15	-	15	-	15	-	15	70	ns
Data Set-Up Time	$t_{SU;DAT}$	250	-	100	-	50	-	10	-	ns
Rise Time of SCL	t_{rCL}	-	1000	-	300	-	120	-	40	ns
Fall Time of SCL	t_{fCL}	-	300	-	300	-	120	-	40	ns
Rise Time of SDA	t_{rDA}	-	1000	-	300	-	120	-	80	ns
Fall Time of SDA	t_{fDA}	-	300	-	300	-	120	-	80	ns
Set-Up Time for STOP Condition	$t_{SU;STO}$	4000	-	600	-	260	-	160	-	ns
Bus Free Time between a STOP and START Condition	t_{BUF}	4700	-	1300	-	500	-	-	-	ns
Capacitive Load for each Bus Line	C_D	-	400	-	400	-	400	-	100	pF
Output Fall Time from VIHmin to VILmax	t_{of}	-	250[5]	$20 \times (V_{DD}/5.5V)[6]$	250[5]	$20 \times (V_{DD}/5.5V)[6]$	120[7]	10 (Note 14)	80	ns
Pulse Width of Spikes Suppressed by the Input Filter	t_{SP}	-	-	0	50	0	50	0	10	ns

Notes:

13. Valid only for $V_{DD} < 4V$.
14. Valid only for $V_{DD} < 1.9V$.
15. V_{DD} is the pull-up source to the I²C lines (GPIO0, GPIO1).

8. Board Layout Recommendations

The ISL91211AIK and ISL91211BIK are 4-channel PMICs consisting of high frequency switching regulators with dual and single phase capability. Correct PCB layout is crucial to ensure satisfactory performance. The power loop is composed of the output inductor L, the output capacitor C_{OUT}, the SW pin, and the PGND pin. Make the power loop as small as possible. The connecting traces among the power loop components should be direct, short, and wide. The same design practices apply to the connections at PVIN. Place the input capacitor as close as possible to the PVIN and PGND pins of the corresponding power stage.

The switching node of the converter, the SW pin, and the traces connected to this node are very noisy, so keep the remote sense lines and other noise sensitive traces away from these traces. Keep the trace connection between the SW pin and the inductor short and wide, and use multiple copper planes in parallel, with sufficient vias in between to maximize thermal performance and efficiency. Renesas recommends descending only one layer for the phase traces to reduce the effective path to the inductor. Ensure the length and width of each inductor trace, and number of vias used, match resistances; this helps ensure proper current matching, when using the dual phase configuration in the ISL91211AIK.

Connect the ground of the input and output capacitors as close as possible. Use as much ground plane as possible underneath the ISL91211AIK and ISL91211BIK. More ground plane supports high current flow and creates a low impedance path for the return current between ISL91211AIK and ISL91211BIK and the load. As much as possible, use a solid ground plane, it helps prevent the SW node traces and high-speed clock signals from interfering with remote sense lines in adjacent layers, and improves EMI performance.

Place an AVIN filter capacitor as close as possible to the ISL91211AIK and ISL91211BIK, but away from noise sources, and reference the GND pad of the decoupling capacitor to a quiet GND plane. The AVIN and AGND pins of the ISL91211AIK and ISL91211BIK should reference to a copper plane.

Do not use plated through-holes when passing the TFBGA pins to lower layers. Renesas recommends using microvias that are staggered if they pass down multiple layers.

The VOUT and RTN lines are sense the output voltage and should be routed directly to the load. Connecting the RTN line to ground away from the load causes a ground error in the output voltage load regulation due to parasitic ground resistance. Also, keep these traces away from switching nodes, which could be phase nodes or high-speed digital signals. Use small low inductance (ESL) capacitors at the load to improve noise immunity and transient response to the ISL91211AIK and ISL91211BIK.

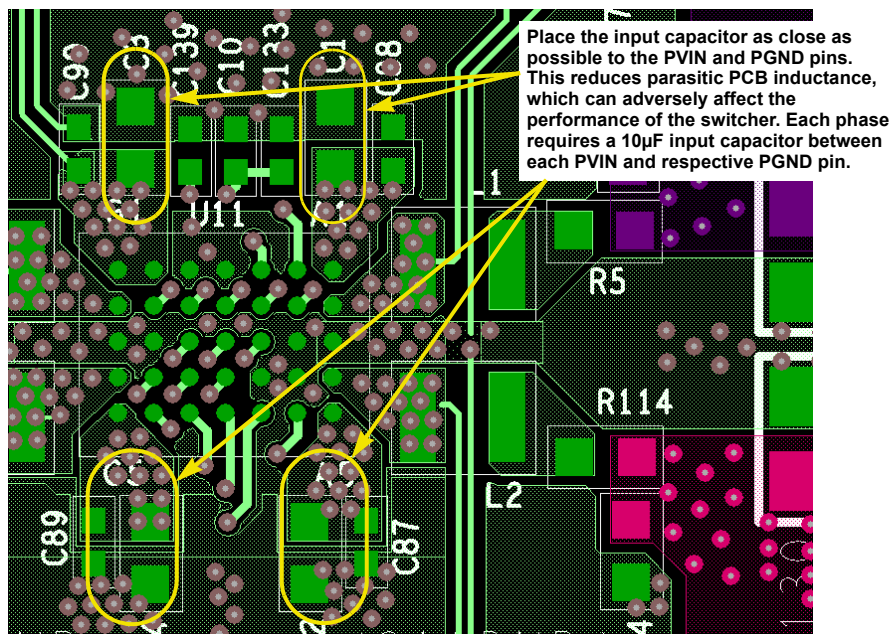


Figure 53. Recommended PCB Layout Top Layer

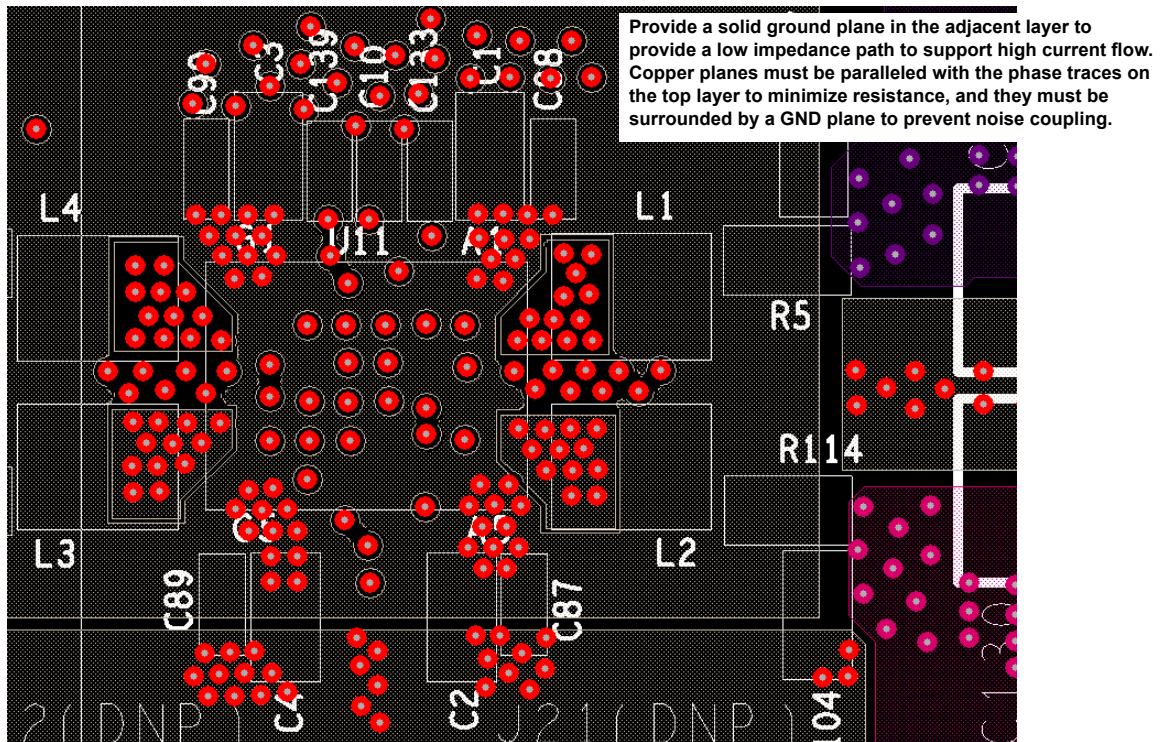


Figure 54. Recommended PCB Layout Second Layer

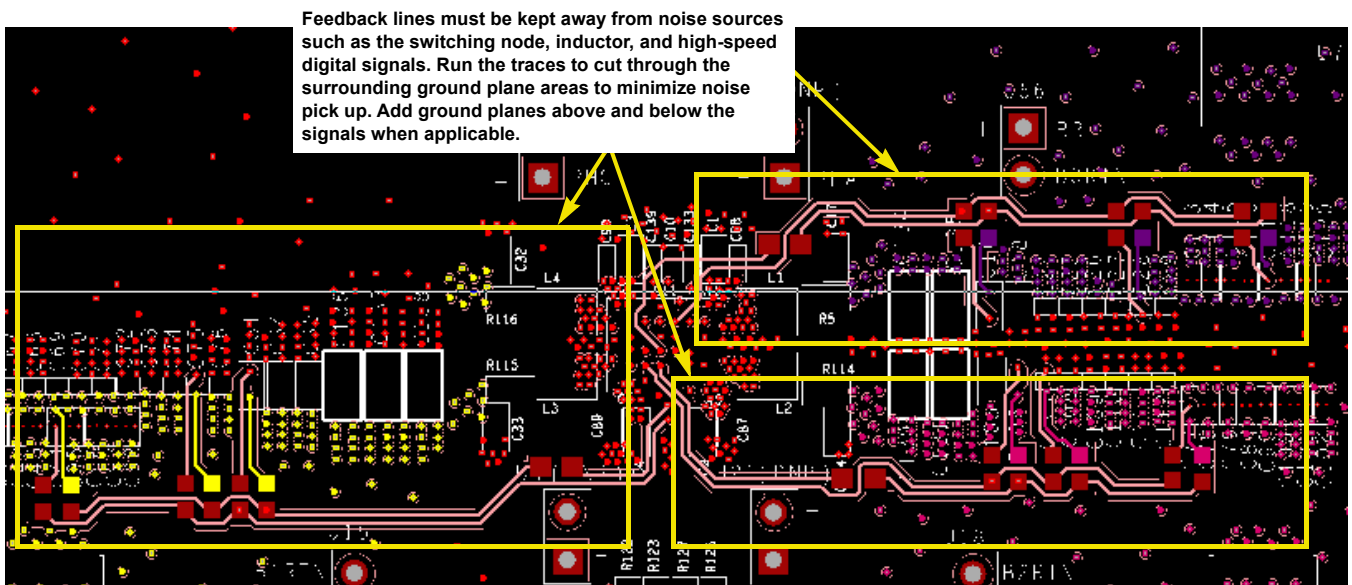


Figure 55. Recommended PCB Layout Bottom Layer

8.1 PCB Layout Summary

- Place input capacitors as close as possible to their respective PVIN and PGND pins.
- Route phase nodes with short, wide traces, and avoid any sensitive nodes.
- Route the VOUT and RTN lines directly to the load using small, low inductance (ESL) capacitors at the load for bypassing.
- Output capacitors should be close to the inductors and have low impedance paths to the PGND pins.
- Keep digital and phase nodes from intersecting the AVIN_FILTER, VOUT, and RTN lines.
- Create a PGND plane on the second layer of the PCB below the power components and bumps carrying high switching currents.

8.2 PCB Design for TFBGA Recommendations

Table 19. PCB Design for TFBGA Recommendations

Design Feature	Design Specification
Cu Pad Diameter	0.8mm pitch: 0.45 ±0.05mm
Microvia Structure	All microvias should be copper filled
Microvia Stacking	Avoid microvia stacking if possible. Use staggered vias instead. If microvia stacking is absolutely necessary for the layout, the maximum number of recommended via stacks is two
Plated Through-Hole (PTH) Location	No PTH should be placed under the BGA bump pads. Use microvias and trace routing to fan the PTH away from the BGA bump array

9. Register Address Map

Address	Register	Address	Register	Address	Register
0x01	IO_CHIPNAME	0x55	BUCK1_RSPCFG0	0x80	BUCK3_DVS2CFG1
0x13	FLT_RECORDTEMP	0x56	BUCK1_EN_DLY	0x81	BUCK3_DVS2CFG0
0x14	FLT_RECORDBUCK1	0x57	BUCK1_SHUTDOWN_DLY	0x82	BUCK3_DVS3CFG1
0x15	FLT_RECORDBUCK2	0x58	BUCK2_EA2	0x83	BUCK3_DVS3CFG0
0x16	FLT_RECORDBUCK3	0x5B	BUCK2_DCM	0x87	BUCK3_DVSSEL
0x17	FLT_RECORDBUCK4	0x5C	BUCK2_CFG3	0x88	BUCK3_RSPCFG1
0x23	IO_SPICFG	0x5D	BUCK2_CFG2	0x89	BUCK3_RSPCFG0
0x24	IO_MODECTRL	0x62	BUCK2_DVS0CFG1	0x8A	BUCK3_EN_DLY
0x32	FLT_MASKTEMP	0x63	BUCK2_DVS0CFG0	0x8B	BUCK3_SHUTDOWN_DLY
0x33	FLT_MASKBUCK1	0x64	BUCK2_DVS1CFG1	0x8C	BUCK4_EA2
0x34	FLT_MASKBUCK2	0x65	BUCK2_DVS1CFG0	0x8F	BUCK4_DCM
0x35	FLT_MASKBUCK3	0x66	BUCK2_DVS2CFG1	0x90	BUCK4_CFG3
0x36	FLT_MASKBUCK4	0x67	BUCK2_DVS2CFG0	0x96	BUCK4_DVS0CFG1
0x3B	BUCK1_EA2	0x68	BUCK2_DVS3CFG1	0x97	BUCK4_DVS0CFG0
0x3E	BUCK1_DCM	0x69	BUCK2_DVS3CFG0	0x98	BUCK4_DVS1CFG1
0x3F	BUCK1_CFG3	0x6D	BUCK2_DVSSEL	0x99	BUCK4_DVS1CFG0
0x46	BUCK1_PHADD	0x6E	BUCK2_RSPCFG1	0x9A	BUCK4_DVS2CFG1
0x48	BUCK1_DVS0CFG1	0x6F	BUCK2_RSPCFG0	0x9B	BUCK4_DVS2CFG0
0x49	BUCK1_DVS0CFG0	0x70	BUCK2_EN_DLY	0x9C	BUCK4_DVS3CFG1
0x4A	BUCK1_DVS1CFG1	0x71	BUCK2_SHUTDOWN_DLY	0x9D	BUCK4_DVS3CFG0
0x4B	BUCK1_DVS1CFG0	0x72	BUCK3_EA2	0xA1	BUCK4_DVSSEL
0x4C	BUCK1_DVS2CFG1	0x75	BUCK3_DCM	0xA3	BUCK4_RSPCFG0
0x4D	BUCK1_DVS2CFG0	0x76	BUCK3_CFG3	0xA2	BUCK4_RSPCFG1
0x4E	BUCK1_DVS3CFG1	0x7C	BUCK3_DVS0CFG1	0xA4	BUCK4_EN_DLY
0x4F	BUCK1_DVS3CFG0	0x7D	BUCK3_DVS0CFG0	0xA5	BUCK4_SHUTDOWN_DLY
0x53	BUCK1_DVSSEL	0x7E	BUCK3_DVS1CFG1		
0x54	BUCK1_RSPCFG1	0x7F	BUCK3_DVS1CFG0		

Note: The registers not listed in the register map and RESERVED bits in the register map are reserved for factory use only. Changing these registers/bits can result in unexpected operation.

10. Register Description by Address

Address	Bit	Name	R/W	Default	Description								
IO_CHIPNAME													
0x01	7:0	IO_CHIPNAME	R	0x03	<table border="1"> <tr> <td colspan="2">Chip Name</td> </tr> <tr> <td>0x03</td> <td>ISL91211AIK and ISL91211BIK</td> </tr> </table>	Chip Name		0x03	ISL91211AIK and ISL91211BIK				
Chip Name													
0x03	ISL91211AIK and ISL91211BIK												
FLT_RECORDTEMP													
0x13	7	FLT_BOOT	R	0x0	<table border="1"> <tr> <td colspan="2">BOOT Occurred</td> </tr> <tr> <td colspan="2">Read only, cleared when read</td> </tr> <tr> <td>0x0</td> <td>No boot process has occurred.</td> </tr> <tr> <td>0x1</td> <td>Boot process has occurred, OTP read is finished.</td> </tr> </table>	BOOT Occurred		Read only, cleared when read		0x0	No boot process has occurred.	0x1	Boot process has occurred, OTP read is finished.
	BOOT Occurred												
	Read only, cleared when read												
0x0	No boot process has occurred.												
0x1	Boot process has occurred, OTP read is finished.												
6:2	RSVD	R	0x0	Reserved									
1	FLT_TEMPSDR	R	0x0	<table border="1"> <tr> <td colspan="2">Over-Temperature (OT) Shutdown (Rising Threshold)</td> </tr> <tr> <td colspan="2">Read only, cleared when read</td> </tr> <tr> <td>0x0</td> <td>No fault, less than threshold.</td> </tr> <tr> <td>0x1</td> <td>Fault, greater than threshold.</td> </tr> </table>	Over-Temperature (OT) Shutdown (Rising Threshold)		Read only, cleared when read		0x0	No fault, less than threshold.	0x1	Fault, greater than threshold.	
Over-Temperature (OT) Shutdown (Rising Threshold)													
Read only, cleared when read													
0x0	No fault, less than threshold.												
0x1	Fault, greater than threshold.												
0	FLT_TEMPSDF	R	0x0	<table border="1"> <tr> <td colspan="2">Over-Temperature (OT) Shutdown (Falling Threshold)</td> </tr> <tr> <td colspan="2">Read only, cleared when read</td> </tr> <tr> <td>0x0</td> <td>No fault, less than threshold.</td> </tr> <tr> <td>0x1</td> <td>Fault, greater than threshold.</td> </tr> </table>	Over-Temperature (OT) Shutdown (Falling Threshold)		Read only, cleared when read		0x0	No fault, less than threshold.	0x1	Fault, greater than threshold.	
Over-Temperature (OT) Shutdown (Falling Threshold)													
Read only, cleared when read													
0x0	No fault, less than threshold.												
0x1	Fault, greater than threshold.												
FLT_RECORDBUCK1													
0x14	7	RSVD	R	0x0	Reserved								
	6	FLT_BUCK1_OC	R	0x0	<table border="1"> <tr> <td colspan="2">Overcurrent (OC) for BUCK1</td> </tr> <tr> <td colspan="2">Read only, cleared when read</td> </tr> <tr> <td>0x0</td> <td>No fault, less than threshold.</td> </tr> <tr> <td>0x1</td> <td>Fault, greater than threshold.</td> </tr> </table>	Overcurrent (OC) for BUCK1		Read only, cleared when read		0x0	No fault, less than threshold.	0x1	Fault, greater than threshold.
	Overcurrent (OC) for BUCK1												
	Read only, cleared when read												
	0x0	No fault, less than threshold.											
0x1	Fault, greater than threshold.												
5	FLT_BUCK1_OV	R	0x0	<table border="1"> <tr> <td colspan="2">Overvoltage (OV)</td> </tr> <tr> <td colspan="2">Read only, cleared when read</td> </tr> <tr> <td>0x0</td> <td>No fault, less than threshold.</td> </tr> <tr> <td>0x1</td> <td>Fault, greater than threshold.</td> </tr> </table>	Overvoltage (OV)		Read only, cleared when read		0x0	No fault, less than threshold.	0x1	Fault, greater than threshold.	
Overvoltage (OV)													
Read only, cleared when read													
0x0	No fault, less than threshold.												
0x1	Fault, greater than threshold.												
4	FLT_BUCK1_UV	R	0x0	<table border="1"> <tr> <td colspan="2">Undervoltage (UV)</td> </tr> <tr> <td colspan="2">Read only, cleared when read</td> </tr> <tr> <td>0x0</td> <td>No fault, less then threshold.</td> </tr> <tr> <td>0x1</td> <td>Fault, greater than threshold.</td> </tr> </table>	Undervoltage (UV)		Read only, cleared when read		0x0	No fault, less then threshold.	0x1	Fault, greater than threshold.	
Undervoltage (UV)													
Read only, cleared when read													
0x0	No fault, less then threshold.												
0x1	Fault, greater than threshold.												
3:0	RSVD	R	0x0	Reserved									

Address	Bit	Name	R/W	Default	Description						
FLT_RECORDBUCK2											
0x15	7	RSVD	R	0x0	See " FLT_RECORDBUCK1 "						
	6	FLT_BUCK2_OC	R	0x0							
	5	FLT_BUCK2_OV	R	0x0							
	4	FLT_BUCK2_UV	R	0x0							
	3:0	RSVD	R	0x0							
FLT_RECORDBUCK3											
0x16	7	RSVD	R	0x0	See " FLT_RECORDBUCK1 "						
	6	FLT_BUCK3_OC	R	0x0							
	5	FLT_BUCK3_OV	R	0x0							
	4	FLT_BUCK3_UV	R	0x0							
	3:0	RSVD	R	0x0							
FLT_RECORDBUCK4											
0x17	7	RSVD	R	0x0	See " FLT_RECORDBUCK1 "						
	6	FLT_BUCK4_OC	R	0x0							
	5	FLT_BUCK4_OV	R	0x0							
	4	FLT_BUCK4_UV	R	0x0							
	3:0	RSVD	R	0x0							
IO_SPICFG											
0x23	7:5	RSVD	R	0x0	Reserved						
	4	IO_IRQ_CMOS	R/W	0x0	<table border="1"> <thead> <tr> <th colspan="2">IRQ Type</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>OD Output</td> </tr> <tr> <td>0x1</td> <td>CMOS Output</td> </tr> </tbody> </table>	IRQ Type		0x0	OD Output	0x1	CMOS Output
	IRQ Type										
	0x0	OD Output									
	0x1	CMOS Output									
3	IO_IRQ_INVERT	R/W	0x1	<table border="1"> <thead> <tr> <th colspan="2">IRQ Polarity</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Active High</td> </tr> <tr> <td>0x1</td> <td>Active Low</td> </tr> </tbody> </table>	IRQ Polarity		0x0	Active High	0x1	Active Low	
IRQ Polarity											
0x0	Active High										
0x1	Active Low										
2:1	RSVD	R	0x0	Reserved							
0	RSVD	R	0x1	Reserved							

Address	Bit	Name	R/W	Default	Description						
IO_MODECTRL											
0x24	7	IO_BUCK1_EN	R/W	0x1	<table border="1"> <tr><td colspan="2">Enable for BUCK1</td></tr> <tr><td>0x0</td><td>Buck1 disabled.</td></tr> <tr><td>0x1</td><td>Buck1 enabled.</td></tr> </table>	Enable for BUCK1		0x0	Buck1 disabled.	0x1	Buck1 enabled.
	Enable for BUCK1										
	0x0	Buck1 disabled.									
	0x1	Buck1 enabled.									
	6	IO_BUCK2_EN	R/W	0x1	<table border="1"> <tr><td colspan="2">Enable for BUCK2</td></tr> <tr><td>0x0</td><td>Buck2 disabled.</td></tr> <tr><td>0x1</td><td>Buck2 enabled.</td></tr> </table>	Enable for BUCK2		0x0	Buck2 disabled.	0x1	Buck2 enabled.
	Enable for BUCK2										
	0x0	Buck2 disabled.									
	0x1	Buck2 enabled.									
5	IO_BUCK3_EN	R/W	0x1	<table border="1"> <tr><td colspan="2">Enable for BUCK3</td></tr> <tr><td>0x0</td><td>Buck3 disabled.</td></tr> <tr><td>0x1</td><td>Buck3 enabled.</td></tr> </table>	Enable for BUCK3		0x0	Buck3 disabled.	0x1	Buck3 enabled.	
Enable for BUCK3											
0x0	Buck3 disabled.										
0x1	Buck3 enabled.										
4	IO_BUCK4_EN	R/W	0x1	<table border="1"> <tr><td colspan="2">Enable for BUCK4</td></tr> <tr><td>0x0</td><td>Buck4 disabled.</td></tr> <tr><td>0x1</td><td>Buck4 enabled.</td></tr> </table>	Enable for BUCK4		0x0	Buck4 disabled.	0x1	Buck4 enabled.	
Enable for BUCK4											
0x0	Buck4 disabled.										
0x1	Buck4 enabled.										
3	RSVD	R	0x0	Reserved							
2	IO_ENVPPULLDOWN	R/W	0x01	<table border="1"> <tr><td colspan="2">Enable for weak Pull-down on EN/VPP Pin</td></tr> <tr><td>0x0</td><td>Weak pull-down disabled.</td></tr> <tr><td>0x1</td><td>Weak pull-down enabled.</td></tr> </table>	Enable for weak Pull-down on EN/VPP Pin		0x0	Weak pull-down disabled.	0x1	Weak pull-down enabled.	
Enable for weak Pull-down on EN/VPP Pin											
0x0	Weak pull-down disabled.										
0x1	Weak pull-down enabled.										
1	RSVD	R	0x0	Reserved							
0	RSVD	R	0x1	Reserved							
FLT_MASKTEMP											
0x32	7	FLT_MASKBOOT	R/W	0x0	<table border="1"> <tr><td colspan="2">Mask IRQ for FLT_BOOT</td></tr> <tr><td>0x0</td><td>IRQ passed to output pin.</td></tr> <tr><td>0x1</td><td>IRQ masked from output pin.</td></tr> </table>	Mask IRQ for FLT_BOOT		0x0	IRQ passed to output pin.	0x1	IRQ masked from output pin.
	Mask IRQ for FLT_BOOT										
	0x0	IRQ passed to output pin.									
	0x1	IRQ masked from output pin.									
6:2	RSVD	R	0x0	Reserved							
1	FLT_MASKEMPSDR	R/W	0x0	<table border="1"> <tr><td colspan="2">Mask IRQ for FLT_TEMPSTR</td></tr> <tr><td>0x0</td><td>IRQ passed to output pin.</td></tr> <tr><td>0x1</td><td>IRQ masked from output pin.</td></tr> </table>	Mask IRQ for FLT_TEMPSTR		0x0	IRQ passed to output pin.	0x1	IRQ masked from output pin.	
Mask IRQ for FLT_TEMPSTR											
0x0	IRQ passed to output pin.										
0x1	IRQ masked from output pin.										
0	FLT_MASKTEMPDF	R/W	0x0	<table border="1"> <tr><td colspan="2">Mask IRQ for FLT_TEMPDF</td></tr> <tr><td>0x0</td><td>IRQ passed to output pin.</td></tr> <tr><td>0x1</td><td>IRQ masked from output pin.</td></tr> </table>	Mask IRQ for FLT_TEMPDF		0x0	IRQ passed to output pin.	0x1	IRQ masked from output pin.	
Mask IRQ for FLT_TEMPDF											
0x0	IRQ passed to output pin.										
0x1	IRQ masked from output pin.										

Address	Bit	Name	R/W	Default	Description															
FLT_MASKBUCK1																				
0x33	7	RSVD	R	0x0	Reserved															
	6	FLT_BUCK1_MASKOC	R/W	0x0	<table border="1"> <tr> <td colspan="3">Mask IRQ for FLT_BUCK1_OC</td> </tr> <tr> <td>0x0</td> <td>IRQ passed to output pin.</td> <td></td> </tr> <tr> <td>0x1</td> <td>IRQ masked from output pin.</td> <td></td> </tr> </table>	Mask IRQ for FLT_BUCK1_OC			0x0	IRQ passed to output pin.		0x1	IRQ masked from output pin.							
	Mask IRQ for FLT_BUCK1_OC																			
	0x0	IRQ passed to output pin.																		
	0x1	IRQ masked from output pin.																		
5	FLT_BUCK1_MASKOV	R/W	0x0	<table border="1"> <tr> <td colspan="3">Mask IRQ for FLT_BUCK1_OV</td> </tr> <tr> <td>0x0</td> <td>IRQ passed to output pin.</td> <td></td> </tr> <tr> <td>0x1</td> <td>IRQ masked from output pin.</td> <td></td> </tr> </table>	Mask IRQ for FLT_BUCK1_OV			0x0	IRQ passed to output pin.		0x1	IRQ masked from output pin.								
Mask IRQ for FLT_BUCK1_OV																				
0x0	IRQ passed to output pin.																			
0x1	IRQ masked from output pin.																			
4	FLT_BUCK1_MASKUV	R/W	0x0	<table border="1"> <tr> <td colspan="3">Mask IRQ for FLT_BUCK1_UV</td> </tr> <tr> <td>0x0</td> <td>IRQ passed to output pin.</td> <td></td> </tr> <tr> <td>0x1</td> <td>IRQ masked from output pin.</td> <td></td> </tr> </table>	Mask IRQ for FLT_BUCK1_UV			0x0	IRQ passed to output pin.		0x1	IRQ masked from output pin.								
Mask IRQ for FLT_BUCK1_UV																				
0x0	IRQ passed to output pin.																			
0x1	IRQ masked from output pin.																			
3:0	RSVD	R	0x0	Reserved																
FLT_MASKBUCK2																				
0x34	7	RSVD	R	0x0	See "FLT_MASKBUCK1"															
	6	FLT_BUCK2_MASKOC	R/W	0x0																
	5	FLT_BUCK2_MASKOV	R/W	0x0																
	4	FLT_BUCK2_MASKUV	R/W	0x0																
	3:0	RSVD	R	0x0																
FLT_MASKBUCK3																				
0x35	7	RSVD	R	0x0	See "FLT_MASKBUCK1"															
	6	FLT_BUCK3_MASKOC	R/W	0x0																
	5	FLT_BUCK3_MASKOV	R/W	0x0																
	4	FLT_BUCK3_MASKUV	R/W	0x0																
	3:0	RSVD	R	0x0																
FLT_MASKBUCK4																				
0x36	7	RSVD	R	0x0	See "FLT_MASKBUCK1"															
	6	FLT_BUCK4_MASKOC	R/W	0x0																
	5	FLT_BUCK4_MASKOV	R/W	0x0																
	4	FLT_BUCK4_MASKUV	R/W	0x0																
	3:0	RSVD	R	0x0																
BUCK1_EA2																				
0x3B	7:6	BUCK1_VOUTFBDIV	R/W	0x0	<p>V_{OUT} feedback divider ratio for the control loop. Should only be changed when the Buck is Disabled (BUCK1_EN = 0).</p> <table border="1"> <thead> <tr> <th></th> <th>Feedback Divider (FBDIV) (%)</th> <th>V_{OUT} Max (V)</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>100</td> <td>1.2</td> </tr> <tr> <td>0x1</td> <td>80</td> <td>1.5</td> </tr> <tr> <td>0x2</td> <td>60</td> <td>2.0</td> </tr> <tr> <td>0x3</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>		Feedback Divider (FBDIV) (%)	V_{OUT} Max (V)	0x0	100	1.2	0x1	80	1.5	0x2	60	2.0	0x3	Reserved	Reserved
		Feedback Divider (FBDIV) (%)	V_{OUT} Max (V)																	
0x0	100	1.2																		
0x1	80	1.5																		
0x2	60	2.0																		
0x3	Reserved	Reserved																		
5:0	RSVD	R/W	N/A	Reserved. Not Available.																

Address	Bit	Name	R/W	Default	Description								
BUCK1_DCM													
0x3E	7:3	Reserved	R	0x0	Reserved								
	2	BUCK1_FCCM	R/W	0x0	<table border="1"> <tr> <td colspan="2">Forced Continuous Conduction Mode</td> </tr> <tr> <td>0x0</td> <td>DCM allowed when load reaches 0A</td> </tr> <tr> <td>0x1</td> <td>Always operate in CCM (Continuous Conduction Mode)</td> </tr> </table>	Forced Continuous Conduction Mode		0x0	DCM allowed when load reaches 0A	0x1	Always operate in CCM (Continuous Conduction Mode)		
	Forced Continuous Conduction Mode												
0x0	DCM allowed when load reaches 0A												
0x1	Always operate in CCM (Continuous Conduction Mode)												
1:0	Reserved	R/W	0x0	Reserved									
BUCK1_CFG3													
0x3F	7:6	BUCK1_FSEL	ORW	0x2	Buck's steady-state switching frequency. <table border="1"> <tr> <td>0x0</td> <td>2MHz</td> </tr> <tr> <td>0x1</td> <td>Reserved</td> </tr> <tr> <td>0x2</td> <td>Reserved</td> </tr> <tr> <td>0x3</td> <td>Reserved</td> </tr> </table>	0x0	2MHz	0x1	Reserved	0x2	Reserved	0x3	Reserved
	0x0	2MHz											
	0x1	Reserved											
0x2	Reserved												
0x3	Reserved												
5:1	RSVD	N/A	N/A	Reserved									
0	RSVD	N/A	N/A	Reserved									
BUCK1_PHADD													
0x46	7:3	RSVD	N/A	0x0	Reserved. Not Available								
	2	BUCK1_MANUALMODE	ORW	0x0	<table border="1"> <tr> <td colspan="2">Automatic Phase Add/Drop Control</td> </tr> <tr> <td>0x0</td> <td>Automatic Phase Add/Drop</td> </tr> <tr> <td>0x1</td> <td>Manual Phase Add/Drop</td> </tr> </table> <p>Note: This functionality is only available in ISL91211AIK.</p>	Automatic Phase Add/Drop Control		0x0	Automatic Phase Add/Drop	0x1	Manual Phase Add/Drop		
	Automatic Phase Add/Drop Control												
0x0	Automatic Phase Add/Drop												
0x1	Manual Phase Add/Drop												
1:0	BUCK1_MANUALPH	ORW	0x2	<table border="1"> <tr> <td colspan="2">Sets the number of active phases when using Manual Phase Add/Drop Mode</td> </tr> <tr> <td>0x1</td> <td>1-phase mode</td> </tr> <tr> <td>0x0, 0x2, 0x3</td> <td>2-phase mode</td> </tr> </table> <p>Note: In Manual Phase Add/Drop mode (BUCK1_MANUALMODE = 0x1) and 2-phase mode (BUCK1_MANUALPH = 0x0 or 0x2 or 0x3), the part operates in Forced CCM 2-phase configuration.</p>	Sets the number of active phases when using Manual Phase Add/Drop Mode		0x1	1-phase mode	0x0, 0x2, 0x3	2-phase mode			
Sets the number of active phases when using Manual Phase Add/Drop Mode													
0x1	1-phase mode												
0x0, 0x2, 0x3	2-phase mode												

Address	Bit	Name	R/W	Default	Description																																				
BUCK1_DVS0CFG1																																									
0x48	7:0	BUCK1_DVS0VOUT92	R/W	TRIM for 0.9V	<p>Upper eight bits of a 10-bit DAC[9:0] value to generate V_{OUT} for DVS Configuration 0.</p> <p>Note: V_{OUT} must be programmed above 0.3V. FBDIV is set by factory OTP to 1x, 0.8x, 0.6x.</p> <table border="1"> <thead> <tr> <th>FBDIV</th> <th>1.0</th> <th>0.8</th> <th>0.6</th> </tr> <tr> <th>DAC</th> <th>V_{OUT} (V)</th> <th>V_{OUT} (V)</th> <th>V_{OUT} (V)</th> </tr> </thead> <tbody> <tr> <td>0x000</td> <td>0.0000</td> <td>0.0000</td> <td>0.0000</td> </tr> <tr> <td>0x001</td> <td>0.0012</td> <td>0.0015</td> <td>0.0020</td> </tr> <tr> <td>...</td> <td></td> <td></td> <td></td> </tr> <tr> <td>0x200</td> <td>0.6144</td> <td>0.768</td> <td>1.024</td> </tr> <tr> <td>0x201</td> <td>0.6156</td> <td>0.7695</td> <td>1.026</td> </tr> <tr> <td>...</td> <td></td> <td></td> <td></td> </tr> <tr> <td>0x3E8</td> <td>1.2</td> <td>1.5</td> <td>2.0</td> </tr> </tbody> </table>	FBDIV	1.0	0.8	0.6	DAC	V_{OUT} (V)	V_{OUT} (V)	V_{OUT} (V)	0x000	0.0000	0.0000	0.0000	0x001	0.0012	0.0015	0.0020	...				0x200	0.6144	0.768	1.024	0x201	0.6156	0.7695	1.026	...				0x3E8	1.2	1.5	2.0
FBDIV	1.0	0.8	0.6																																						
DAC	V_{OUT} (V)	V_{OUT} (V)	V_{OUT} (V)																																						
0x000	0.0000	0.0000	0.0000																																						
0x001	0.0012	0.0015	0.0020																																						
...																																									
0x200	0.6144	0.768	1.024																																						
0x201	0.6156	0.7695	1.026																																						
...																																									
0x3E8	1.2	1.5	2.0																																						
BUCK1_DVS0CFG0																																									
0x49	7:6	BUCK1_DVS0VOUT10	R/W	TRIM for 0.9V	<p>Lower two bits of a 10-bit DAC[9:0] value to generate V_{OUT} for DVS configuration.</p> <p>Note: When DVS Configuration 0 is selected (using pins or registers) any write to BUCK1_DVS0CFG0 causes a DVS ramping to occur.</p> <p>For details, see "Dynamic Voltage Scaling (DVS)" on page 21.</p>																																				
	5	RSVD	R	0x0	Reserved																																				
	4:1	RSVD	R	0x0	Reserved																																				
	0	RSVD	R	0x0	Reserved																																				
BUCK1_DVS1CFG1																																									
0x4A	7:0	BUCK1_DVS1VOUT92	R/W	0xBF	See "BUCK1_DVS0CFG1"																																				
BUCK1_DVS1CFG0																																									
0x4B	7:6	BUCK1_DVS1VOUT10	R/W	0x3	See "BUCK1_DVS0CFG0"																																				
	5	RSVD	R	0x0																																					
	4:1	RSVD	R	0x0																																					
	0	RSVD	R	0x0																																					
BUCK1_DVS2CFG1																																									
0x4C	7:0	BUCK1_DVS2VOUT92	R/W	0x58	See "BUCK1_DVS0CFG1"																																				
BUCK1_DVS2CFG0																																									
0x4D	7:6	BUCK1_DVS2VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"																																				
	5	RSVD	R	0x0																																					
	4:1	RSVD	R	0x0																																					
	0	RSVD	R	0x0																																					
BUCK1_DVS3CFG1																																									
0x4E	7:0	BUCK1_DVS3VOUT92	R/W	0x00	See "BUCK1_DVS0CFG1"																																				

Address	Bit	Name	R/W	Default	Description																																																							
BUCK1_DVS3CFG0																																																												
0x4F	7:6	BUCK1_DVS3VOUT10	R/W	0x0	See " BUCK1_DVS0CFG0 "																																																							
	5	RSVD	R	0x0																																																								
	4:1	RSVD	R	0x0																																																								
	0	RSVD	R	0x0																																																								
BUCK1_DVSSEL																																																												
0x53	7:3	RSVD	R	0x0	Reserved																																																							
	2	BUCK1_DVSCTRL	R/W	0x0	<table border="1"> <tr> <th colspan="2">BUCK1 DVS Control</th> </tr> <tr> <td>0x0</td> <td>Use BUCK1_DVSSELECT to select active DVS configuration.</td> </tr> </table>	BUCK1 DVS Control		0x0	Use BUCK1_DVSSELECT to select active DVS configuration.																																																			
BUCK1 DVS Control																																																												
0x0	Use BUCK1_DVSSELECT to select active DVS configuration.																																																											
1:0	BUCK1_DVSSELECT	R/W	0x0	<table border="1"> <tr> <th colspan="2">BUCK1 DVS Selection</th> </tr> <tr> <td>0x0</td> <td>Use DVS Configuration 0 in BUCK1_DVS0CFG and BUCK1_DVS0VOUT.</td> </tr> <tr> <td>0x1</td> <td>Use DVS Configuration 1 in BUCK1_DVS1CFG and BUCK1_DVS1VOUT.</td> </tr> <tr> <td>0x2</td> <td>Use DVS Configuration 2 in BUCK1_DVS2CFG and BUCK1_DVS2VOUT.</td> </tr> <tr> <td>0x3</td> <td>Use DVS Configuration 3 in BUCK1_DVS3CFG and BUCK1_DVS3VOUT. Note: When BUCK1_DVSCTRL = 0x0 any write to the register BUCK1_DVSSEL causes a DVS ramping event to occur.</td> </tr> </table>		BUCK1 DVS Selection		0x0	Use DVS Configuration 0 in BUCK1_DVS0CFG and BUCK1_DVS0VOUT.	0x1	Use DVS Configuration 1 in BUCK1_DVS1CFG and BUCK1_DVS1VOUT.	0x2	Use DVS Configuration 2 in BUCK1_DVS2CFG and BUCK1_DVS2VOUT.	0x3	Use DVS Configuration 3 in BUCK1_DVS3CFG and BUCK1_DVS3VOUT. Note: When BUCK1_DVSCTRL = 0x0 any write to the register BUCK1_DVSSEL causes a DVS ramping event to occur.																																													
				BUCK1 DVS Selection																																																								
				0x0	Use DVS Configuration 0 in BUCK1_DVS0CFG and BUCK1_DVS0VOUT.																																																							
				0x1	Use DVS Configuration 1 in BUCK1_DVS1CFG and BUCK1_DVS1VOUT.																																																							
				0x2	Use DVS Configuration 2 in BUCK1_DVS2CFG and BUCK1_DVS2VOUT.																																																							
0x3	Use DVS Configuration 3 in BUCK1_DVS3CFG and BUCK1_DVS3VOUT. Note: When BUCK1_DVSCTRL = 0x0 any write to the register BUCK1_DVSSEL causes a DVS ramping event to occur.																																																											
BUCK1_RSPCFG1																																																												
0x54	7	RSVD	R	0x0	Reserved																																																							
	6:4	BUCK1_RSPUP	R/W	0x7	<p>V_{OUT} Ramp Slew Rate RSP = BUCK1_RSPUP[1:0], Ramp Speed FBDIV = BUCK1_VOUTFBDIV[1:0] = (1.0, 0.8, 0.6) Slow = BUCK1_RSPUP[2] = 0 Fast = BUCK1_RSPUP[2] = 1</p> <table border="1"> <thead> <tr> <th colspan="2"></th> <th colspan="2">V_{OUT} Ramp Speed mV/μs</th> </tr> <tr> <th>RSP</th> <th>FBDIV</th> <th>Fast</th> <th>Slow</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>1.0</td> <td>12</td> <td>3</td> </tr> <tr> <td>0x1</td> <td>1.0</td> <td>24</td> <td>6</td> </tr> <tr> <td>0x2</td> <td>1.0</td> <td>58</td> <td>14</td> </tr> <tr> <td>0x3</td> <td>1.0</td> <td>115</td> <td>29</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th colspan="2"></th> <th colspan="2">V_{OUT} Ramp Speed mV/μs</th> </tr> <tr> <th>RSP</th> <th>FBDIV</th> <th>Fast</th> <th>Slow</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>0.8</td> <td>12</td> <td>3</td> </tr> <tr> <td>0x1</td> <td>0.8</td> <td>24</td> <td>6</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th colspan="2"></th> <th colspan="2">V_{OUT} Ramp Speed mV/μs</th> </tr> <tr> <th>RSP</th> <th>FBDIV</th> <th>Fast</th> <th>Slow</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>0.6</td> <td>12</td> <td>3</td> </tr> <tr> <td>0x1</td> <td>0.6</td> <td>24</td> <td>6</td> </tr> </tbody> </table>			V_{OUT} Ramp Speed mV/ μ s		RSP	FBDIV	Fast	Slow	0x0	1.0	12	3	0x1	1.0	24	6	0x2	1.0	58	14	0x3	1.0	115	29			V_{OUT} Ramp Speed mV/ μ s		RSP	FBDIV	Fast	Slow	0x0	0.8	12	3	0x1	0.8	24	6			V_{OUT} Ramp Speed mV/ μ s		RSP	FBDIV	Fast	Slow	0x0	0.6	12	3	0x1	0.6	24
		V_{OUT} Ramp Speed mV/ μ s																																																										
RSP	FBDIV	Fast	Slow																																																									
0x0	1.0	12	3																																																									
0x1	1.0	24	6																																																									
0x2	1.0	58	14																																																									
0x3	1.0	115	29																																																									
		V_{OUT} Ramp Speed mV/ μ s																																																										
RSP	FBDIV	Fast	Slow																																																									
0x0	0.8	12	3																																																									
0x1	0.8	24	6																																																									
		V_{OUT} Ramp Speed mV/ μ s																																																										
RSP	FBDIV	Fast	Slow																																																									
0x0	0.6	12	3																																																									
0x1	0.6	24	6																																																									
3	RSVD	R/W	0x0	Reserved																																																								

Address	Bit	Name	R/W	Default	Description																																																		
	2:0	BUCK1_RSPDN	R/W	0x3	See " BUCK1_RSPUP " for rate definition																																																		
BUCK1_RSPCFG0																																																							
0x55	7	RSVD	R	0x0	Reserved																																																		
	6:4	BUCK1_RSPPUP	R/W	0x7	<p>V_{OUT} Ramp Slew Rate RSP = BUCK1_RSPPUP[1:0], Ramp Speed FBDIV = BUCK1_VOUTFBDIV[1:0] = (1.0, 0.8, 0.6) Slow = BUCK1_RSPPUP[2] = 0 Fast = BUCK1_RSPPUP[2] = 1</p> <table border="1"> <thead> <tr> <th rowspan="2">RSP</th> <th rowspan="2">FBDIV</th> <th colspan="2">V_{OUT} Ramp Speed mV/μs</th> </tr> <tr> <th>Fast</th> <th>Slow</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>1.0</td> <td>6</td> <td>1.2</td> </tr> <tr> <td>0x1</td> <td>1.0</td> <td>12</td> <td>3</td> </tr> <tr> <td>0x2</td> <td>1.0</td> <td>29</td> <td>7.2</td> </tr> <tr> <td>0x3</td> <td>1.0</td> <td>58</td> <td>15</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th rowspan="2">RSP</th> <th rowspan="2">FBDIV</th> <th colspan="2">V_{OUT} Ramp Speed mV/μs</th> </tr> <tr> <th>Fast</th> <th>Slow</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>0.8</td> <td>12</td> <td>3</td> </tr> <tr> <td>0x1</td> <td>0.8</td> <td>24</td> <td>6</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th rowspan="2">RSP</th> <th rowspan="2">FBDIV</th> <th colspan="2">V_{OUT} Ramp Speed mV/μs</th> </tr> <tr> <th>Fast</th> <th>Slow</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>0.6</td> <td>12</td> <td>3</td> </tr> <tr> <td>0x1</td> <td>0.6</td> <td>24</td> <td>6</td> </tr> </tbody> </table>	RSP	FBDIV	V _{OUT} Ramp Speed mV/μs		Fast	Slow	0x0	1.0	6	1.2	0x1	1.0	12	3	0x2	1.0	29	7.2	0x3	1.0	58	15	RSP	FBDIV	V _{OUT} Ramp Speed mV/μs		Fast	Slow	0x0	0.8	12	3	0x1	0.8	24	6	RSP	FBDIV	V _{OUT} Ramp Speed mV/μs		Fast	Slow	0x0	0.6	12	3	0x1	0.6	24	6
					RSP			FBDIV	V _{OUT} Ramp Speed mV/μs																																														
						Fast	Slow																																																
					0x0	1.0	6	1.2																																															
0x1	1.0	12	3																																																				
0x2	1.0	29	7.2																																																				
0x3	1.0	58	15																																																				
RSP	FBDIV	V _{OUT} Ramp Speed mV/μs																																																					
		Fast	Slow																																																				
0x0	0.8	12	3																																																				
0x1	0.8	24	6																																																				
RSP	FBDIV	V _{OUT} Ramp Speed mV/μs																																																					
		Fast	Slow																																																				
0x0	0.6	12	3																																																				
0x1	0.6	24	6																																																				
3	BUCK	R/W	0x0	Reserved																																																			
2:0	BUCK1_RSPPDN	R/W	0x3	See " BUCK1_RSPPUP " for rate definition																																																			
BUCK1_EN_DLY																																																							
0x56	1:0	BUCK1_ENPIN_CFG	R/W	0x0	<p>EN_X pin control is valid only in PINMODE 1. BUCK EN Control = IO_BUCK1_EN and BUCK1_EN_PIN If not in PINMODE 1, BUCK1_EN_PIN is default high, only IO_BUCK1_EN can toggle BUCK1 EN</p> <table border="1"> <thead> <tr> <th colspan="2">BUCK1_EN_PIN</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>EN_A</td> </tr> <tr> <td>0x1</td> <td>EN_B</td> </tr> <tr> <td>0x2</td> <td>EN_C</td> </tr> <tr> <td>0x3</td> <td>1</td> </tr> </tbody> </table>	BUCK1_EN_PIN		0x0	EN_A	0x1	EN_B	0x2	EN_C	0x3	1																																								
	BUCK1_EN_PIN																																																						
0x0	EN_A																																																						
0x1	EN_B																																																						
0x2	EN_C																																																						
0x3	1																																																						
5:0	BUCK1_EN_DLY	R/W	0x0	<p>Delay time from BUCK_EN pin and IO_REGVAID go high to BUCK1_EN control asserted. Delay = (integer value of register) ms [1ms/LSB]</p>																																																			

Address	Bit	Name	R/W	Default	Description										
BUCK1_SHUTDOWN_DLY															
0x57	1:0	BUCK1_DVSPIN_CFG	R/W	0x0	DVS_PIN_X pin control is valid only in PINMODE 3. DVS_1 = 0 DVS_0 = BUCK1_DVS_PIN0 and BUCK1_DVS_CTRL If not in PINMODE 3, DVS_PIN_x function is disabled <table border="1"> <thead> <tr> <th colspan="2">BUCK1_DVS_PIN0</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>EN_A</td> </tr> <tr> <td>0x1</td> <td>EN_B</td> </tr> <tr> <td>0x2</td> <td>EN_C</td> </tr> <tr> <td>0x3</td> <td>1</td> </tr> </tbody> </table>	BUCK1_DVS_PIN0		0x0	EN_A	0x1	EN_B	0x2	EN_C	0x3	1
	BUCK1_DVS_PIN0														
0x0	EN_A														
0x1	EN_B														
0x2	EN_C														
0x3	1														
5:0	BUCK1_SHUTDOWN_DLY	R/W	0x0	Delay time from BUCK_EN pin or IO_REGVAID go low to BUCK1_EN control deasserted. Delay = (integer value of register) ms [1ms/LSB]											
BUCK2_EA2															
0x58	7:6	BUCK2_VOUTFBDIV	R/W	0x0	See "BUCK1_EA2"										
	5:0	RSVD	R/W	N/A											
BUCK2_DCM															
0x5B	7:3	Reserved	R	0x0	Reserved										
	2	BUCK2_FCCM	R/W	0x0	See "BUCK1_DCM"										
	1:0	Reserved	R/W	0x0	Reserved										
BUCK2_CFG3															
0x5C	7:6	BUCK2_FSEL[1:0]	R/W	0x0	See "BUCK1_CFG3"										
	5:0	RSVD	R/W	N/A											
BUCK2_CFG2															
0x5D	7:4	RSVD	R/W	0x8	Reserved										
	3	RSVD	R	TRIM	Reserved										
	2	RSVD	R	0x0	Reserved										
	1:0	PULL_DOWN_DISCHARGE	R/W	0x0	<table border="1"> <thead> <tr> <th colspan="2">VOUT pulldown when BUCK is shut off</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Disable VOUT pulldown</td> </tr> <tr> <td>0x1</td> <td>Enable VOUT pulldown.</td> </tr> </tbody> </table> <p>Applies the weak pull-down feature for all the buck outputs. 1: Weak pull-down resistor is enabled when the buck output is turned off by software and master EN remains asserted. 0: Weak pull-down resistor is disabled when the buck output is turned off by software and master EN remains asserted.</p>	VOUT pulldown when BUCK is shut off		0x0	Disable VOUT pulldown	0x1	Enable VOUT pulldown.				
VOUT pulldown when BUCK is shut off															
0x0	Disable VOUT pulldown														
0x1	Enable VOUT pulldown.														
BUCK2_DVS0CFG1															
0x62	7:0	BUCK2_DVS0VOUT92	R/W	0xBF	See "BUCK1_DVS0VOUT92"										
BUCK2_DVS0CFG0															
0x63	7:6	BUCK2_DVS0VOUT10	R/W	0x3	See "BUCK1_DVS0CFG0"										
	5	RSVD	R	0x0											
	4:1	RSVD	R	0x0											
	0	RSVD	R	0x0											

Address	Bit	Name	R/W	Default	Description
BUCK2_DVS1CFG1					
0x64	7:0	BUCK2_DVS1VOUT92	R/W	0xBF	See "BUCK1_DVS0CFG1"
BUCK2_DVS1CFG0					
0x65	7:6	BUCK2_DVS1VOUT10	R/W	0x3	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK2_DVS2CFG1					
0x66	7:0	BUCK1_DVS2VOUT92	R/W	0x58	See "BUCK1_DVS0CFG1"
BUCK2_DVS2CFG0					
0x67	7:6	BUCK2_DVS2VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK2_DVS3CFG1					
0x68	7:0	BUCK2_DVS3VOUT92	R/W	0x00	See "BUCK1_DVS0CFG1"
BUCK2_DVS3CFG0					
0x69	7:6	BUCK2_DVS3VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK2_DVSSEL					
0x6D	7:3	RSVD	R	0x0	See "BUCK1_DVSSEL"
	2	BUCK1_DVSCTRL	R/W	0x0	
	1:0	BUCK1_DVSSELECT	R/W	0x0	
BUCK2_RSPCFG1					
0x6E	7	RSVD	R	0x0	See "BUCK1_RSPCFG1"
	6:4	BUCK2_RSPUP	R/W	0x7	
	3	RSVD	R	0x0	
	2:0	BUCK2_RSPDN	R/W	0x3	
BUCK2_RSPCFG0					
0x6F	7	RSVD	R	0x0	See "BUCK1_RSPCFG0"
	6:4	BUCK2_RSPPUP	R/W	0x7	
	3	RSVD	R	0x0	
	2:0	BUCK2_RSPPDN	R/W	0x3	
BUCK2_EN_DLY					
0x70	1:0	BUCK2_ENPIN_CFG	R/W	0x1	See "BUCK1_ENPIN_CFG"
	5:0	BUCK2_EN_DLY	R/W	0x0	See "BUCK1_EN_DLY"
BUCK2_SHUTDN_DLY					
0x71	1:0	BUCK2_DVSPIN_CFG	R/W	0x1	See "BUCK1_DVSPIN_CFG"
	5:0	BUCK2_SHUTDN_DLY	R/W	0x0	See "BUCK1_SHUTDN_DLY"

Address	Bit	Name	R/W	Default	Description
BUCK3_EA2					
0x72	7:6	BUCK3_VOUTFBDIV	R/W	0x0	See "BUCK1_EA2"
	5:0	RSVD	R/W	N/A	
BUCK3_DCM					
0x75	7:3	Reserved	R	0x0	Reserved
	2	BUCK3_FCCM	R/W	0x0	See "BUCK1_DCM"
	1:0	Reserved	R/W	0x0	Reserved
BUCK3_CFG3					
0x76	7:6	BUCK3_FSEL[1:0]	R/W	0x0	See "BUCK1_CFG3"
	5:0	RSVD	R/W	N/A	
BUCK3_DVS0CFG1					
0x7C	7:0	BUCK3_DVS0VOUT92	R/W	0xFF	See "BUCK1_DVS0VOUT92"
BUCK3_DVS0CFG0					
0x7D	7:6	BUCK3_DVS0VOUT10	R/W	0x3	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK3_DVS1CFG1					
0x7E	7:0	BUCK3_DVS1VOUT92	R/W	0xBF	See "BUCK1_DVS0CFG1"
BUCK3_DVS1CFG0					
0x7F	7:6	BUCK3_DVS1VOUT10	R/W	0x3	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK3_DVS2CFG1					
0x80	7:0	BUCK3_DVS2VOUT92	R/W	0x58	See "BUCK1_DVS0CFG1"
BUCK3_DVS2CFG0					
0x81	7:6	BUCK3_DVS2VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK3_DVS3CFG1					
0x82	7:0	BUCK3_DVS3VOUT92	R/W	0x00	See "BUCK1_DVS0CFG1"
BUCK3_DVS3CFG0					
0x83	7:6	BUCK3_DVS3VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK3_DVSSEL					
0x87	7:3	RSVD	R	0x0	See "BUCK1_DVSSEL"
	2	BUCK3_DVSCTRL	R/W	0x0	
	1:0	BUCK3_DVSSELECT	R/W	0x0	

Address	Bit	Name	R/W	Default	Description
BUCK3_RSPCFG1					
0x88	7	RSVD	R	0x0	See "BUCK1_RSPCFG1"
	6:4	BUCK3_RSPUP	R/W	0x7	
	3	RSVD	R	0x0	
	2:0	BUCK3_RSPDN	R/W	0x3	
BUCK3_RSPCFG0					
0x89	7	RSVD	R	0x0	See "BUCK1_RSPCFG0"
	6:4	BUCK3_RSPPUP	R/W	0x7	
	3	RSVD	R	0x0	
	2:0	BUCK3_RSPPDN	R/W	0x3	
BUCK3_EN_DLY					
0x8A	1:0	BUCK3_ENPIN_CFG	R/W	0x2	See "BUCK1_ENPIN_CFG"
	5:0	BUCK3_EN_DLY	R/W	0x0	See "BUCK1_EN_DLY"
BUCK3_SHUTDOWN_DLY					
0x8B	1:0	BUCK3_DVSPIN_CFG	R/W	0x2	See "BUCK1_DVSPIN_CFG"
	5:0	BUCK3_SHUTDOWN_DLY	R/W	0x0	See "BUCK1_SHUTDOWN_DLY"
BUCK4_EA2					
0x8C	7:6	BUCK4_VOUTFBDIV	R/W	0x0	See "BUCK1_EA2"
	5:0	RSVD	R/W	N/A	
BUCK4_DCM					
0x8F	7:3	Reserved	R	0x0	Reserved
	2	BUCK4_FCCM	R/W	0x0	See "BUCK1_DCM"
	1:0	Reserved	R/W	0x0	Reserved
BUCK4_CFG3					
0x90	7:6	BUCK4_FSEL[1:0]	R/W	0x0	See "BUCK1_CFG3"
	5:0	RSVD	R/W	N/A	
BUCK4_DVS0CFG1					
0x96	7:0	BUCK4_DVS0VOUT92	R/W	0xFF	See "BUCK1_DVS0VOUT92"
BUCK4_DVS0CFG0					
0x97	7:6	BUCK4_DVS0VOUT10	R/W	0x3	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK4_DVS1CFG1					
0x98	7:0	BUCK4_DVS1VOUT92	R/W	0xBF	See "BUCK1_DVS0CFG1"
BUCK4_DVS1CFG0					
0x99	7:6	BUCK4_DVS1VOUT10	R/W	0x3	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK4_DVS2CFG1					
0x9A	7:0	BUCK4_DVS2VOUT92	R/W	0x58	See "BUCK1_DVS0CFG1"

Address	Bit	Name	R/W	Default	Description
BUCK4_DVS2CFG0					
0x9B	7:6	BUCK4_DVS2VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK4_DVS3CFG1					
0x9C	7:0	BUCK4_DVS3VOUT92	R/W	0x00	See "BUCK1_DVS0CFG1"
BUCK4_DVS3CFG0					
0x9D	7:6	BUCK4_DVS3VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK4_DVSSEL					
0xA1	7:3	RSVD	R	0x0	See "BUCK1_DVSSEL"
	2	BUCK4_DVSCTRL	R/W	0x0	
	1:0	BUCK4_DVSSELECT	R/W	0x0	
BUCK4_RSPCFG1					
0xA2	7	RSVD	R	0x0	See "BUCK1_RSPCFG1"
	6:4	BUCK4_RSPUP	R/W	0x7	
	3	RSVD	R	0x0	
	2:0	BUCK4_RSPDN	R/W	0x3	
BUCK4_RSPCFG0					
0xA3	7	RSVD	R	0x0	See "BUCK1_RSPCFG0"
	6:4	BUCK4_RSPPUP	R/W	0x7	
	3	RSVD	R	0x0	
	2:0	BUCK4_RSPPDN	R/W	0x3	
BUCK4_EN_DLY					
0xA4	1:0	BUCK4_ENPIN_CFG	R/W	0x2	See "BUCK1_ENPIN_CFG"
	5:0	BUCK4_EN_DLY	R/W	0x0	See "BUCK1_EN_DLY"
BUCK4_SHUTDN_DLY					
0xA5	1:0	BUCK4_DVSPIN_CFG	R/W	0x2	See "BUCK1_DVSPIN_CFG"
	5:0	BUCK4_SHUTDN_DLY	R/W	0x0	See "BUCK1_SHUTDN_DLY"

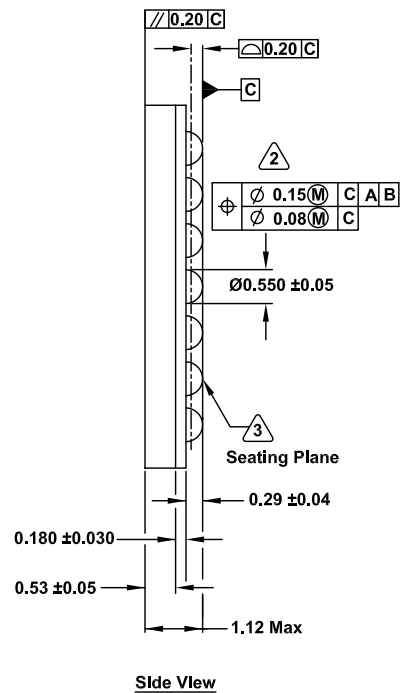
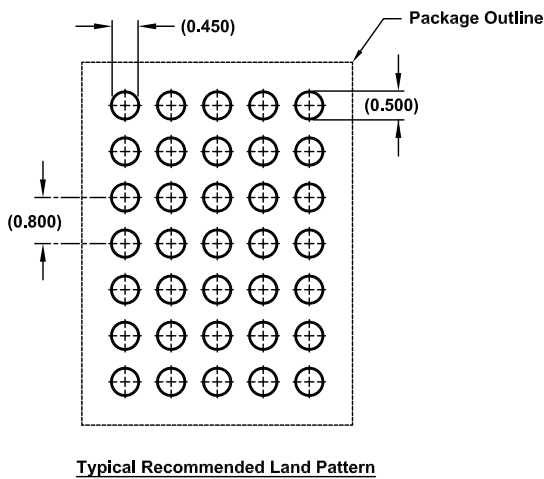
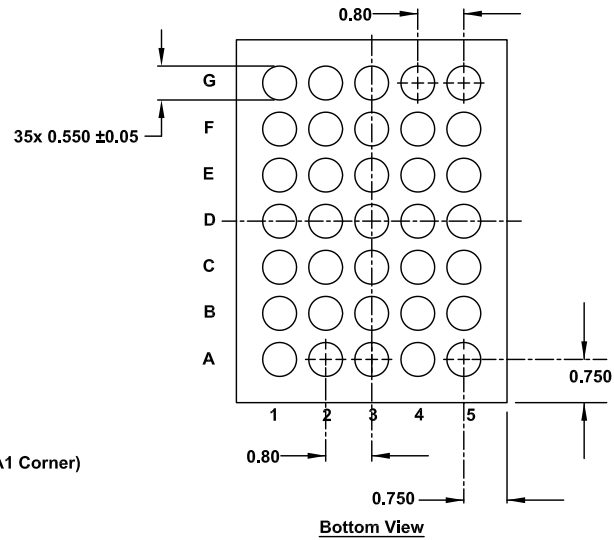
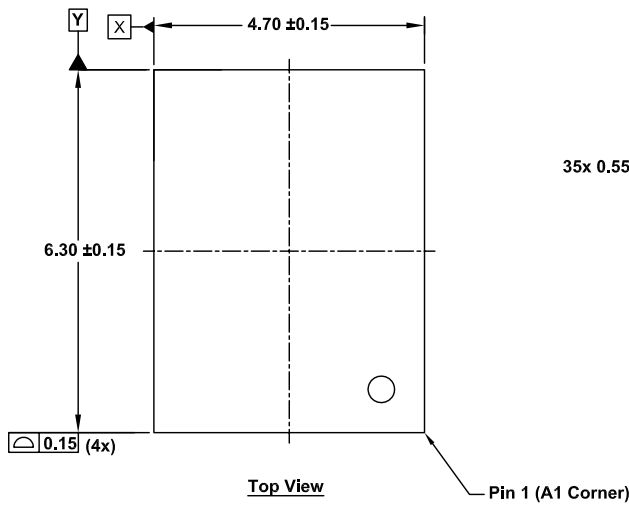
11. Revision History

Rev.	Date	Description
1.02	Feb.25.20	Updated Note 1. Removed Addendum.
1.01	Dec.9.19	Corrected configuration in Addendum for all BIK parts.
1.00	Dec.3.19	Initial release.

12. Package Outline Drawing

For the most recent package outline drawing, see [V35.4.7x6.3](#).

V35.4.7x6.3
 35 Thin Profile Ball Grid Array Package (TFBGA)
 Rev 3, 10/19



- Notes:
- All dimensions and tolerances conform to ASME Y14.5 - 2009.
 - Dimension is measured at the maximum solder ball diameter, parallel to primary datum **C**.
 - Primary datum **C** and seating plane are defined by the spherical crowns of the solder balls.
 - Unless otherwise specified, dimensions are in millimeters.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.