HARRIS SEMICONDUCTOR

IRFF320, IRFF321, IRFF322, IRFF323

2.0A and 2.5A, 350V and 400V, 1.8 and 2.5 Ohm, N-Channel Power MOSFETs

January 1998

Features

- 2.0A and 2.5A, 350V to 400V
- $r_{DS(ON)}$ = 1.8Ω and 2.5Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRFF320	TO-205AF	IRFF320
IRFF321	TO-205AF	IRFF321
IRFF322	TO-205AF	IRFF322
IRFF323	TO-205AF	IRFF323

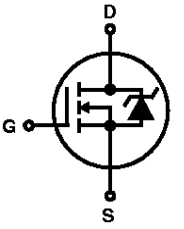
NOTE: When ordering, include the entire part number.

Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

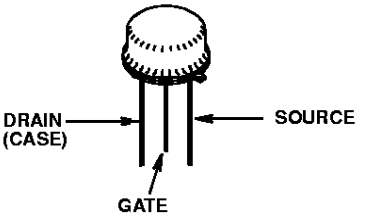
Formerly developmental type TA17404.

Symbol



Packaging

JEDEC TO-205AF



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Copyright © Harris Corporation 1998

File Number **1890.2**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

	IRFF320	IRFF321	IRFF322	IRFF323	UNITS
Drain to Source Voltage (Note 1) . . . . . V_{DS}	400	350	400	350	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1) . . . . . V_{DGR}	400	350	400	350	V
Continuous Drain Current . . . . . I_D	2.5	2.5	2.0	2.0	A
Pulsed Drain Current (Note 3) . . . . . I_{DM}	10	10	8.0	8.0	A
Gate to Source Voltage . . . . . V_{GS}	20	20	20	20	V
Maximum Power Dissipation . . . . . P_D	20	20	20	20	W
Linear Derating Factor	0.16	0.16	0.16	0.16	W/^{o}C
Single Pulse Avalanche Energy Rating (Note 4) . . . . . E_{AS}	100	100	100	100	mJ
Operating and Storage Junction Temperature Range . . . . . T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	^{o}C
Maximum Temperature for Soldering					
Leads at 0.063in (1.6mm) from Case for 10s . . . . . T_L	300	300	300	300	^{o}C
Package Body for 10s, See Techbrief 334 . . . . . T_{pkg}	260	260	260	260	^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

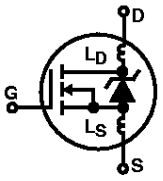
NOTE:

1. $T_J = 25^oC$ to 125^oC.

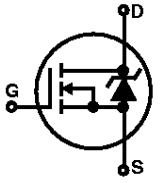
Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA, (Figure 10)				
IRFF320, IRFF322			400	-	-	V
IRFF321, IRFF323			350	-	-	V
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_J = 125^oC$	-	-	250	μA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = 10V, (Figure 7)				
IRFF320, IRFF321			2.5	-	-	A
IRFF322, IRFF323			2.0	-	-	A
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA	2.0	-	4.0	V
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.25A, (Figures 8, 9)				
IRFF320, IRFF321			-	1.5	1.8	Ω
IRFF322, IRFF323			-	1.8	2.5	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, I_D = 1.25A (Figure 12)	1.0	2.0	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 0.5 x Rated BV_{DSS}, $I_D \approx$ 2.5A, R_G = 9.1Ω, V_{GS} = 10V, R_L = 78.2Ω For V_{DSS} = 200V, R_L = 68.2Ω For V_{DSS} = 175V, (Figures 17, 18) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	20	40	ns
Rise Time	t_r		-	25	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	25	50	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = 10V, I_D = 2.5A, V_{DS} = 0.8 x Rated BV_{DSS}, $I_{G(REF)}$ = 1.5mA, (Figures 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature	-	12	15	nC
Gate to Source Charge	Q_{gs}		-	6.0	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	6.0	-	nC

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz, (Figure 11)		-	450	-	pF
Output Capacitance	C_{OSS}			-	100	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	20	-	pF
Internal Drain Inductance	L_D	Measured From the Drain Lead, 5mm (0.2in) From Header to Center of Die	Modified MOSFET Symbol Showing the Internal Device Inductances	-	5.0	-	nH
Internal Source Inductance	L_S	Measured From the Source Lead, 5mm (0.2in) From Header to Source Bonding Pad		-	15	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	6.25	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	175	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Rectifier		-	-	2.5	A
Pulse Source to Drain Current (Note 3)	I_{SDM}			-	-	10	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^oC$, I_{SD} = 2.5A, V_{GS} = 0V, (Figure 13)		-	-	1.6	V
Reverse Recovery Time	t_{rr}	$T_J = 25^oC$, I_{SD} = 2.5A, dI_{SD}/d_t = 100A/μs		-	450	-	ns
Reverse Recovered Charge	Q_{RR}	$T_J = 25^oC$, I_{SD} = 2.5A, dI_{SD}/d_t = 100A/μs		-	3.1	-	μC

NOTES:

2. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive Rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. V_{DD} = 40V, starting $T_J = 25^oC$, L = 29.09mH, R_G = 50Ω, peak I_{AS}= 2.5A (Figures 15, 16).

Typical Performance Curves Unless Otherwise Specified

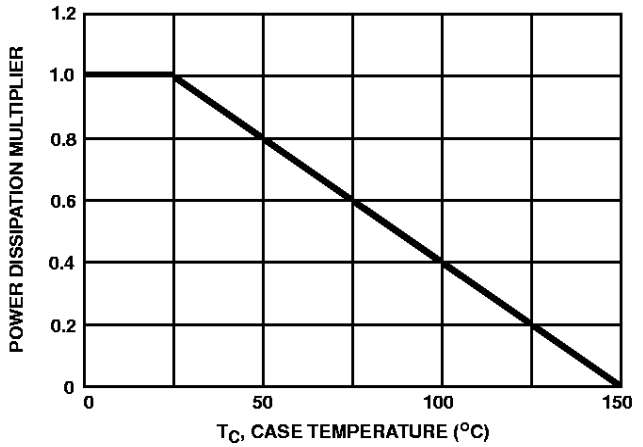


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

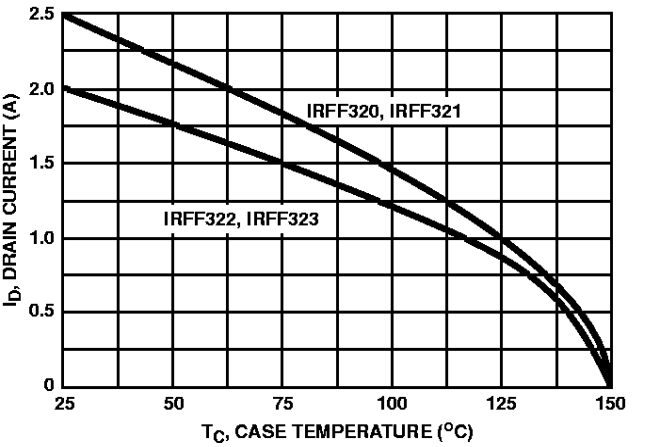


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

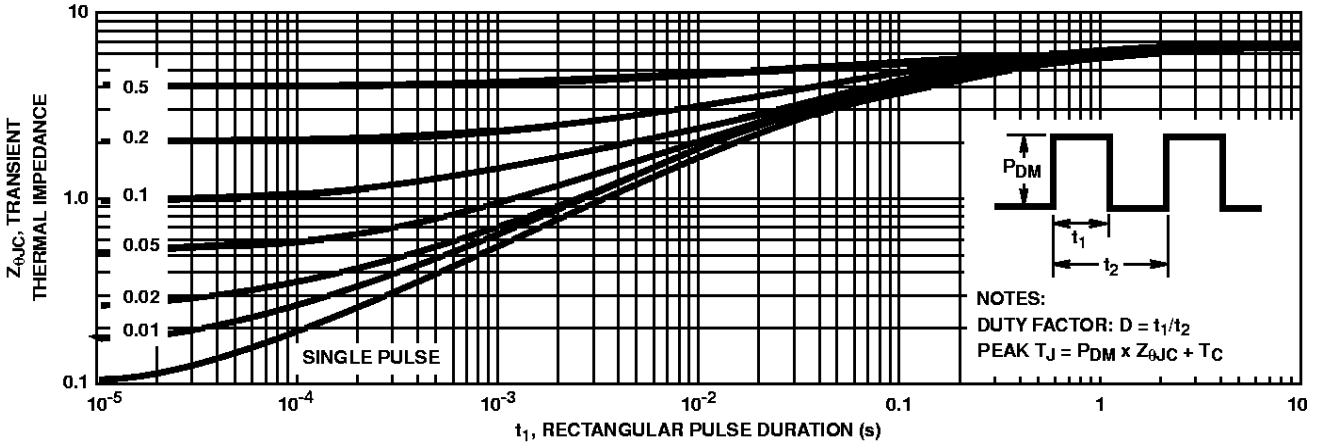


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

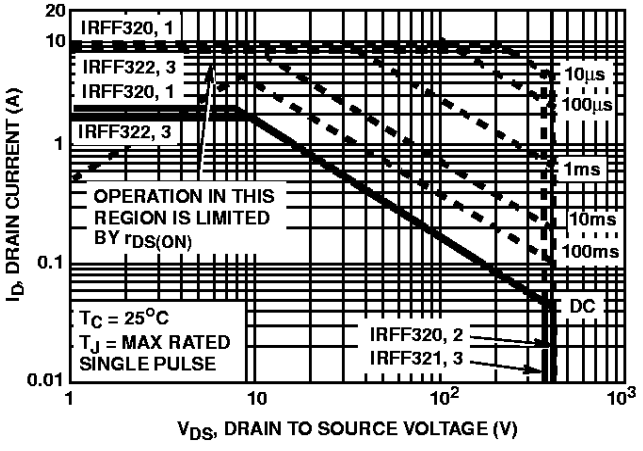


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

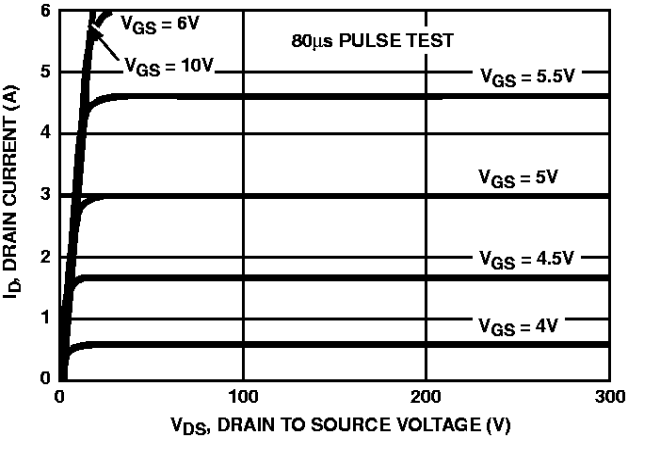


FIGURE 5. OUTPUT CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

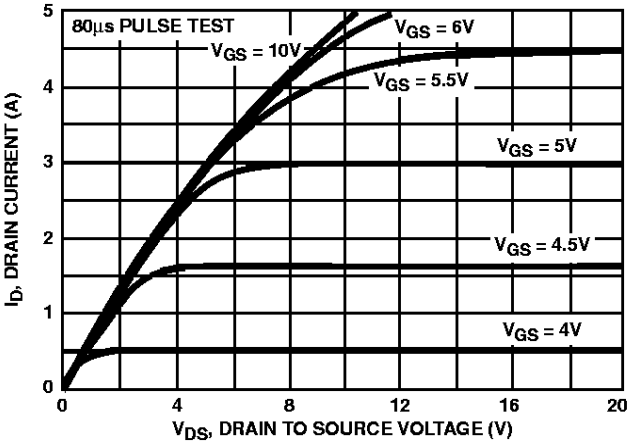


FIGURE 6. SATURATION CHARACTERISTICS

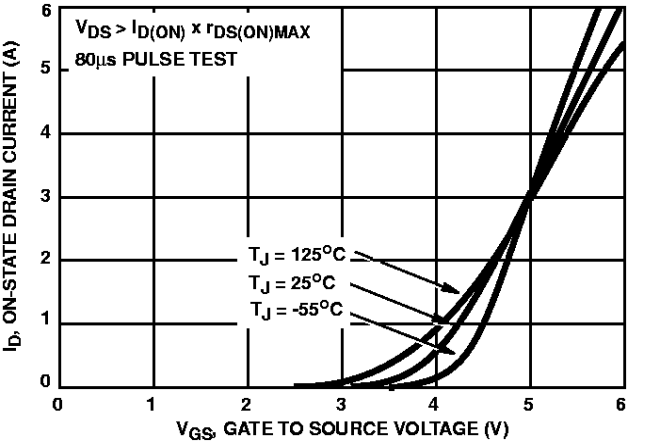
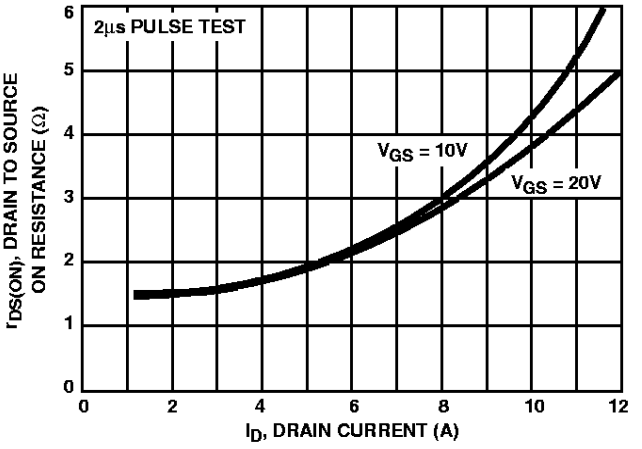


FIGURE 7. TRANSFER CHARACTERISTICS



NOTE: Heating effect of 2μs pulse is minimal.

FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

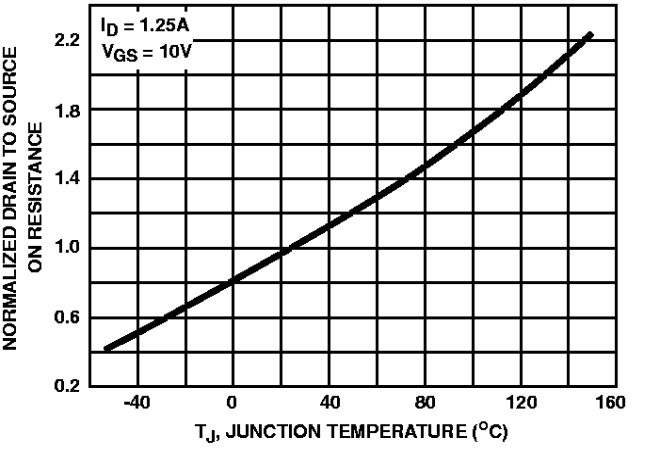


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

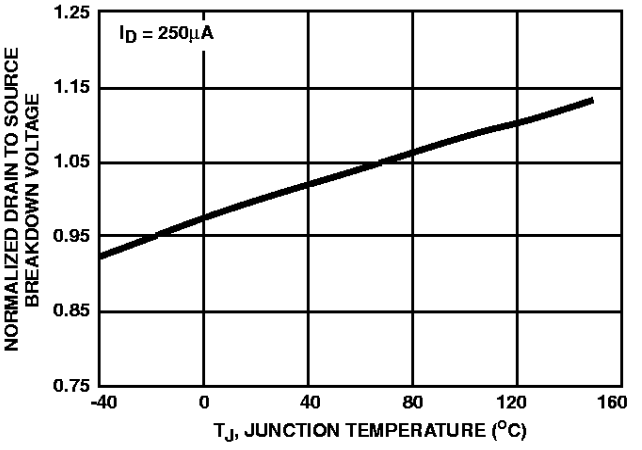


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

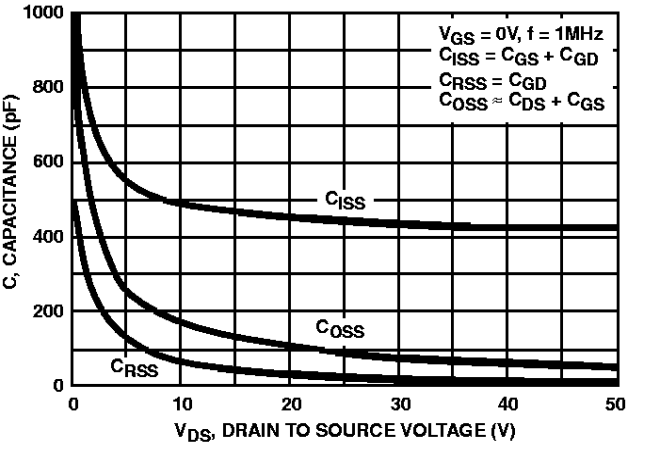


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves Unless Otherwise Specified (Continued)

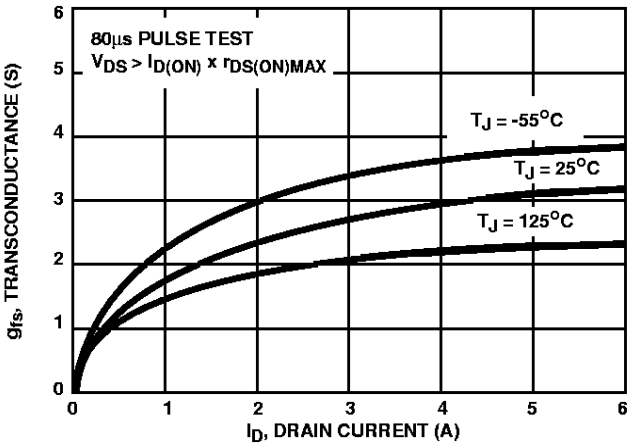


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

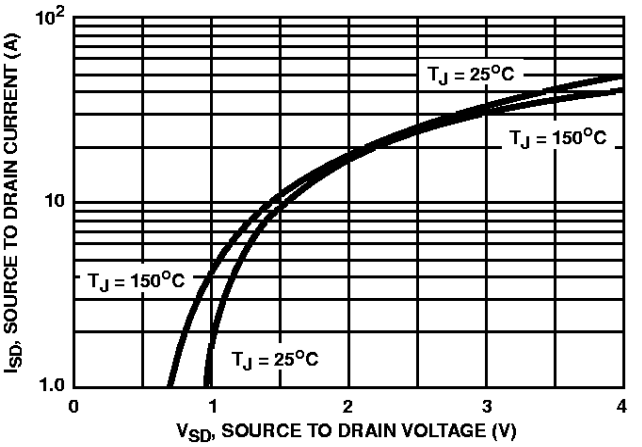


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

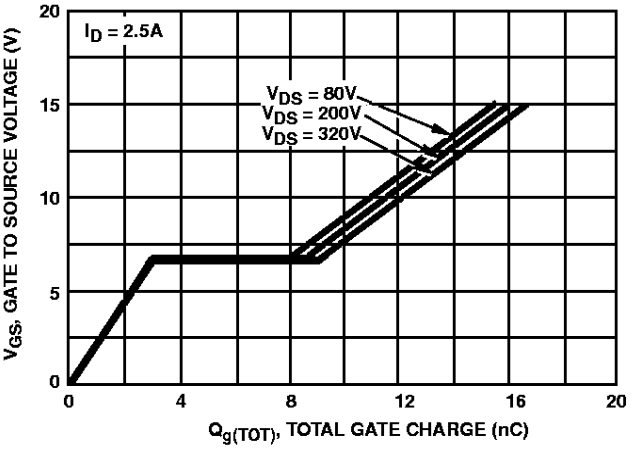


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

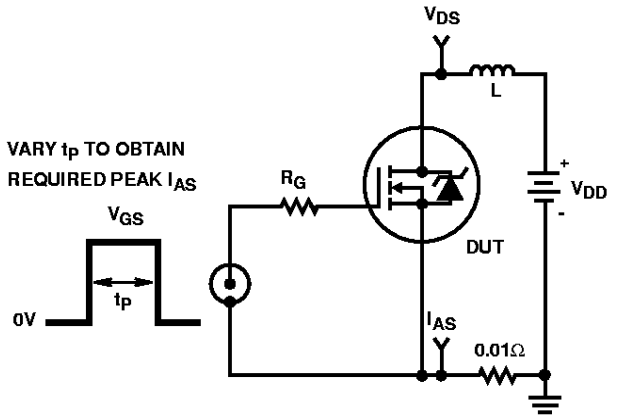


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

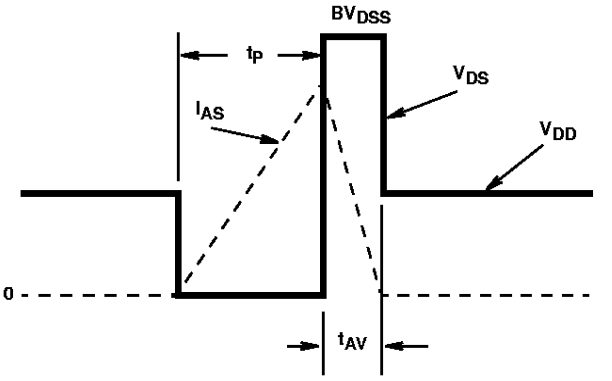


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

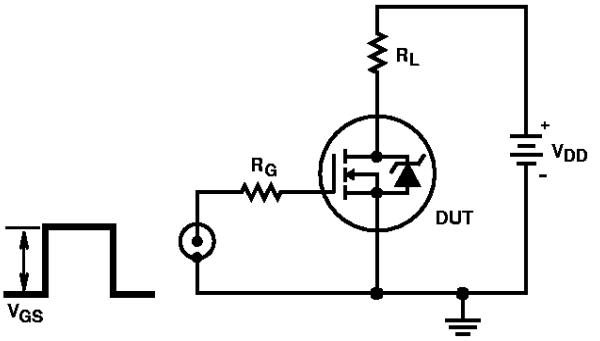


FIGURE 17. SWITCHING TIME TEST CIRCUIT

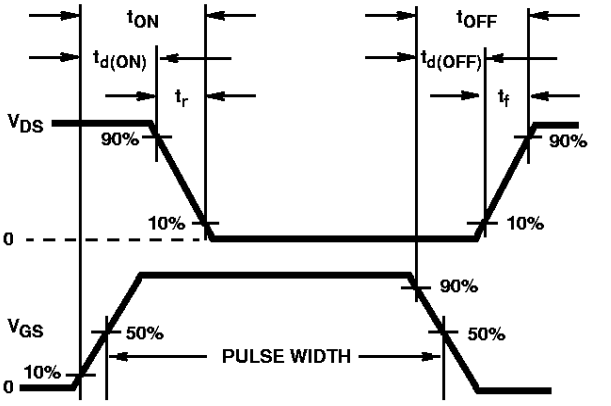


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

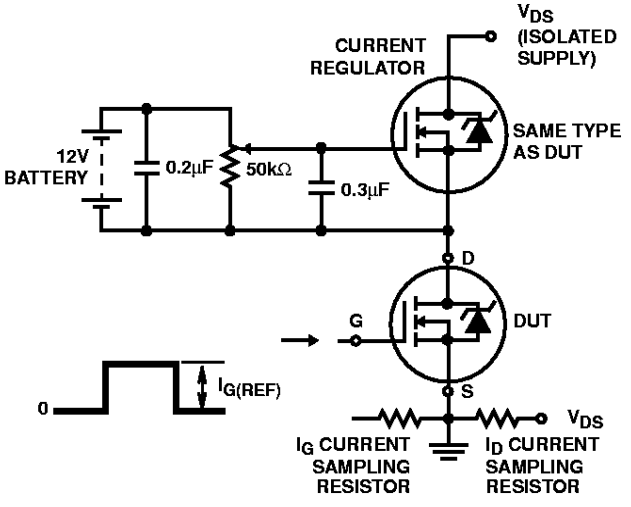


FIGURE 19. GATE CHARGE TEST CIRCUIT

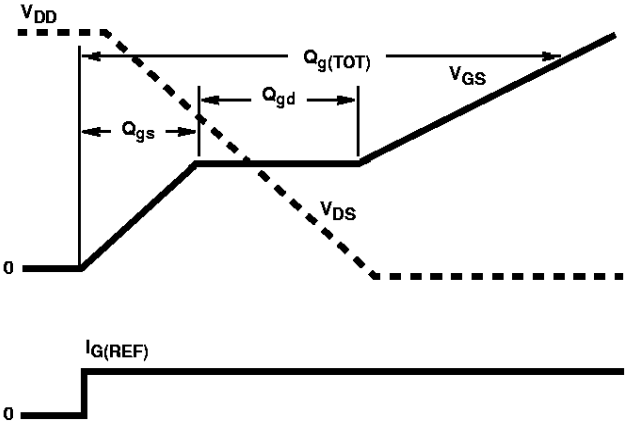


FIGURE 20. GATE CHARGE WAVEFORMS