Features

- ESD protection for one line with bi-direction
- Provide transient protection for the protected line to
  IEC 61000-4-2 (ESD) ±15kV (air) / ±12kV (contact)
  IEC 61000-4-5 (Lightning) 6.5A (8/20μs)
- **Ultra-low capacitance: 0.2pF typical**
- For low operating voltage applications: **2.0V and below**
- **0402 small DFN package** saves board space
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- 2.5G/5G/10GbE
- Thunderbolt interface
- USB3.1 and USB3.0 interfaces
- USB Type-C interface
- DisplayPort interface
- Hand held portable applications

Description

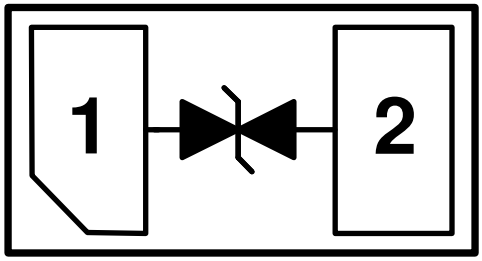
AZ522S-01F is a design which includes a bi-directional ESD rated clamping cell to protect high-speed data interfaces in an electronic system. The AZ522S-01F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD), Lightning, and Cable Discharge Event (CDE).

AZ522S-01F is a unique design which includes proprietary clamping cell with ultra-low capacitance in a small package. During transient conditions, the proprietary clamping cell prevents over-voltage on the control lines, or data lines, protecting any downstream components.

AZ522S-01F is bi-directional and may be used on lines where the signal swings above and below ground.

AZ522S-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



DFN1006P2E (Bottom View)

Specifications

Absolute Maximum Ratings (T_A= 25°C, unless otherwise specified)			
Parameter	**Symbol**	**Rating**	**Unit**
Peak Pulse Current (t_p=8/20μs)	I_{PP} (Note 1)	6.5	A
Operating Voltage	V_{DC}	±2.2	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD-1} V_{ESD-2}	±15 ±12	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STO}	-55 to +150	°C

Electrical Characteristics						
Parameter	**Symbol**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Reverse Stand-Off Voltage	V_{RWM}	T=25 °C.	-2		2	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = ±2V, T=25 °C.			500	nA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C.	5.5		10	V
Surge Clamping Voltage (Note 1)	$V_{CL-surge}$	I_{PP} = 6.5A, t_p = 8/20μs, T=25°C.		5		V
ESD Clamping Voltage (Note 2)	V_{CL-ESD}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), contact mode, T=25 °C.		6.5		V
ESD Dynamic Turn on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+8kV, contact mode, T=25 °C.		0.25		Ω
Channel Input Capacitance	C_{IN}	V_R = 2V, f = 1MHz, T=25 °C.		0.20		pF

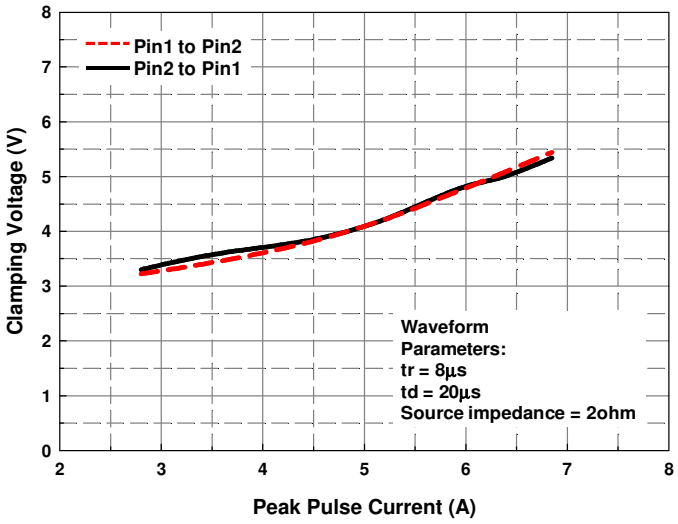
Note 1: The Peak Pulse Current measured conditions: t_p= 8/20μs, 2Ω source impedance.

Note 2: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

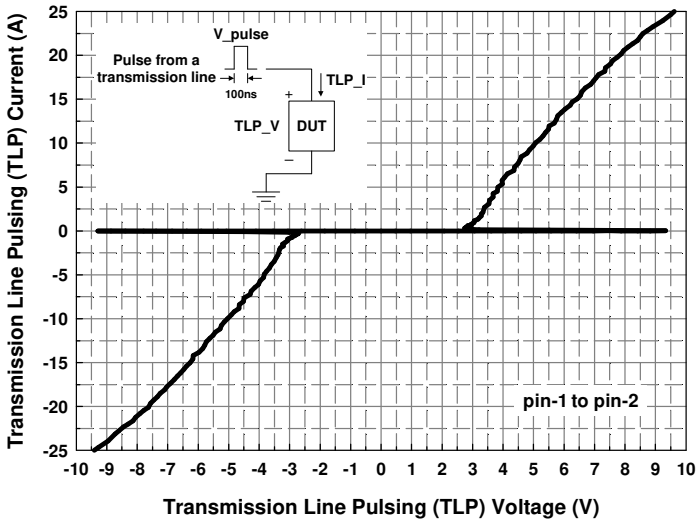
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics

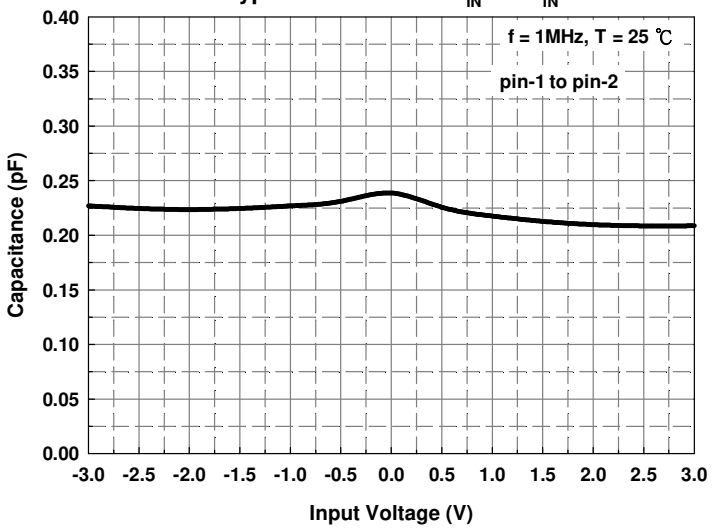
Reverse Clamping Voltage vs. Peak Pulse Current



Transmission Line Pulsing (TLP) Measurement



Typical Variation of C_{IN} vs. V_{IN}



Application Information

The AZ522S-01F is designed to protect one line against system ESD pulse by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ522S-01F is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ522S-01F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ522S-01F.
- Place the AZ522S-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

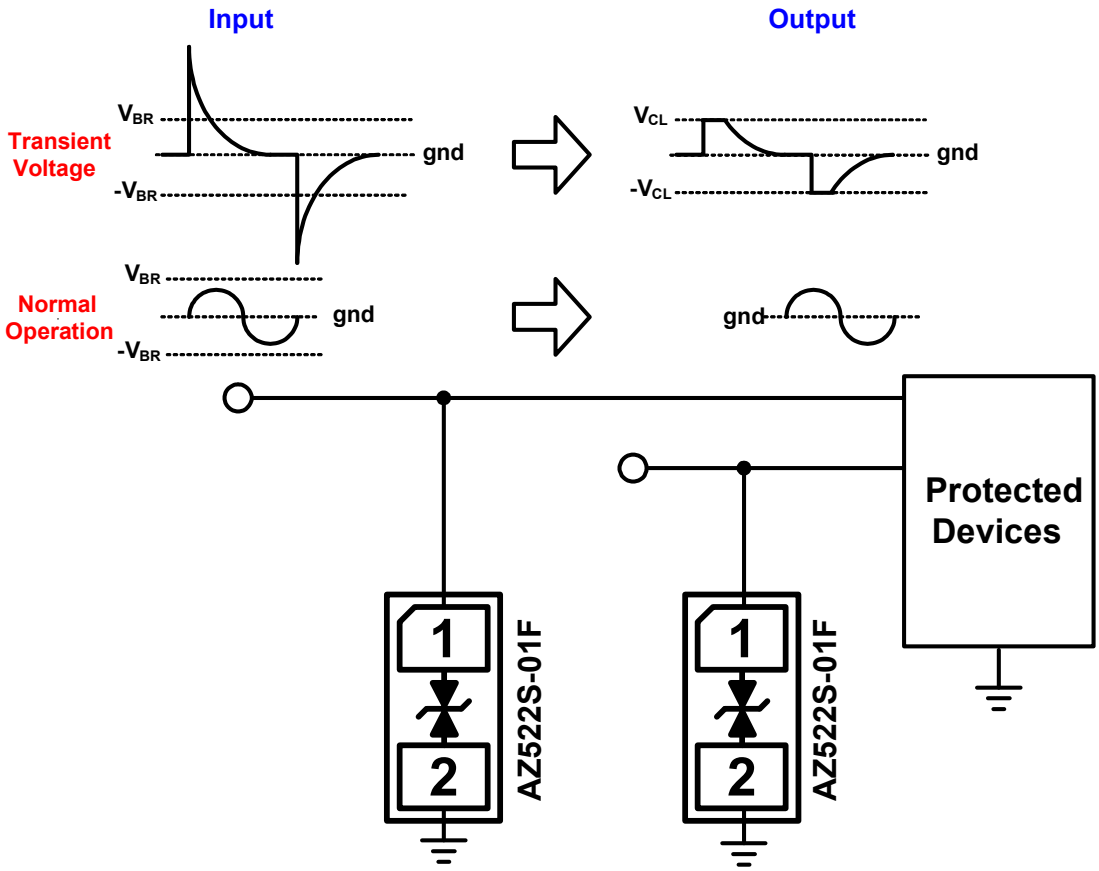
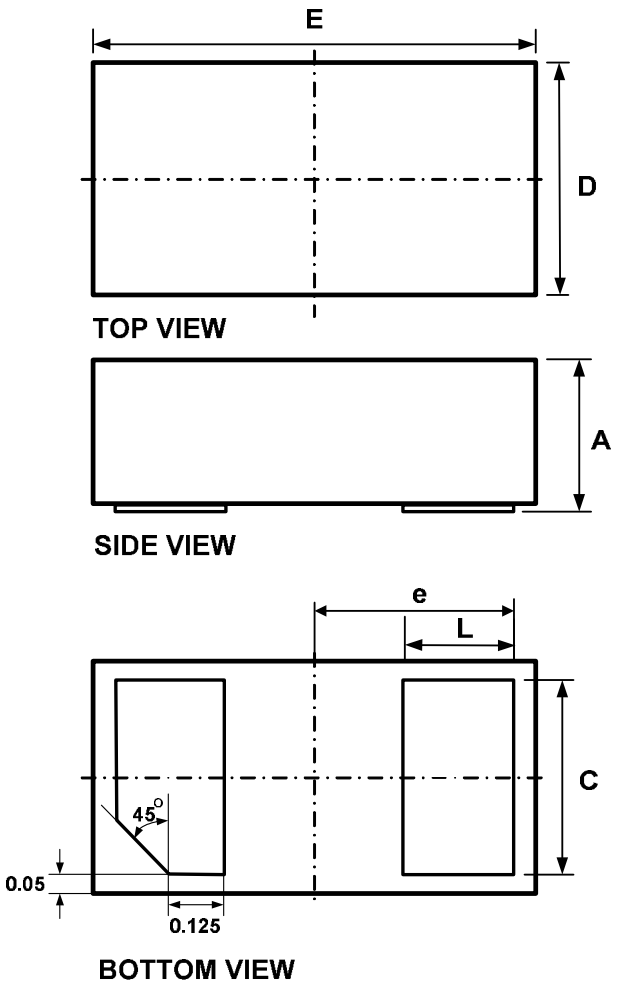


Fig. 1

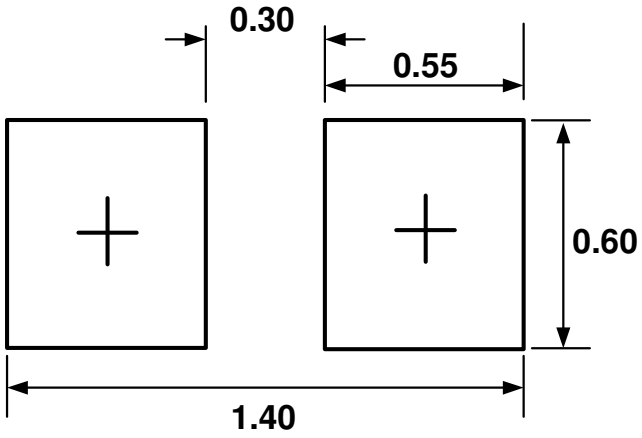
Mechanical Details

DFN1006P2E
PACKAGE DIAGRAMS



Symbol	Millimeters	
	Min.	Max.
E	0.95	1.05
D	0.55	0.65
A	0.45	0.55
e	0.45 BSC	
L	0.20	0.30
C	0.45	0.55

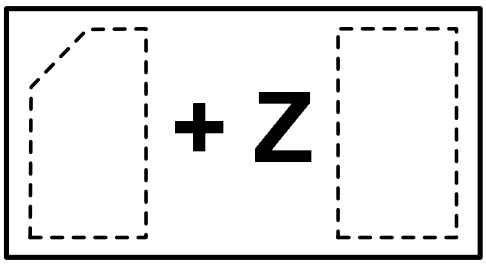
Land Layout



(Unit: mm)

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

Marking Code



Top View

Z = Device Code

Part Number	Marking Code
AZ522S-01F.R7GR (Green Part)	Z

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ522S-01F.R7GR	Green	T/R	7 inch	12,000/reel	4 reels= 48,000/box	6 boxes =288,000/carton

Revision History

Revision	Modification Description
Revision 2020/03/31	Formal Release.