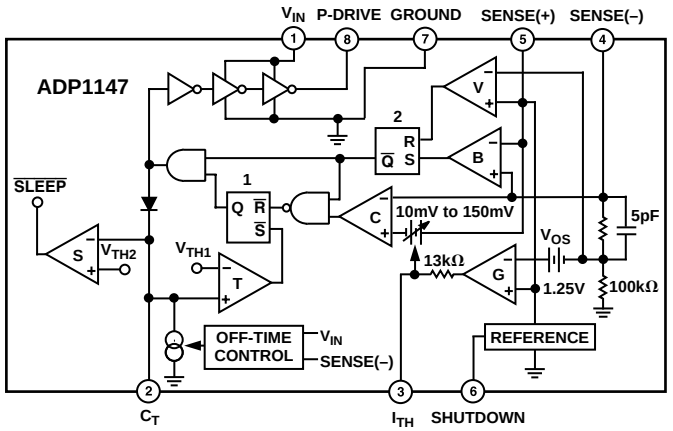
High Efficiency Step-Down Switching Regulator Controllers

ADP1147-3.3/ADP1147-5

FEATURES
Greater Than 95% Efficiency
Current Mode Switching Architecture Provides Superior Load and Line Transient Response
Wide Input Voltage Range 3.5 V* to 16 V
User Defined Current Limit
Short Circuit Protection
Shutdown Pin
Low Dropout Voltage
Low Standby Current 160 μA typ
Low Cost
Available in 8-Lead PDIP or 8-Lead SOIC

APPLICATIONS
Portable Computers
Modems
Cellular Telephones
Portable Equipment
GPS Systems
Handheld Instruments

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP1147 is part of a family of High Efficiency Step-Down Switching Regulators. These regulators offer superior load and line transient response, a user defined current limit and an automatic power savings mode. The automatic power savings mode is used to maintain efficiency at lower output currents. The ADP1147 incorporates a constant off-time, current mode switching architecture to drive an external P-channel MOSFET at frequencies up to 250 kHz. Constant off-time switching generates a constant ripple current in the external inductor. This results in a wider input voltage operating range of 3.5 V* to 16 V, and a less complex circuit design.

*3.5 volt operation is for the ADP1147-3.3.

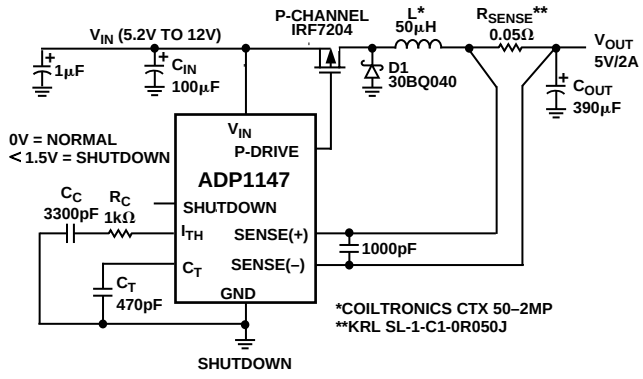


Figure 1. High Efficiency Step-Down Converter (Typical Application)

A very low dropout voltage with excellent output regulation can be obtained by minimizing the dc resistance of the Inductor, the R_{SENSE} resistor, and the $R_{DS(ON)}$ of the P-MOSFET. The power savings mode conserves power by reducing switching losses at lower output currents. When the output load current falls below the minimum required for the continuous mode the ADP1147 will automatically switch to the power savings mode. It will remain in this mode until the inductor requires additional current or the sleep mode is entered. In sleep mode with no load the standby power consumption of the device is reduced to 2.0 mW typical at V_{IN} = 10 V.

For designs requiring even greater efficiencies refer to the ADP1148 data sheet.

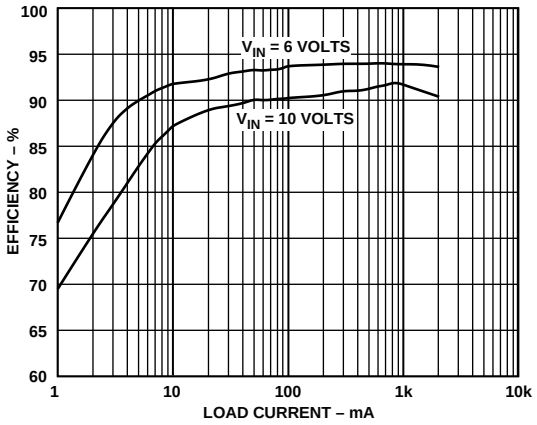


Figure 2. ADP1147-5 Typical Efficiency, Figure 1 Circuit

REV. 0

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ADP1147-3.3/ADP1147-5–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le +70°C$[1], V_{IN} = 10 V, $V_{SHUTDOWN}$ = 0 V unless otherwise noted)

Parameter	Conditions	V_S	ADP1147 Min	Typ	Max	Units
REGULATED OUTPUT VOLTAGE	V_{IN} = 9 V	V_{OUT}				
ADP1147-3-3	I_{LOAD} = 700 mA		3.23	3.33	3.43	V
ADP1147-5	I_{LOAD} = 700 mA		4.90	5.05	5.20	V
OUTPUT VOLTAGE LINE REGULATION	T_A = +25°C	ΔV_{OUT}				
	V_{IN} = 7 V to 12 V,					
	I_{LOAD} = 50 mA		–40	0	+40	mV
OUTPUT VOLTAGE LOAD REGULATION						
ADP1147-3.3	5 mA < I_{LOAD} < 2 A	ΔV_{OUT}		40	65	mV
ADP1147-5	5 mA < I_{LOAD} < 2 A			60	100	mV
Sleep Mode Output Ripple	T_A = +25°C, I_{LOAD} = 0 A			50		mV p-p
INPUT DC SUPPLY CURRENT[2]	T_A = +25°C					
Normal Mode	4 V < V_{IN} < 16 V	I_Q		1.6	2.3	mA
Sleep Mode (ADP1147-3.3)	4 V < V_{IN} < 16 V			160	250	µA
Sleep Mode (ADP1147-5)	4 V < V_{IN} < 16 V			160	250	µA
Shutdown	$V_{SHUTDOWN}$ = 2.1 V, 4 V < V_{IN} < 16 V			10	22	µA
CURRENT SENSE THRESHOLD VOLTAGE						
ADP1147-3.3	$V_{SENSE}(-) = V_{OUT}^+$ 100 mV (Forced)					
	T_A = +25°C			10		mV
	$V_{SENSE}(-) = V_{OUT}^-$ 100 mV (Forced)	$V_5–V_4$	120	150	170	mV
ADP1147-5	$V_{SENSE}(-) = V_{OUT}^+$ 100 mV (Forced)					
	T_A = +25°C			10		mV
	$V_{SENSE}(-) = V_{OUT}^-$ 100 mV (Forced)		120	150	170	mV
SHUTDOWN PIN THRESHOLD	T_A = +25°C	V_6	0.6	0.8	2	V
SHUTDOWN PIN INPUT CURRENT	0 V < $V_{SHUTDOWN}$ < 8 V, V_{IN} = 16 V	I_6		1.2	5	µA
	T_A = +25°C					
C_T PIN DISCHARGE CURRENT	T_A = +25°C, V_{OUT} in Regulation,		50	70	90	µA
	$V_{SENSE}(-) = V_{OUT}$, V_{OUT} = 0 V	I_2		2	10	µA
OFF-TIME	C_T = 390 pF, I_{LOAD} = 700 mA	t_{OFF}	4	5	6	µs
DRIVER OUTPUT TRANSITION TIMES	T_A = +25°C					
	C_L = 3000 pF (Pin 8) V_{IN} = 6 V	tr, tf		100	200	ns

NOTES

[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

[2]Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pin 1) . . . . . 16 V to –0.3 V
Continuous Output Current (Pin 8) . . . . . 50 mA
Sense Voltages (Pins 4, 5) . . . . . 10 V to –0.3 V
Operating Ambient Temperature Range . . . . . 0°C to +70°C
Extended Commercial Temperature Range . . –40°C to +85°C
Junction Temperature* . . . . . +150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

*T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the following formulas: ADP1147AN-3.3, ADP1147AN-5: $T_J = T_A + (P_D \times 110°C/W)$. ADP1147AR-3.3, ADP1147AR-5: $T_J = T_A + (P_D \times 150°C/W)$.

ORDERING GUIDE

Model	Output Voltage	Package Description	Package Option
ADP1147AN-3.3	3.3 V	Plastic DIP	N-8
ADP1147AR-3.3	3.3 V	SOIC	SO-8
ADP1147AN-5	5 V	Plastic DIP	N-8
ADP1147AR-5	5 V	SOIC	SO-8

ELECTRICAL CHARACTERISTICS ($-40°C \le T_A \le +85°C$[1], V_{IN} = 10 V, unless otherwise noted)

Parameter	Conditions	V_S	ADP1147 Min	Typ	Max	Units
REGULATED OUTPUT VOLTAGE	V_{IN} = 9 V					
ADP1147-3.3	I_{LOAD} = 700 mA	V_{OUT}	3.17	3.33	3.4	V
ADP1147-5	I_{LOAD} = 700 mA		4.85	5.05	5.2	V
INPUT DC SUPPLY CURRENT						
Normal Mode	4 V < V_{IN} < 16 V	I_Q		1.6	2.6	mA
Sleep Mode (ADP1147-3.3)	4 V < V_{IN} < 16 V			160	280	µA
Sleep Mode (ADP1147-5)	5 V < V_{IN} < 16 V			160	280	µA
Shutdown	$V_{SHUTDOWN}$ = 2.1 V, 4 V < V_{IN} < 16 V			10	28	µA
CURRENT SENSE THRESHOLD VOLTAGE						
ADP1147-3.3	$V_{SENSE}(-) = V_{OUT}^+$ 100 mV (Forced)	$V_5–V_4$				
	T_A = +25°C			25		mV
	$V_{SENSE}(-) = V_{OUT}^-$ 100 mV (Forced)		120	150	175	mV
ADP1147-5	$V_{SENSE}(-) = V_{OUT}^+$ 100 mV (Forced)					
	T_A = +25°C			25		mV
	$V_{SENSE}(-) = V_{OUT}^-$ 100 mV (Forced)		120	150	175	mV
SHUTDOWN PIN THRESHOLD		V_6	0.55	0.8	2	V
OFF-TIME	C_T = 390 pF, I_{LOAD} = 700 mA	t_{OFF}	3.8	5	6	µs

NOTES
[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

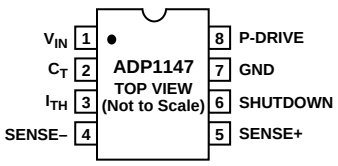
Specifications subject to change without notice.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	V_{IN}	Input Voltage.
2	C_T	External Capacitor Connection. This capacitor sets the operating frequency of the device. The frequency is also dependent on the input voltage level.
3	I_{TH}	Error Amplifier Decoupling Pin. Pin 3 voltage level causes the comparator current threshold to increase.
4	SENSE(–)	This connects to internal resistive divider, which senses the output voltage. Pin 4 is also the (–) input for the current comparator.
5	SENSE(+)	This provides the + input to the current comparator. The offset between Pins 4 and 5 together with R_{SENSE} establish the current trip threshold.
6	SHUTDOWN	When this pin is pulled high, it keeps the MOSFET turned off. When the pin is pulled to ground, the ADP1147 functions normally. This pin cannot be left floating.
7	GND	Independent ground lines must be connected separately to (a) the negative pin of C_{OUT} and (b) the cathode of the Schottky diode and the negative terminal of C_{IN}.
8	P-DRIVE	Provides high current drive for the MOSFET. Voltage swing is from V_{IN} to ground at this pin.

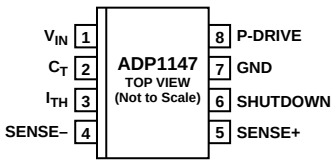
PIN CONFIGURATIONS

8-Lead Plastic DIP (N-8)



T_{JMAX} = 125°C, θ_{JA} = 110°C/W

8-Lead SOIC (SO-8)



T_{JMAX} = 125°C, θ_{JA} = 150°C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP1147 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

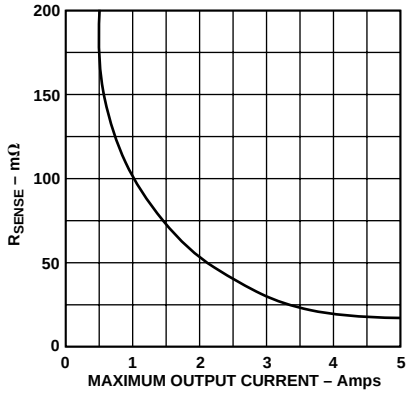


Figure 3. Selecting R_{SENSE} vs. Maximum Output Current

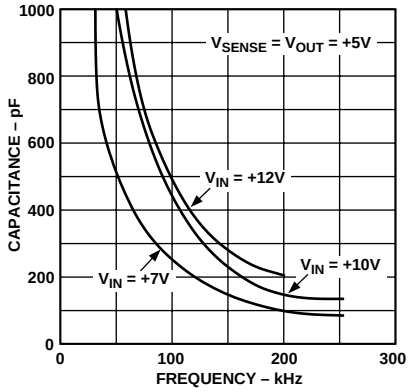


Figure 4. Operating Frequency vs. Timing Capacitor

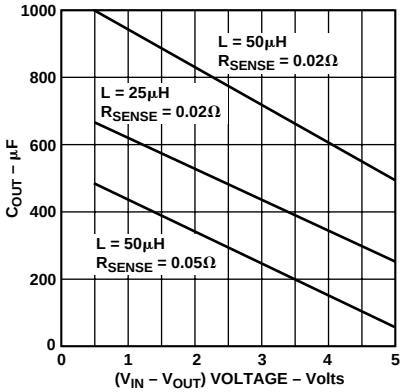


Figure 5. Selecting Minimum Output Capacitor vs. ($V_{IN} – V_{OUT}$) and Inductor

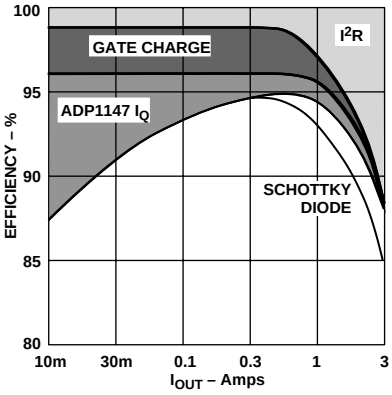


Figure 6. Typical Efficiency Losses

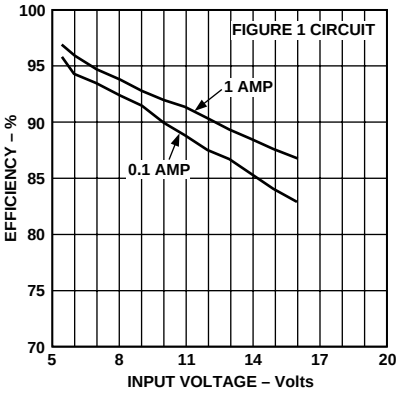


Figure 7. Efficiency vs. Input Voltage

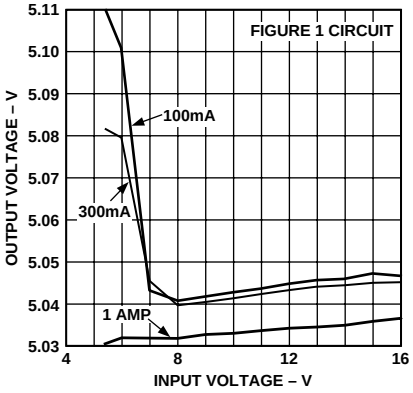


Figure 8. ADP1147-5 Output Voltage vs. Input Voltage

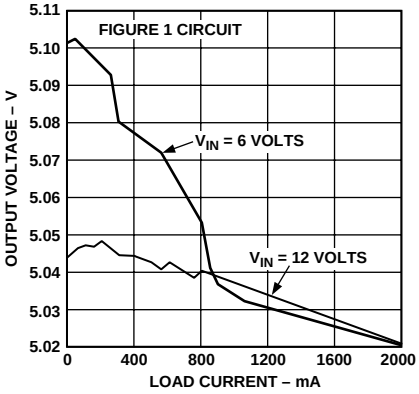


Figure 9. Load Regulation

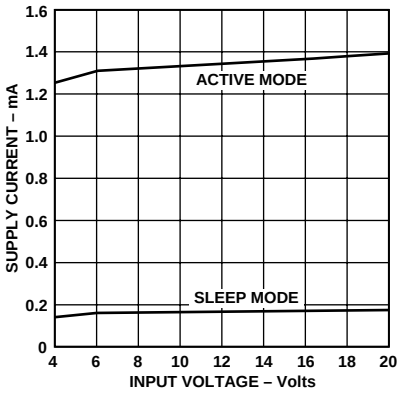


Figure 10. DC Supply Current

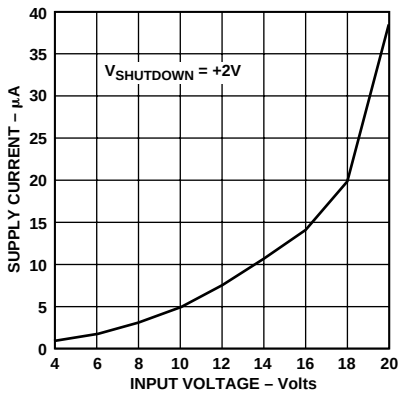


Figure 11. Supply Current in Shutdown

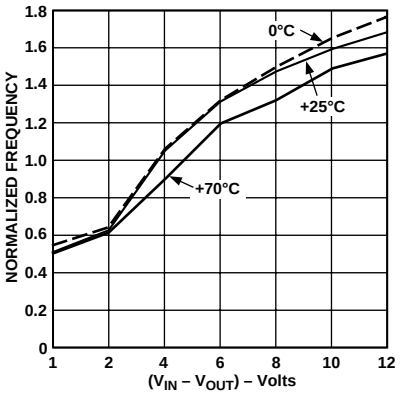


Figure 12. Operating Frequency vs. (V_{IN}–V_{OUT})

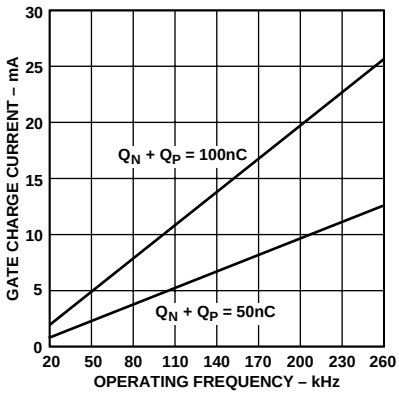


Figure 13. Gate Charge Supply Current

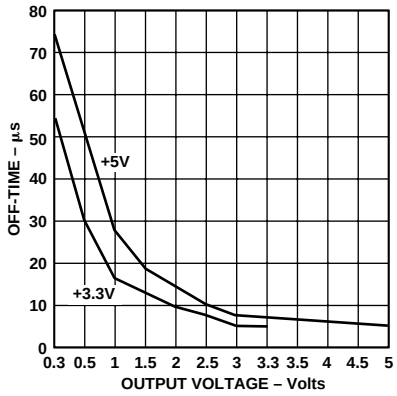


Figure 14. Off-Time vs. V_{OUT}

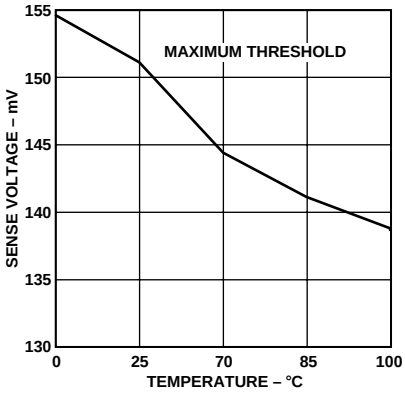


Figure 15. Current Sense Threshold Voltage

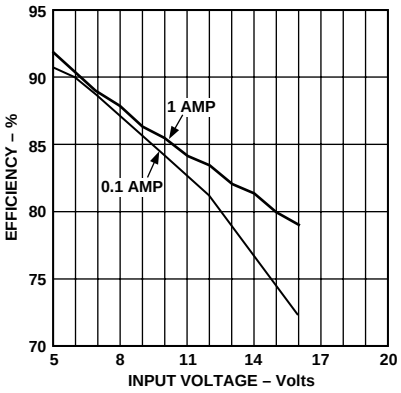


Figure 16. Efficiency vs. Input Voltage at V_O = 3.3 V; Figure 1 Circuit with ADP1147-3.3

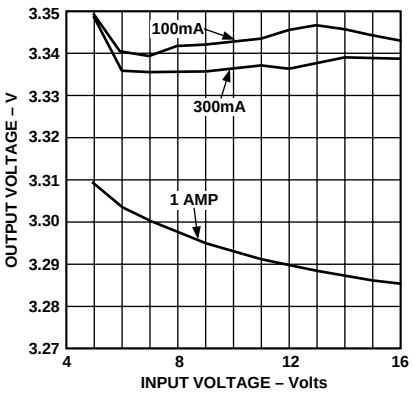


Figure 17. Output Voltage vs. Input Voltage (V_O = 3.3 V); Figure 1 Circuit with ADP1147-3.3

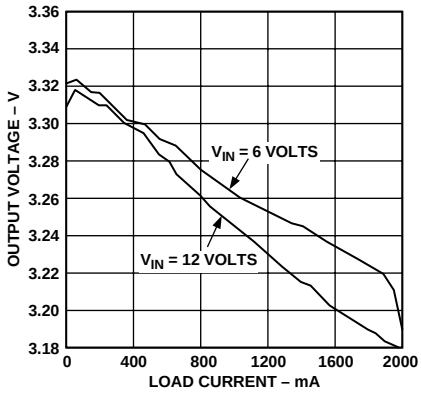
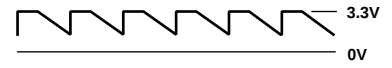


Figure 18. Load Regulation (V_O = 3.3 V); Figure 1 Circuit with ADP1147-3.3



(a) Continuous Mode Operation

(b) Power Saving Mode

Figure 19. C_T Waveforms

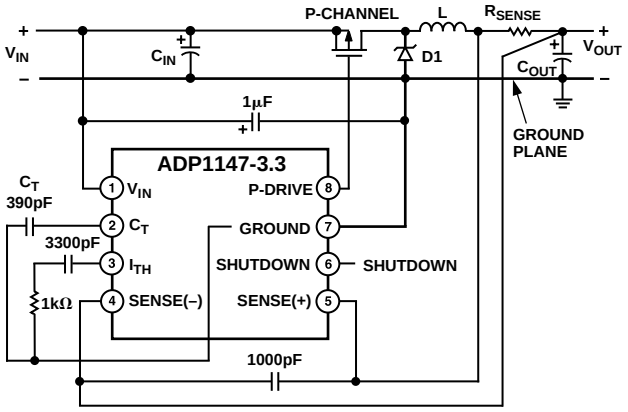


Figure 20. Circuit Diagram Indicating the Recommended Ground Plane Scheme for PCB Layout

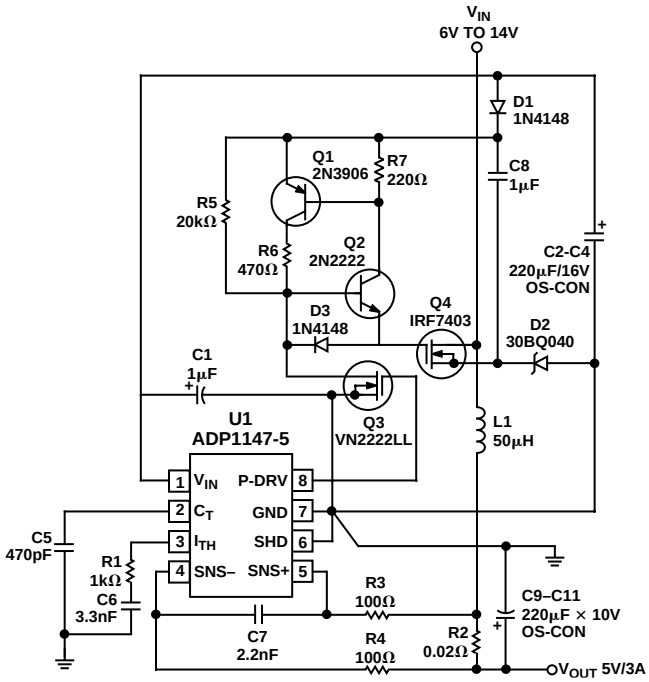


Figure 21. 5 V/3 A Regulator Using N-Channel Device

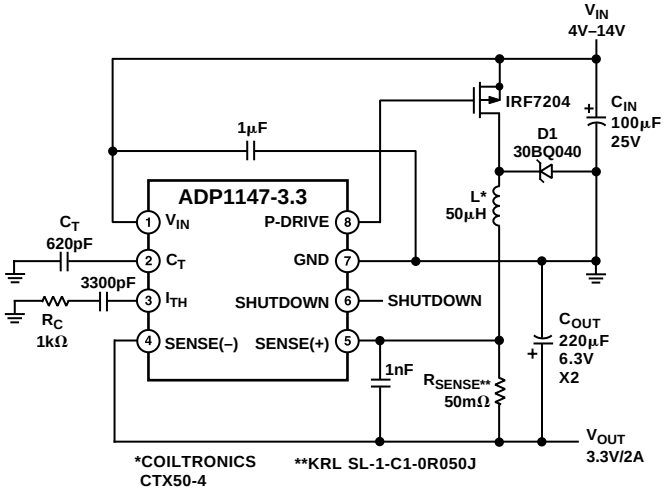


Figure 22. 3.3 V/2 A Regulator

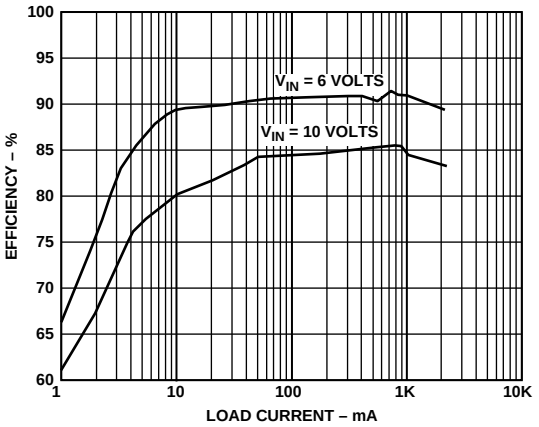


Figure 23. Efficiency vs. Load Current at V_O = 3.3 V; Figure 22 Circuit

APPLICATIONS

The ADP1147 family of regulators incorporate a current mode, constant off-time architecture to switch an external P-channel MOSFET. The external MOSFET can be switched at frequencies up to 250 kHz. The switching frequency of the device is determined by the value selected for capacitor C_T.

A regulated output voltage is maintained by the feedback voltage at the SENSE(–) pin. The SENSE(–) pin is connected to an internal voltage divider. The voltage from this internal divider is fed to comparator V, and gain block G. It is then compared to an internal 1.25 volt reference.

The ADP1147 is capable of maintaining high levels of efficiency by automatically switching between the power saving and continuous modes. The internal R-S flip-flop #2 controls the device in the power saving mode, and gain block G assumes control when the device is in the continuous mode of operation.

During the P-MOSFET on time, the voltage developed across R_{SENSE} is monitored by the SENSE(–) and SENSE(+) pins of the device. When this voltage reaches the threshold level of comparator C the output trips, switching the P drive to V_{IN}, and turns the external P-MOSFET off. At this point capacitor C_T begins to discharge at a rate that is determined by the off-time controller. The C_T discharge current is proportional to the voltage measured at the SENSE(–) pin. When the voltage on cap C_T decays to the threshold voltage (V_{TH1}), comparator T switches and sets R-S flip-flop #1. This forces the P-drive output low, and turns on the P-MOSFET. The sequence is then repeated. As the load current is increased, the output voltage starts to drop. This causes the gain circuit to raise the threshold of the current comparator, and the load current is now tracked.

When load currents are low, comparator B sets the R-S flip-flop #2 and asserts the power savings mode of operation. Comparator B monitors the voltage developed across R_{SENSE}. As the load current decreases to 50% of the designed inductor ripple current, the voltage reverses polarity. This reversal causes comparator B to trip, setting the Q-bar output of R-S flip-flop #2 to a logic zero, and interrupts the cycle by cycle operation of the output. The output storage capacitors are then slowly discharged by the load. When the output cap voltage decays to the V_{OS} level of comparator V, it resets flip-flop #2, and the normal cycle by cycle mode of operation resumes. If load currents are extremely small, the time it takes for flip-flop #2 to reset increases. During the extended wait for reset period, capacitor C_T will discharge below the value of V_{TH2} causing comparator S to trip. This forces the internal sleep bar low and the device enters the sleep mode. A significant amount of the IC is disabled during the sleep mode, reducing the ground current from 1.6 mA to 160 µA, typical. In sleep mode the P-MOSFET is turned off until additional inductor current is required. The sleep mode is terminated when flip-flop #2 is reset.

Due to the constant off-time architecture, the input voltage has an effect on the device switching frequency. To limit the effects of this variation in frequency the discharge current is increased as the device approaches the dropout voltage of V_{IN} +1.5 V. In the dropout mode the P-MOSFET is constantly turned on.

Determining the Output Current and the Value for R_{SENSE}

The value selected for R_{SENSE} is determined by the required output current. The current comparator C has a threshold voltage range of 10 mV/R_{SENSE} to 150 mV/R_{SENSE} maximum. This threshold sets the peak current in the external inductor and yields a maximum output current of:

$$I_{MAX} = I_{PEAK} - \frac{I_{RIPPLE\ p-p}}{2}$$

The resistance values for R_{SENSE} can range from 20 mΩ to 200 mΩ. A graph for selecting R_{SENSE} vs. the maximum output current is shown in Figure 3.

The value of R_{SENSE} can be determined by using the following equation:

$$R_{SENSE}\ (in\ m\Omega) = 100/I_{MAX}$$

This equation allows for a design margin due to component variations.

The following equations are used to approximate the trip point for the power savings mode and the peak short circuit current.

$$I_{POWER\ SAVINGS} \sim 5\ mV/R_{SENSE} + V_O\ t_{OFF}/2L$$

$$I_{SC(PK)} = 150\ mV/R_{SENSE}$$

The ADP1147 automatically increases the t_{OFF} time when a short circuit condition is encountered. This allows sufficient time for the inductor to decay between switching cycles. Due to the resulting inductor ripple current the average short circuit current $I_{SC(AVG)}$ is reduced to approximately I_{MAX}.

Determining the Operating Frequency and Selecting Values for C_T and L

The ADP1147 incorporates a constant off-time architecture to switch an external P-MOSFET. The off-time (t_{OFF}) is determined by the value of the external timing cap C_T. When the P-MOSFET is turned on the voltage across C_T is charged to approximately 3.3 volts. During the switch off-time the voltage on C_T is discharged by a current that is proportional to the voltage level of V_{OUT}. The voltage across C_T is representative of the current in the inductor, which decays at a rate that is proportional to V_{OUT}. Due to this relationship the value of the inductor must track the value selected for C_T.

The following equation is used to determine the desired continuous mode operating frequency:

$$C_T = \frac{1 - \frac{V_{OUT} + V_D}{V_{IN} + V_D}}{1.3 \times 10^4 \times f}$$

V_D = the voltage drop across the Schottky diode.

The graph in Figure 4 can be used to help determine the capacitance value of C_T vs. the operating frequency and input voltage.

The P-MOSFET gate charge losses increase with the operating frequency and results in lower efficiency (see the Efficiency section).

The formula used to calculate the continuous operating frequency is:

$$f = \frac{1 - \frac{V_{OUT} + V_D}{V_{IN} + V_D}}{t_{OFF}}$$

$$t_{OFF} = 1.3 \times 10^4 \times C_T \times \frac{V_{REG}}{V_{OUT}}$$

V_{REG} is the value of the desired output voltage. V_{OUT} is the actual measured value of the output voltage. When in regulation V_{REG}/V_{OUT} is equal to 1. The switching frequency of the ADP1147 decreases as the input voltage decreases. The ADP1147 will reduce the t_{OFF} time by increasing the discharge current in capacitor C_T if the input to output voltage differential falls below 1.5 volts. This is to eliminate the possible occurrence of audible switching prior to dropout.

Now that the operating frequency has been determined and the value selected for C_T, the required inductance for inductor L can be computed. The inductor L should be chosen so it will generate no more than 25 mV/R_{SENSE} of peak-to-peak inductor ripple current.

The following equation is used to determine the required value for inductor L:

$$\frac{25\,mV}{R_{SENSE}} = \frac{(V_{OUT} + V_D) \times t_{OFF}}{L_{MIN}} \; or$$

$$L_{MIN} = \frac{(V_{OUT} + V_D) \times t_{OFF} \times R_{SENSE}}{25\,mV}$$

Substituting for t_{OFF} above gives the minimum required inductor value of:

$$L_{MIN} = 5.1 \times 10^5 \times R_{SENSE} \times C_T \times V_{REG}$$

The ESR requirements for the output storage capacitor can be relaxed by increasing the inductor value, but efficiency due to copper losses will be reduced. Conversely, the use of too low an inductance may allow the inductor current to become discontinuous, causing the device to enter the power savings mode prematurely. As a result of this the power savings threshold is lowered and the efficiency at lower current levels is severely reduced.

Inductor Core Considerations

Now that the minimum inductance value for L has been determined, the inductor core selection can be made. High efficiency converters generally cannot afford the core losses found in low cost powdered iron cores. This forces the use of a more expensive ferrite, molypermalloy, or Kool Mu® cores. The typical efficiency in Figure 1 reflects the use of a molypermalloy core. The cost of the inductor can be cut in half by Using a Kool Mu core type CTX 50-4 by Coiltronics, but the efficiency will be approximately 1%–2% less. The actual core losses are not dependent on the size of the core, but on the amount of inductance. An increase in inductance will yield a decrease in the amount of core loss. Although this appears to be desirable, more inductance requires more turns of wire with added resistance and greater copper losses.

Kool Mu is a registered trademark of Magnetics, Inc.

Using a ferrite cores in a design can produce very low core losses, allowing the designer to focus on minimizing copper loss and core saturation problems. Ferrite cores exhibit a condition known as "Hard Saturation," which results in an abrupt collapse of the inductance when the peak design current is exceeded. This causes the inductor ripple current to rise sharply, the output ripple voltage to increase and the power savings mode of operation to be erroneously activated. To prevent this from occurring the core should never be allowed to saturate.

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for a toroids, but is more expensive than a ferrite core. A reasonable compromise between price and performance, from the same manufacturer is Kool Mu. Toroidal cores are extremely desirable where efficient use of available space and several layers of wire are required. They are available in various surface mount configurations from Coiltronics Inc. and other companies.

Power MOSFET Selection and Considerations

The ADP1147 requires the use of an external P-channel MOSFET. The major parameters to be considered when selecting the power MOSFET are the threshold voltage $V_{GS(TH)}$ and the on resistance of the device $R_{DS(ON)}$.

The minimum input voltage determines if the design requires a logic level or a standard threshold MOSFET. In applications where the input voltage is > 8 volts, a standard threshold MOSFET with a $V_{GS(TH)}$ of < 4 volts can be used. In designs where V_{IN} is < 8 volts, a logic level MOSFET with a $V_{GS(TH)}$ of < 2.5 volts is recommended. Note: If a logic level MOSFET is selected, the supply voltage to the ADP1147 must not exceed the absolute maximum for the V_{GS} of the MOSFET (e.g., < ±8 volts for IRF7304).

The $R_{DS(ON)}$ requirement for the selected power MOSFET is determined by the maximum output current (I_{MAX}). An assumption is made that when the ADP1147 is operating in the continuous mode, either the Schottky Diode or the MOSFET are always conducting the average load current. The following formulas are used to determine the duty cycle of each of the components.

$$P\text{-}Channel\ MOSFET\ \ Duty\ Cycle = \frac{V_{OUT} + V_D}{V_{IN} + V_D}$$

$$Schottky\ Diode\ Duty\ Cycle = \frac{V_{IN} - V_D}{V_{IN} + V_D}$$

Once the Duty Cycle is known, the $R_{DS(ON)}$ requirement for the Power MOSFET can be determined by:

$$R_{DS(ON)} = \frac{(V_{IN} + V_D) \times P_P}{(V_{OUT} + V_D) \times I_{MAX}{}^2 \times (1 + \delta_P)}$$

where P_P is the max allowable power dissipation and where δ_P is the temperature dependency of $R_{DS(ON)}$ for the MOSFET. Efficiency and thermal requirements will determine the value of P_P, (refer to Efficiency section). MOSFETS usually specify the 1+ δ as a normalized $R_{DS(ON)}$ vs. temperature trace, and δ can be approximated to 0.007/°C for most low voltage MOSFETs.

Output Diode Considerations

When selecting the output diode careful consideration should be given to peak current and average power dissipation so the maximum specifications for the diode are not exceeded.

The Schottky diode is in conduction during the MOSFET off-time. A short circuit of V_{OUT} = 0 is the most demanding situation on for the diode. During this time it must be capable of delivering $I_{SC(PK)}$ for duty cycles approaching 100%. The equation below is used to calculate the average current conducted by the diode under normal load conditions.

$$I_{D1} = \frac{V_{IN} - V_{OUT}}{V_{IN} + V_D} \times I_{LOAD}$$

To guard against increased power dissipation due to undesired ringing, it is extremely important to adhere to the following:

1. Use proper grounding techniques.
2. Keep all track lengths as short as possible, especially connections made to the diode (refer to PCB Layout Considerations section).

The allowable forward voltage drop of the diode is determined by the maximum short circuit current and power dissipation. The equation below is used to calculate V_F:

$$V_F = P_D / I_{SC(PK)}$$

where P_D is the maximum allowable power dissipation and is determined by the system efficiency and thermal requirements (refer to Efficiency Section).

C_{IN} Considerations

During the continuous mode of operation the current drawn from the source is a square wave with a duty cycle equal to V_{OUT}/V_{IN}. To reduce or prevent large voltage transients an input capacitor with a low ESR value and capable of handling the maximum rms current should be selected. The formula below is used to determine the required maximum rms capacitor current:

$$C_{IN}\ I_{RMS} = [V_{OUT}\ (V_{IN} - V_{OUT})]^{0.5} \times I_{MAX}/V_{IN}$$

The maximum for this formula is reached when V_{IN} = 2 V_{OUT}, where $I_{RMS} = I_{OUT}/2$. It is best to use this worst case scenario for design margin. Manufacturers of capacitors typically base the current ratings of their caps on a 2000-hour life. This requires a prudent designer to use capacitors that are derated or rated at a higher temperature. The use of multiple capacitors in parallel may also be used to meet design requirements. The capacitor manufacturer should be consulted for questions regarding specific capacitor selection.

In addition, for high frequency decoupling a 0.1 µF to 1.0 µF ceramic capacitor should be placed and connected as close to the V_{IN} pin as possible.

C_{OUT} Considerations

The minimum required ESR value is the primary consideration when selecting C_{OUT}. For proper circuit operation the ESR value of C_{OUT} must be less than two times the value selected for R_{SENSE} (see equation below):

$$C_{OUT}\ Minimum\ Required\ ESR < 2\ R_{SENSE}$$

When selecting a capacitor for C_{OUT}, the minimum required ESR is the primary concern. Proper circuit operation mandates that the ESR value of C_{OUT} must be less than two times the value of R_{SENSE}.

A capacitor with an ESR value equal to R_{SENSE} will provide the best overall efficiency. If the ESR value of C_{OUT} increases to two times R_{SENSE} a 1% decrease in efficiency results. United Chemicon, Nichicon and Sprague are three manufacturers of high grade capacitors. Sprague offers a capacitor that uses an OS-CON semiconductor dielectric. This style capacitor provides the lowest amount of ESR for its size, but at a higher cost. Most capacitors that meet the ESR requirements for I_{P-P} ripple will usually meet or exceed the rms current requirements. The specifications for the selected capacitor should be consulted.

Surface mount applications may require the use of multiple capacitors in parallel to meet the ESR or rms current requirements. If dry tantalum capacitors are used it is critical that they be surge tested and recommended by the manufacturer for use in switching power supplies such as Type 593D from Sprague. AVX offers the TPS series of capacitors with various heights from 2 mm to 4 mm. The manufacturer should be consulted for the latest information, specifications and recommendations concerning specific capacitors. When operating with low supply voltages, a minimum output capacitance will be required to prevent the device from operating in a low frequency mode (see Figure 5). The output ripple also increases at low frequencies if C_{OUT} is too small.

Transient Response

The response of the regulator loop can be verified by monitoring the transient load response. Several cycles may be required for a switching regulator circuit to respond to a step change in the dc load current (resistive load). When a step in the load current takes place a change in V_{OUT} occurs. The amount of the change in V_{OUT} is equal to the delta of $I_{LOAD} \times$ ESR of C_{OUT}. The delta of I_{LOAD} charges or discharges the output voltage on capacitor C_{OUT}. This continues until the regulator loop responds to the change in load and is able to restore V_{OUT} to its original value. V_{OUT} should be monitored during the step change in load for overshoot, undershoot or ringing, which may indicate a stability problem. The circuit shown in Figure 1 contains external components that should provide sufficient compensation for most applications. The most demanding form of a transient that can be placed on a switching regulator is the hot switching in of loads that contain bypass or other sources of capacitance greater than 1 µF. When a discharged capacitor is placed on the load it is effectively placed in parallel with the output cap C_{OUT}, and results in a rapid drop in the output voltage V_{OUT}. Switching regulators are not capable of supplying enough instantaneous current to prevent this from occurring. Therefore, the inrush current to the load capacitors should be held below the current limit of the design.

Efficiency

Efficiency is one of the most important reasons for choosing a switching regulator. The percentile efficiency of a regulator can be determined by dividing the output power of the device by the input power and then multiplying the results by 100. Efficiency losses can occur at any point in a circuit and it is important to analyze the individual losses to determine changes that would yield the most improvement. The efficiency of a circuit can be expressed as:

$$\%\ efficiency = 100\% - (\%\ L1 + \%\ L2 + \%\ L3\ \ldots\ etc.)$$

L1, L2, L3, etc., are the individual losses as a percentage of the input power. In high efficiency circuits small errors result when expressing losses as a percentage of the output power.

Losses are encountered in all elements of the circuit, but the four major sources for the circuit shown in Figure 1 are:

1. The ADP1147 dc bias current.
2. The MOSFET gate charge current.
3. The $I^2 \times R$ losses.
4. The voltage drop of the Schottky diode.

1. The ADP1147's dc bias current is the amount of current that flows into V_{IN} of the device minus the gate charge current. With V_{IN} = 10 volts, the dc supply current to the device is typically 160 µA for a no load condition, and increases proportionally with load to a constant of 1.6 mA in the continuous mode of operation. Losses due to dc bias currents increase as the input voltage V_{IN} is increased. At V_{IN} = 10 volts the dc bias losses are usually less than 1% with a load current greater than 30 mA. When very low load currents are encountered the dc bias current becomes the primary point of loss.
2. The MOSFET gate charge current is due to the switching of the power MOSFET's gate capacitance. As the MOSFET's gate is switched from a low to a high and back to a low again, charge impulses dQ travel from V_{IN} to ground. The current out of V_{IN} is equal to dQ/dt and is usually much greater than the dc supply current. When the device is operating in the continuous mode the I gate charge is = f (Q_P). Typically a P-channel power MOSFET with an R_{DS} on of 135 mΩ will have a gate charge of 40 nC. With a 100 kHz, switching frequency in the continuous mode, the I gate charge would equate to 4 mA or about a 2%–3% loss with a V_{IN} of 10 volts.

   It should be noted that gate charge losses increase with switching frequency or input voltage. A design requiring the highest efficiency can be obtained by using more moderate switching frequencies.

3. $I^2 \times R$ loss is a result of the combined dc circuit resistance and the output load current. The primary contributors to circuit dc resistance are the MOSFET, the Inductor and R_{SENSE}. In the continuous mode of operation the average output current is switched between the MOSFET and the Schottky diode and a continuous current flows through the inductor and R_{SENSE}. Therefore the $R_{DS(ON)}$ of the MOSFET is multiplied by the on portion of the duty cycle. The result is then combined with the resistance of the Inductor and R_{SENSE}. The following equations and example show how to approximate the $I^2 \times R$ losses of a circuit.

$$R_{DS(ON)} \times (Duty\ Cycle) + R_{INDUCTOR} + R_{SENSE} = R$$

$$I_{LOAD}{}^2 \times R = P_{LOSS}$$

$$V_{OUT} \times I_{LOAD} = P_{OUT}$$

$$P_{LOSS}/P_{OUT} \times 100 = \%\ I^2 \times R_{LOSS}.$$

   With the duty cycle = 0.5, $R_{INDUCTOR}$ = 0.15, R_{SENSE} = 0.05 and I_{LOAD} = 0.5 A. The result would be a 3% I^2R loss. The effects of I^2R losses causes the efficiency to fall off at higher output currents.

4. At high current loads the Schottky diode can be a substantial point of power loss. The diode efficiency is further reduced by the use of high input voltages. To calculate the diode loss, the load current should be multiplied by the duty cycle of the diode times the forward voltage drop of the diode.

$$I_{LOAD} \times \%\ duty\ cycle \times V_{DROP} = Diode\ Loss$$

   Figure 6 indicates the distribution of losses versus load current in a typical ADP1147 switching regulator circuit. With medium current loads the gate charge current is responsible for a substantial amount of efficiency loss. At lower loads the gate charge losses become large in comparison to the load, and result in unacceptable efficiency levels. When low load currents are encountered the ADP1147 employs a power savings mode to reduce the effects of the gate loss. In the power savings mode of operation the dc supply current is the major source of loss and becomes a greater percentage as the output current decreases.

   Losses at higher loads are primarily due to I^2R and the Schottky diode. All other variables such as capacitor ESR dissipation, MOSFET switching, and inductor core losses typically contribute less than 2% additional loss.

Circuit Design Example

In using the design example below assumptions are as follows:

V_{IN} = 5 Volts
V_{OUT} = 3.3 Volts
V_{DIODE} drop (V_D) = 0.4 Volts
$I_{MAX\ OUT}$ = 1 Amp
Max switching frequency (f) = 100 kHz.

The values for R_{SENSE}, C_T and L can be calculated based on the above assumptions.

R_{SENSE} = 100 mV/1 Amp = 100 mΩ.
t_{OFF} time = (1/100 kHz) × [1 – (3.7/5.4)] = 3.15 µs.
C_T = 3.15 µs /(1.3×10^4) = 242 pF.
L = $5.1 \times 10^5 \times 0.1\ \Omega \times 242$ pF × 3.3 V = 41 µH.

If we further assume:

1. The data is specified at +25°C.
2. MOSFET max power dissipation (P_P) is limited to 250 mW.
3. MOSFET thermal resistance is 50°C/W.
4. The normalized $R_{DS(ON)}$ vs. temperature approximation (δ_P) is 0.007/°C.

This results in 250 mW × 50°C per watt = 12.5°C of MOSFET heat rise. If the ambient temperature T_A is 50°C, a junction temperature of 12.5°C +50°C, T_A = 62.5°C. δP = 0.007 × (62.5°C –25°C) = 0.2625

We can now determine the required $R_{DS(ON)}$ for the MOSFET:

$$R_{DS(ON)} = 5(0.25)/3.3\ (1)^2\ (1.2625) = 300\ m\Omega$$

The above requirements can be met with the use of a P-channel IRF7204 or an Si9430.

When V_{OUT} is short circuited the power dissipation of the Schottky diode is at worst case and the dissipation can rise greatly. The following equation can be used to determine the power dissipation:

$$P_D = I_{SC(AVG)} \times V_{DIODE}\ Drop$$

A 100 mΩ R_{SENSE} resistor will yield an $I_{SC(AVG)}$ of 1 A. With a forward diode drop of 0.4 volts a 400 milliwatt diode power dissipation results.

The rms current rating needed for C_{IN} will be at least 0.5 A over the temperature range.

To obtain optimum efficiency the required ESR value of C_{OUT} is 100 mΩ or less.

The circuit should also be evaluated with the minimum input voltage. This is done to assure that the power dissipation and junction temperature of the P-channel MOSFET are not exceeded. At lower input voltages the operating frequency of the ADP1147 decreases. This causes the P-channel MOSFET to remain in conduction for longer periods of time, resulting in more power dissipation in the MOSFET.

The effects of $V_{IN(MIN)}$ can be evaluated if we assume the following:

$V_{IN(MIN)}$ = 4.5 V
V_{OUT} = 3.3 V
V_D = 0.4 V
f_{MIN} = (1/3.15 µs) × (1– (3.7/4.9)) = 78 kHz.

$$P_D = \frac{3.3(0.125\ \Omega)(1\ A)^2(1.2625)}{4.5} = 116\ mW$$

Troubleshooting Hints
Efficiency is the primary reason for choosing the ADP1147 for use in an application, and it is critical to determine that all portions of the circuit are functioning properly in all modes. After the design is complete the voltage waveforms on the timing capacitor, C_T, at Pin 2 of the device, should be compared to the waveforms in Figures 19a and 19b.

In the continuous mode of operation the dc voltage level of the waveform on C_T should never fall below the 2 V level and it should have a 0.9 V peak-to-peak sawtooth on it (see Figure 19a).

In the Power Savings Mode the sawtooth waveform on C_T will decay to ground for extended periods of time (see Figure 19b). During the time that the capacitor voltage is at ground the ADP1147 is in the power savings or sleep mode and the quiescent current is reduced to 160 µA typical.

The ripple current in the inductor should also be monitored to determine that it is approximately the same in both modes of operation. With a higher output currents the voltage level on C_T should never decay to ground as this would indicate poor grounding and or decoupling.

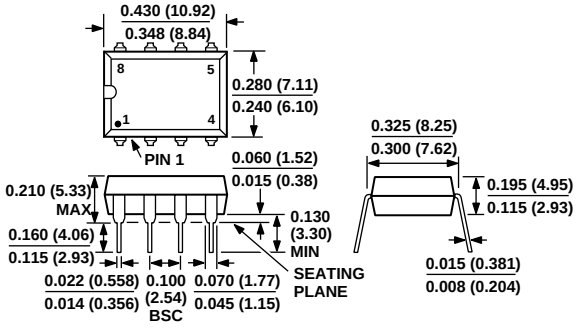
Printed Wire Board Layout Considerations
The PWB layout is extremely critical for proper circuit operation and the items listed below should be carefully considered (see Figure 20)

1. The signal and power grounds should be separate from each other. They should be tied together only at ground Pin 7 of the ADP1147. The power ground should be tied to the anode of the Schottky diode, and the (–) side of the C_{IN} capacitor. The connections should be made with traces that are as wide and as short as possible. The signal ground should be connected to the (–) side of capacitor C_{OUT} using the same type of runs as above.
2. The sense(–) run to Pin 4 of the ADP1147 should be connected directly to the junction point of R_{SENSE} and the + side of C_{OUT}.
3. The sense(–) and sense(+) traces should be routed together with minimum track spacing and run lengths. The 1000 pF filter capacitor across Pins 4 and 5 of the ADP1147 should be located as close to the device as possible.
4. In order to supply sufficient ac current the (+) side of capacitor C_{IN} should be connected with wide short traces and must be located as close to the source of the P-MOSFET as possible.
5. In order to supply high frequency peak currents the input decoupling capacitors should range from 0.1 µF to 1.0 µF and must be located as close to the V_{IN} pin and the ground Pin 7 as possible.
6. The shutdown Pin (6) is a high impedance input and it must not be allowed to float. The normal mode of operation of the device requires that this pin be pulled low.

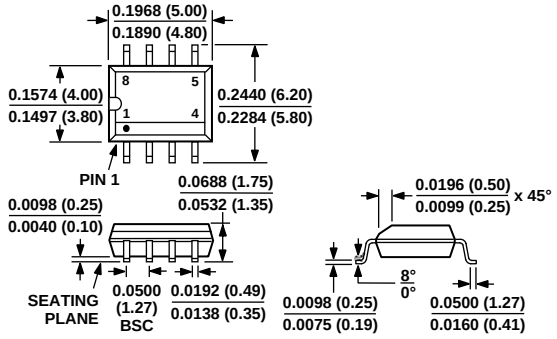
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP
(N-8)



8-Lead SOIC
(SO-8)



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