

Description

The ZXGD3113W6 is intended to drive a MOSFET configured as an ideal diode replacement. The device is comprised of a differential amplifier detector stage and high current driver. The detector monitors the reverse voltage of the MOSFET, such that if the body diode conduction occurs, a positive voltage is applied to the MOSFET's Gate Pin.

Once the positive voltage is applied to the Gate, the MOSFET switches on. The detector's output voltage is then proportional to the MOSFET Drain-Source voltage, and this is applied to the Gate via the driver. This action provides a rapid MOSFET turn-off at zero Drain current.

Applications

- Flyback Converters

Features

- 3.5V to 40V V_{CC} Range
- Operating up to 250kHz
- Suitable for Discontinuous Conduction Mode (DCM), Critical Conduction Mode (CrCM), and Continuous Conduction Mode (CCM) Operation
- Proportional Gate Drive Control
- Detector Threshold Voltage: -10mV
- Standby Current: 6mA
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)**

Mechanical Data

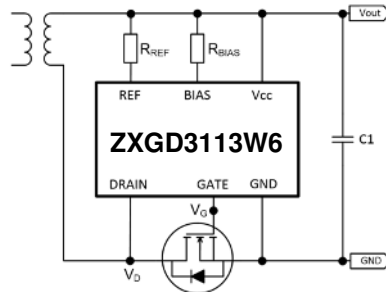
- Case: SOT26
- Case Material: Molded Plastic. "Green" Molding Compound. UL Flammability Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish – Solderable per MIL-STD-202, Method 208
- Weight: 0.018 grams (Approximate)

SOT26

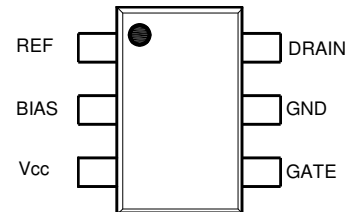


Top View

Typical Configuration



SOT26



Top View
Pin-Out

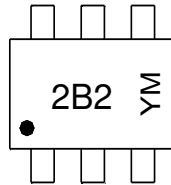
Ordering Information (Note 4)

| Product | Marking | Reel Size (inches) | Tape Width (mm) | Quantity per Reel |
|--------------|---------|--------------------|-----------------|-------------------|
| ZXGD3113W6-7 | 2B2 | 7 | 8 | 3000 |

- Notes:
- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 - See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 - Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 - For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information

SOT26



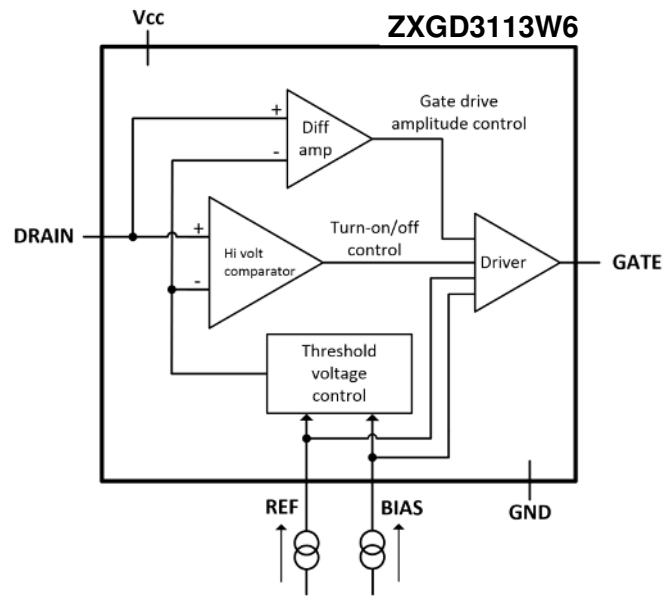
2B2 = Product Type Marking Code
 YM = Date Code Marking
 Y or \bar{Y} = Year (ex: E = 2017)
 M or \bar{M} = Month (ex: 9 = September)

Date Code Key

| Year | 2017 | 2018 | 2019 | 2020 | 2021 | 2022 | 2023 | 2024 | 2025 | 2026 | 2027 |
|------|------|------|------|------|------|------|------|------|------|------|------|
| Code | E | F | G | H | I | J | K | L | M | N | O |

| Month | Jan | Feb | Mar | Apr | May | Jun | Jul | Aug | Sep | Oct | Nov | Dec |
|-------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Code | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | O | N | D |

Functional Block Diagram



| Pin Number | Name | Description and Function |
|------------|----------|-------------------------------------------------------------------------------------------------------------------------------------|
| 1 | REF | Reference This pin is connected to V_{CC} via a resistor, R_{REF} . R_{REF} sets the source current into this pin |
| 2 | BIAS | Bias This pin is connected to V_{CC} via a resistor, R_{BIAS} . R_{BIAS} sets the source current into this pin. |
| 3 | V_{CC} | Power Supply This is the supply pin. It is recommended to decouple this point to Ground closely with a ceramic capacitor. |
| 4 | GATE | Gate Drive This pin sources and sinks current to and from the synchronous MOSFET Gate. |
| 5 | GND | Ground This is the ground reference point. Connect to the synchronous MOSFET Source terminal. |
| 6 | DRAIN | Drain This pin is connected to the Drain pin of the synchronous MOSFET. |

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

| Characteristic | Symbol | Value | Unit |
|---------------------------------|---------------------|--------------------------|------|
| Supply Voltage, Relative to GND | V _{CC} | 40 | V |
| Drain Pin Voltage | V _D | -3 to 160 | V |
| Gate Output Voltage | V _G | -3 to V _{CC} +3 | V |
| Gate Driver Peak Source Current | I _{SOURCE} | 1.5 | A |
| Gate Driver Peak Sink Current | I _{SINK} | 3 | A |
| Reference Voltage | V _{REF} | V _{CC} | V |
| Reference Current | I _{REF} | 25 | mA |
| Bias Voltage | V _{BIAS} | V _{CC} | V |
| Bias Current | I _{BIAS} | 100 | mA |

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

| Characteristic | Symbol | Value | Unit |
|---------------------------------------------|------------------|-------------|-------------|
| Power Dissipation Linear Derating Factor | P _D | 500 | mW mW/°C |
| | | 5 | |
| | | 731 | |
| | | 5.8 | |
| | | 868 | |
| Thermal Resistance, Junction to Ambient | R _{θJA} | 6.9 | °C/W |
| | | 1016 | |
| | | 8.1 | |
| | | 250 | |
| Thermal Resistance, Junction to Lead | R _{θJL} | 171 | °C/W |
| | | 144 | |
| | | 123 | |
| Operating Temperature Range | T _J | -40 to +150 | °C |
| Storage Temperature Range | T _{STG} | -55 to +150 | |

ESD Ratings (Note 10)

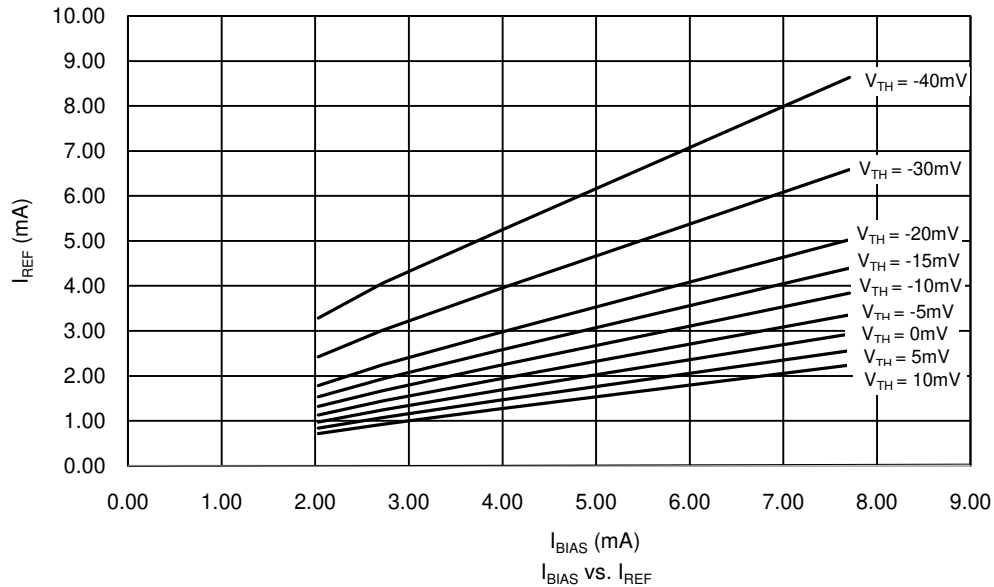
| Characteristic | Symbol | Value | Unit | JEDEC Class |
|------------------------------------------------|---------|-------|------|-------------|
| Electrostatic Discharge - Human Body Model | ESD HBM | 4000 | V | 3A |
| Electrostatic Discharge – Charged Device Model | ESD CDM | 1000 | V | IV |
| Electrostatic Discharge – Machine Model | ESD MM | 400 | V | C |

- Notes:
5. For a device surface mounted on minimum recommended pad layout FR-4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
 6. Same as Note 5, except Pin 3 (V_{CC}) and Pin 2 (BIAS) are both connected to separate 5mm x 5mm 1oz copper heatsinks.
 7. Same as Note 6, except both heatsinks are 10mm x 10mm.
 8. Same as Note 6, except both heatsinks are 15mm x 15mm.
 9. Thermal resistance from junction to solder-point at the end of each lead on Pin 3 (V_{CC}) and Pin 2 (Bias).
 10. Refer to JEDEC specification JESD22-A114 JESD22-A115 and JESD22-C101.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

V_{CC} = 19V; R_{BIAS} = 4.7kΩ; R_{REF} = 8.2kΩ

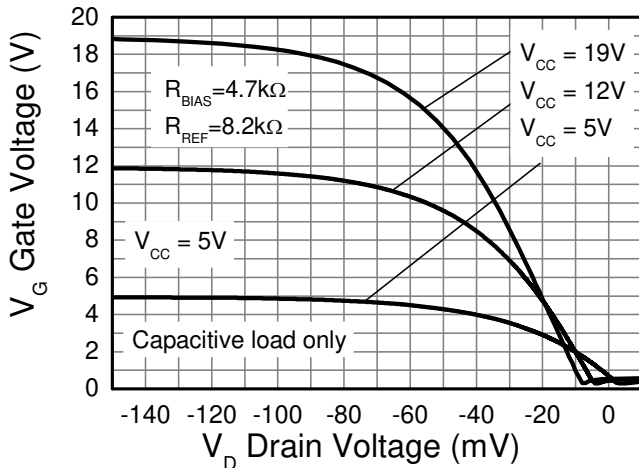
| Characteristic | Symbol | Min | Typ | Max | Unit | Test Condition |
|-----------------------------------------------------------|----------------------|------|------|-----------------|------|-----------------------------------|
| Input and Supply | | | | | | |
| Quiescent Current | I _Q | — | 6.2 | — | mA | V _D ≥ 0V |
| Gate Driver | | | | | | |
| Turn-Off Threshold Voltage | V _T | -20 | -10 | 0 | mV | V _G = 1V |
| Gate Output Voltage | V _{G(OFF)} | 0 | 0.73 | 1.0 | V | V _D ≥ 1V |
| | V _G | 12.5 | 13.8 | V _{CC} | | V _D = -50mV |
| | | 17 | 17.8 | V _{CC} | | V _D = -100mV |
| Switching Performance for C _{LOAD} = 10nF | | | | | | |
| Turn-On Propagation Delay | t _{D(RISE)} | — | 250 | — | ns | — |
| Turn-Off Propagation Delay | t _{D(FALL)} | — | 27 | — | | From 10% of V _G to 10V |
| Gate Rise Time | t _R | — | 187 | — | | From 10% to 90% of V _G |
| | | — | 360 | — | | From 90% to 10% of V _G |
| Gate Fall Time | t _F | — | 210 | — | | |
| Source Current | I _{SOURCE} | — | 0.5 | — | A | Capacitive Load of 10nF |
| Sink Current | I _{SINK} | — | 1.5 | — | | |

Threshold Settings Characteristics (@T_A = +25°C, unless otherwise specified.)


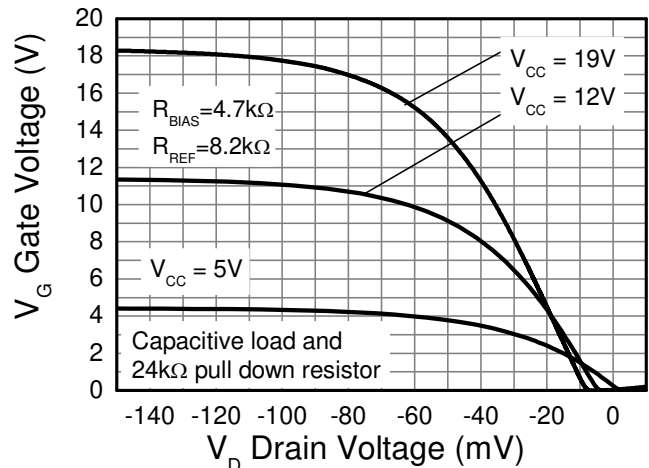
$$R_{BIAS} = \sim (V_{CC} - 0.5) / I_{BIAS}$$

$$R_{REF} = \sim (V_{CC} - 0.7) / I_{REF}$$

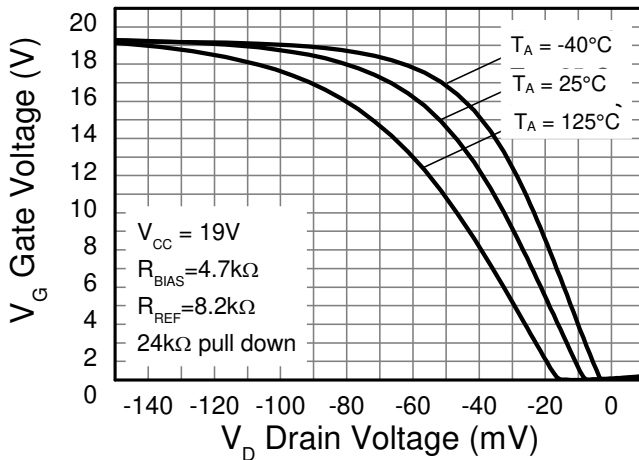
Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)



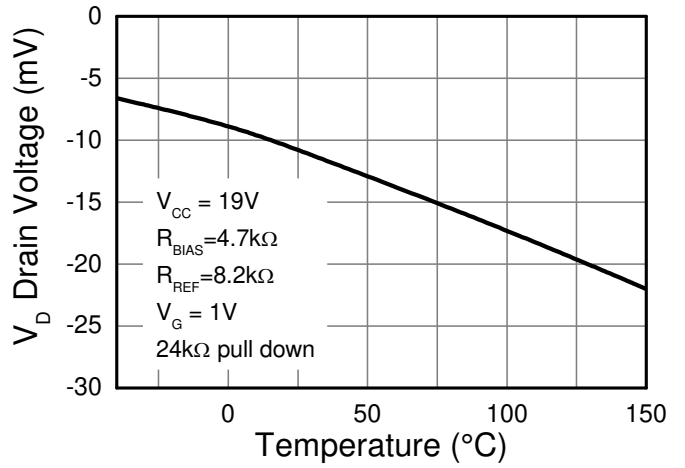
Transfer Characteristic



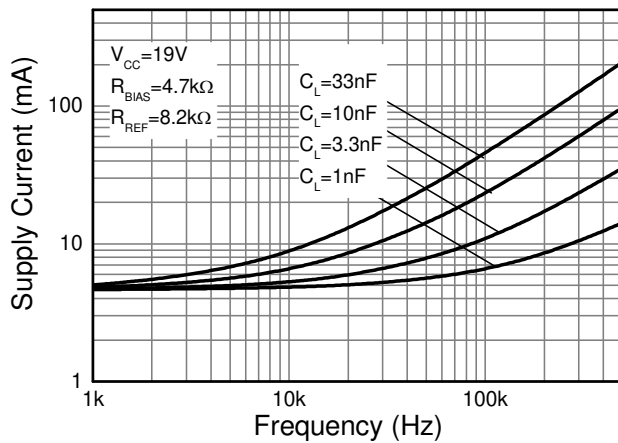
Transfer Characteristic



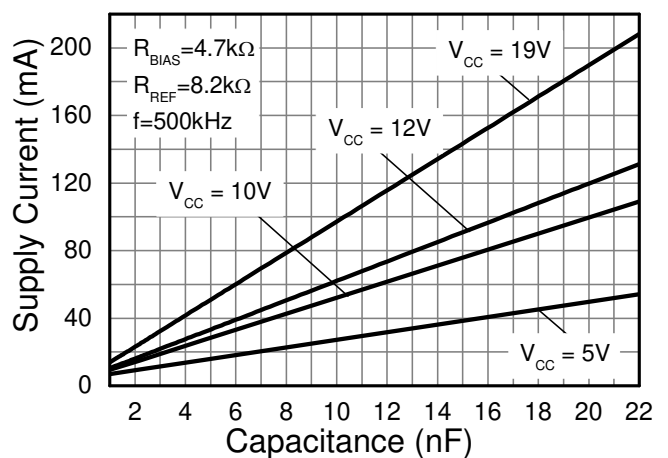
Transfer Characteristic



Drain Sense Voltage vs Temperature

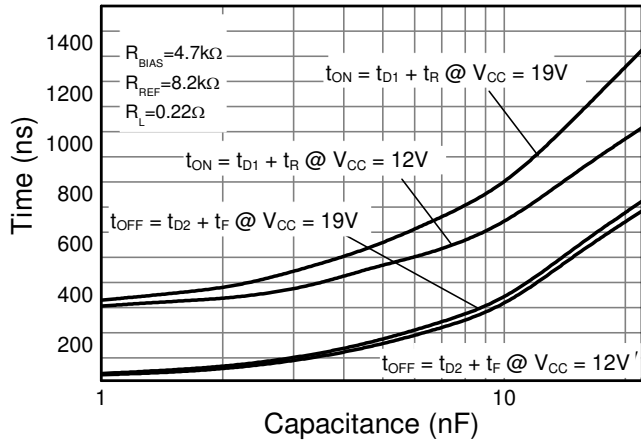


Supply Current vs Frequency

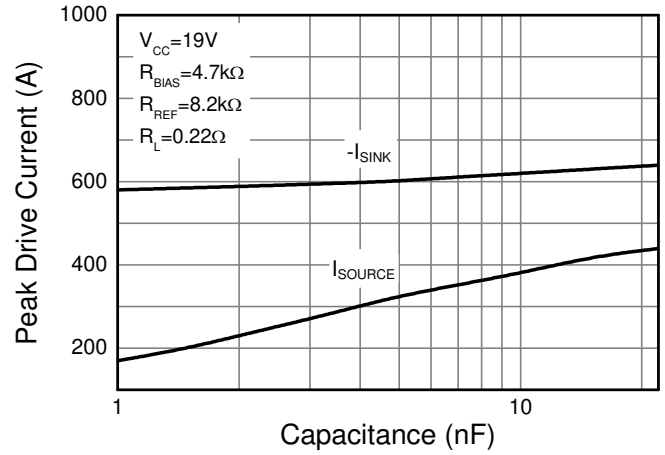


Supply Current vs Capacitive Load

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.) (Cont.)



Switching vs Capacitive Load

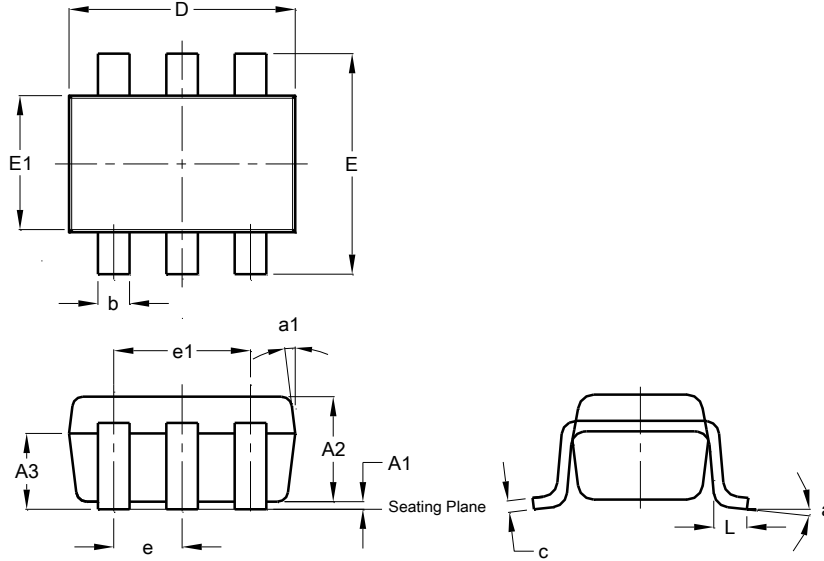


Gate Current vs Capacitive Load

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SOT26

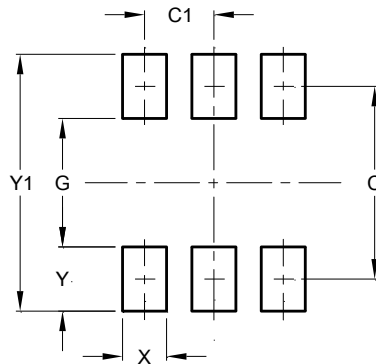


| SOT26 | | | |
|----------------------|-------|------|------|
| Dim | Min | Max | Typ |
| A1 | 0.013 | 0.10 | 0.05 |
| A2 | 1.00 | 1.30 | 1.10 |
| A3 | 0.70 | 0.80 | 0.75 |
| b | 0.35 | 0.50 | 0.38 |
| c | 0.10 | 0.20 | 0.15 |
| D | 2.90 | 3.10 | 3.00 |
| e | - | - | 0.95 |
| e1 | - | - | 1.90 |
| E | 2.70 | 3.00 | 2.80 |
| E1 | 1.50 | 1.70 | 1.60 |
| L | 0.35 | 0.55 | 0.40 |
| a | - | - | 8° |
| a1 | - | - | 7° |
| All Dimensions in mm | | | |

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

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| Dimensions | Value (in mm) |
|------------|---------------|
| C | 2.40 |
| C1 | 0.95 |
| G | 1.60 |
| X | 0.55 |
| Y | 0.80 |
| Y1 | 3.20 |

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

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