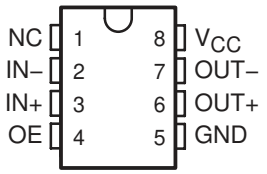
SLCS002D – JUNE 1983 – REVISED AUGUST 2003

- **Operates From a Single 5-V Supply**
- **0-V to 5.5-V Common-Mode Input Voltage Range**
- **Self-Biased Inputs**
- **Complementary 3-State Outputs**
- **Enable Capability**
- **Hysteresis . . . 5 mV Typ**
- **Response Times . . . 25 ns Typ**

**D, P, PS, OR PW PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description/ordering information

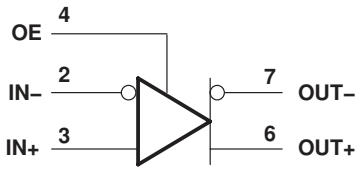
The TL712 is a high-speed comparator fabricated with bipolar Schottky process technology. The circuit has differential analog inputs and complementary 3-state TTL-compatible logic outputs with symmetrical switching characteristics. When the output enable (OE) is low, both outputs are in the high-impedance state. This device operates from a single 5-V supply and is useful as a disk memory read-chain data comparator.

**ORDERING INFORMATION**

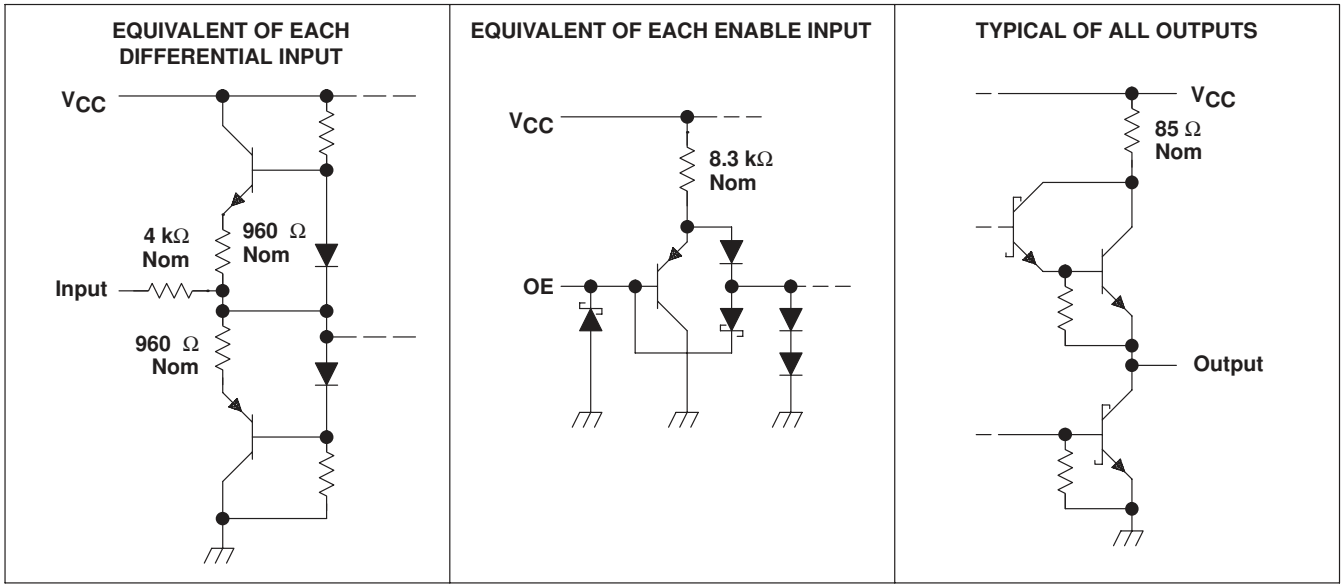
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| 0°C to 70°C | PDIP (P) | Tube of 50 | TL712CP | TL712CP |
| | SOIC (D) | Tube of 75 | TL712CD | TL712C |
| | | Reel of 2500 | TL712CDR | |
| | SOP (PS) | Reel of 2000 | TL712CPSR | T712 |
| | TSSOP (PW) | Tube of 150 | TL712CPW | T712 |
| | | Reel of 2000 | TL712CPWR | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## symbol (positive logic)



## schematics of inputs and outputs




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage, $V_{CC}$ (see Note 1) | 7 V |
| Differential input voltage, $V_{ID}$ (see Note 2) | ±25 V |
| Input voltage, $V_I$, any differential input | ±25 V |
| Output enable voltage | 7 V |
| Low-level output current, $I_{OL}$ | 50 mA |
| Package thermal impedance, $\theta_{JA}$ (see Notes 3 and 4): D package | 97°C/W |
| P package | 85°C/W |
| PS package | 95°C/W |
| PW package | 149°C/W |
| Operating virtual junction temperature, $T_J$ | 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the “recommended operating conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground.
2. Differential voltage values are at IN+ with respect to IN–.
3. Maximum power dissipation is a function of $T_J(max)$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.75 | 5 | 5.25 | V |
| $V_{IC}$ | Common-mode input voltage | 0 | | 5.5 | V |
| $I_{OH}$ | High-level output current | | | –1 | mA |
| $I_{OL}$ | Low-level output current | | | 16 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_T$ | Threshold voltage ($V_{T+}$ and $V_{T-}$) | $V_{ICR}$ = 0 to 5 V | | –100† | | 100 | mV |
| $V_{hys}$ | Hysteresis ($V_{T+} - V_{T-}$) | | | | 5 | | mV |
| $V_{OH}$ | High-level output voltage | $V_{ID}$ = 100 mV, | $I_{OH}$ = –1 mA | 2.7 | 3.5 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = – 100 mV, | $I_{OL}$ = 16 mA | | 0.4 | 0.5 | V |
| $I_{OZ}$ | Off-state output current | $V_O$ = 2.4 V | | | | –20 | μA |
| $I_I$ | Enable current | $V_I$ = 5.5 V | | | | 100 | μA |
| $I_{IH}$ | High-level enable current | $V_{IH}$ = 2.7 V | | | | 20 | μA |
| $I_{IL}$ | Low-level enable current | $V_{IL}$ = 0.4 V | | | | –360 | μA |
| $r_i$ | Differential input resistance | | | 4 | | | kΩ |
| $r_o$ | Output resistance | | | | | 100 | Ω |
| $I_{OS}$ | Short-circuit output current | | | –15 | | –85 | mA |
| $I_{CC}$ | Supply current | $V_{ID}$ = 0, | No load | | 17 | 20 | mA |

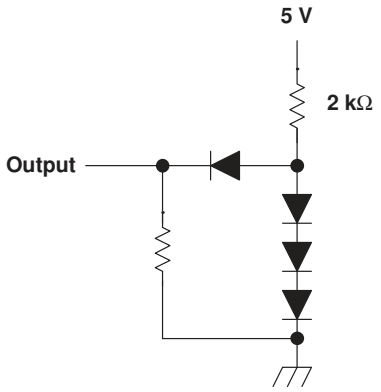
† The algebraic convention, where the more-negative limit is designated as minimum, is used in this data sheet for input threshold voltage levels only.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | TTL load, See Note 5 and Figure 1 | 25 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | 25 | ns |

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive (105 mV total) and is the interval between the input step function and the instant when the output crosses 2.5 V.

## PARAMETER MEASUREMENT INFORMATION




NOTE A: All diodes are 1N4148 or equivalent.

**Figure 1. TTL Output Load Circuit**

## TYPICAL CHARACTERISTICS

**OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVE VOLTAGES**

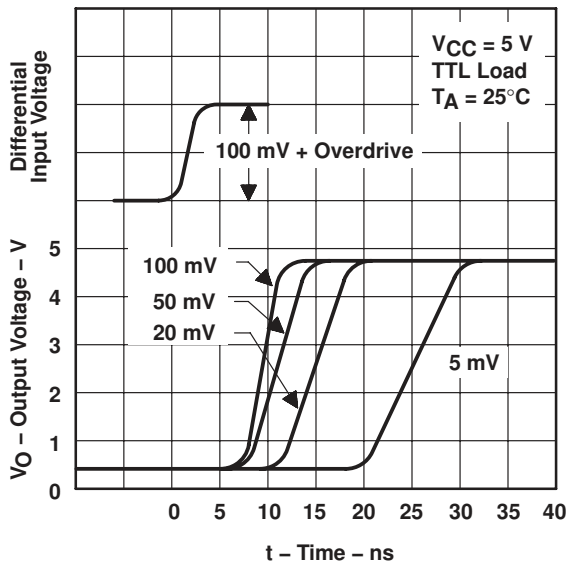



**Figure 2**

**OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVE VOLTAGES**

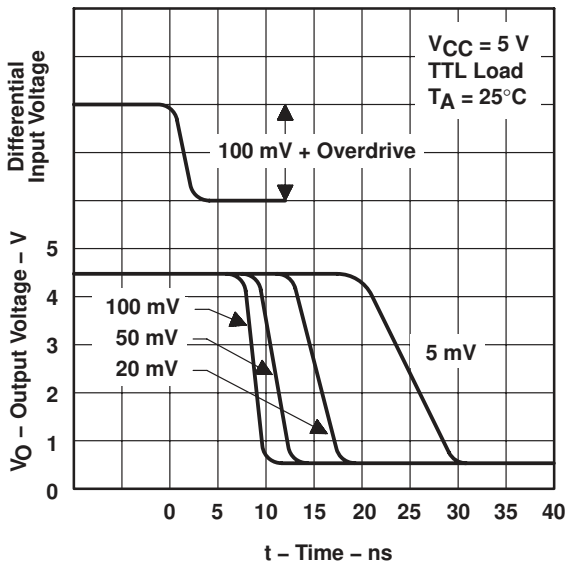



**Figure 3**

## TYPICAL CHARACTERISTICS

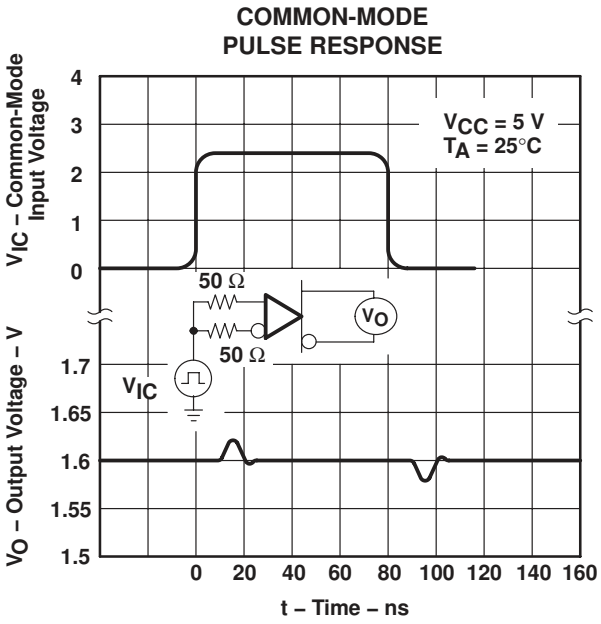



**Figure 4**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TL712CD | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL712C | Samples |
| TL712CDG4 | LIFEBUY | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL712C | |
| TL712CDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL712C | Samples |
| TL712CP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL712CP | Samples |
| TL712CPSR | ACTIVE | SO | PS | 8 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T712 | Samples |
| TL712CPWR | ACTIVE | TSSOP | PW | 8 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T712 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

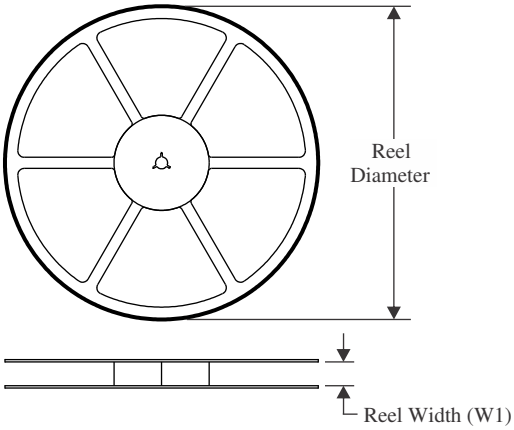
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

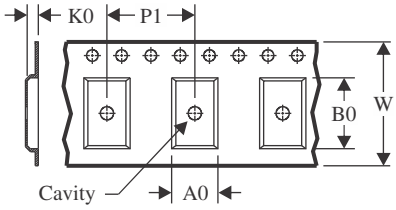
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

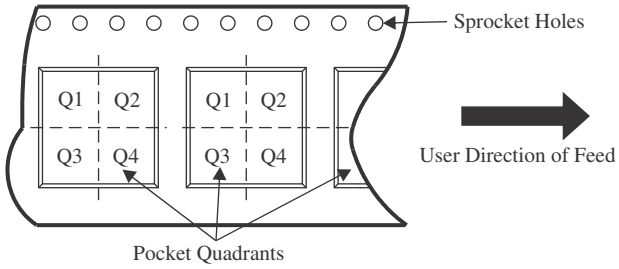



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

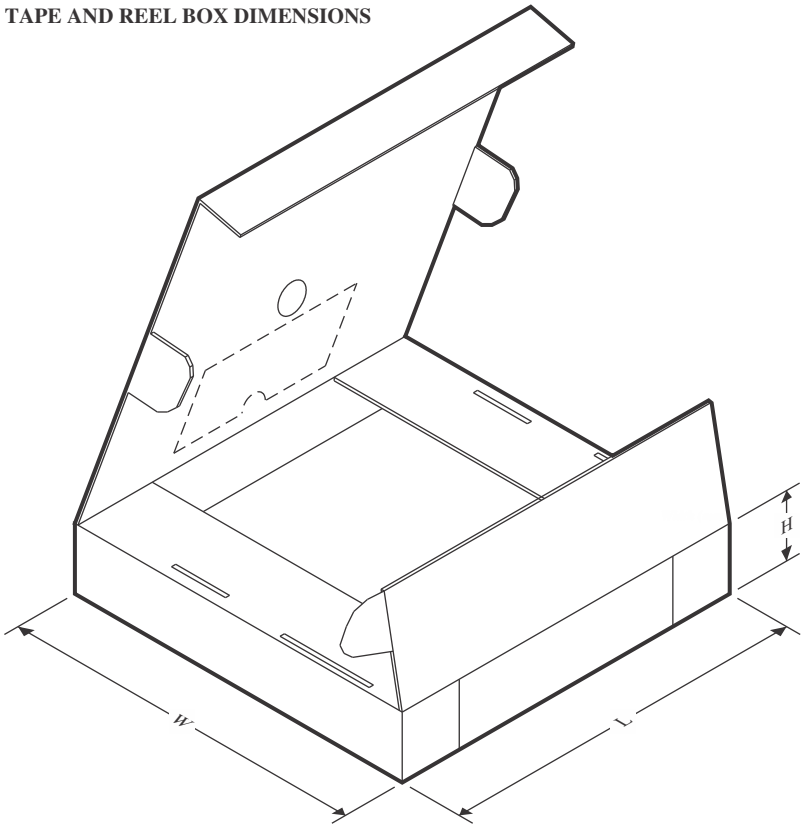
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TL712CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL712CPSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| TL712CPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |

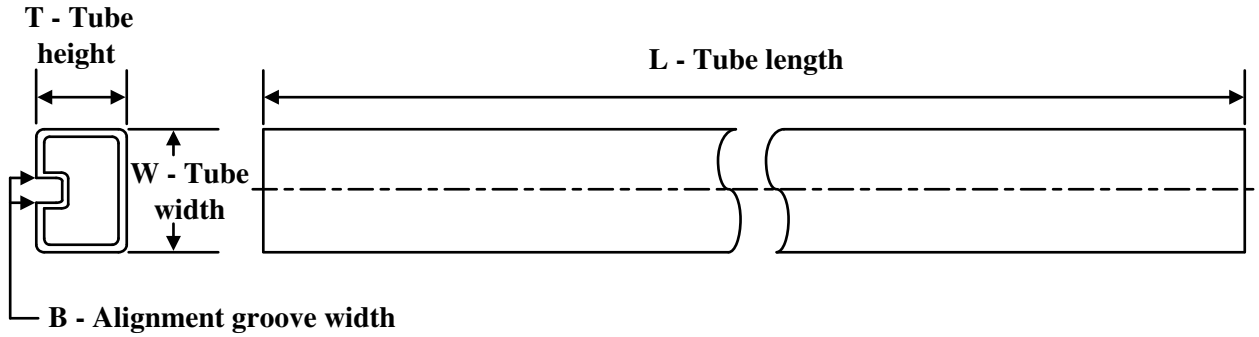
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

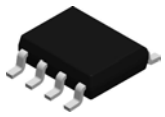
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TL712CDR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TL712CPSR | SO | PS | 8 | 2000 | 356.0 | 356.0 | 35.0 |
| TL712CPWR | TSSOP | PW | 8 | 2000 | 356.0 | 356.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TL712CD | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL712CDG4 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL712CP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |

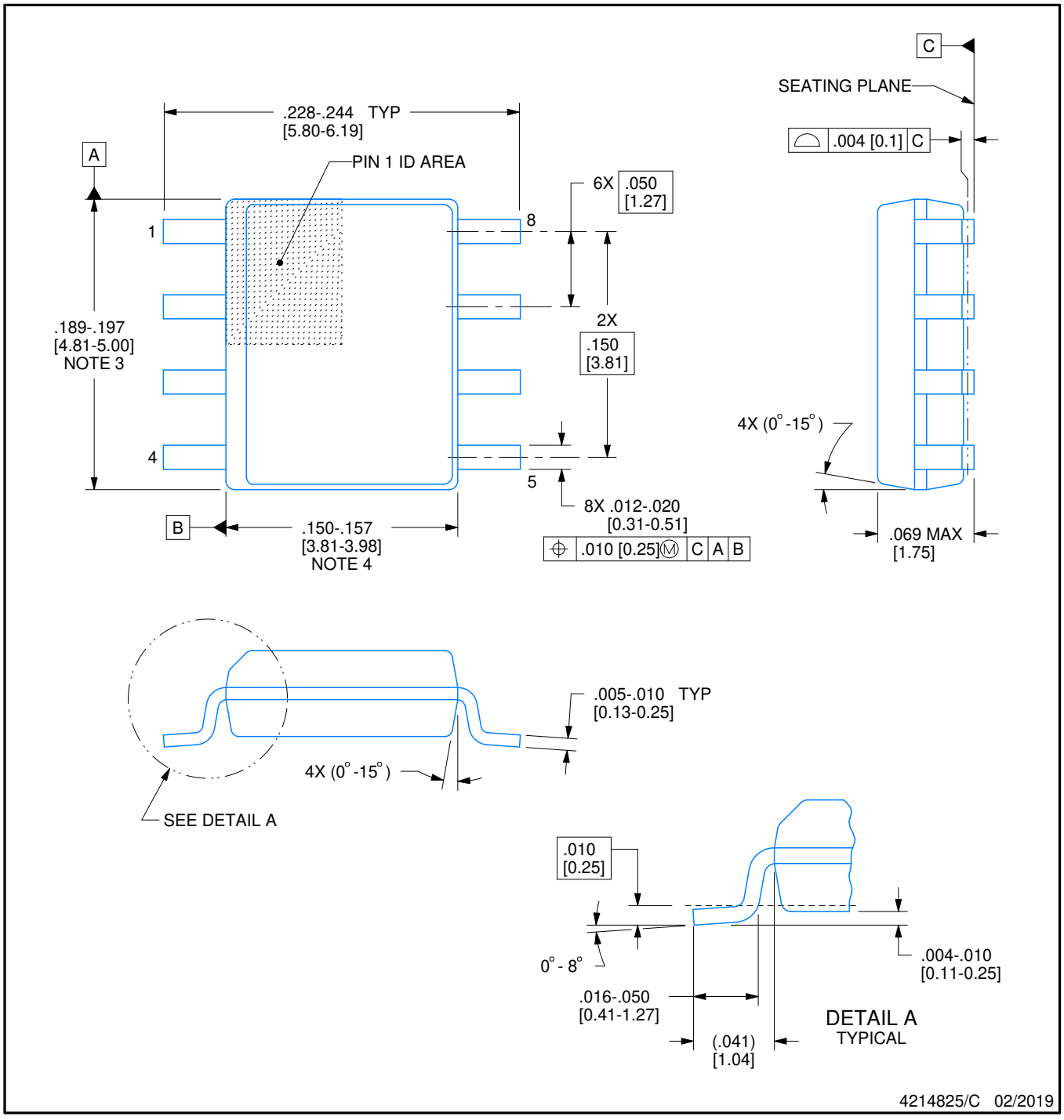


# PACKAGE OUTLINE

## D0008A

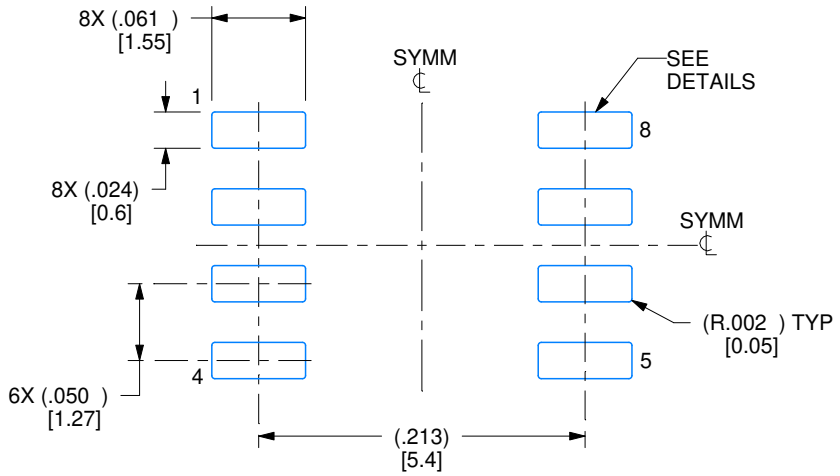
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

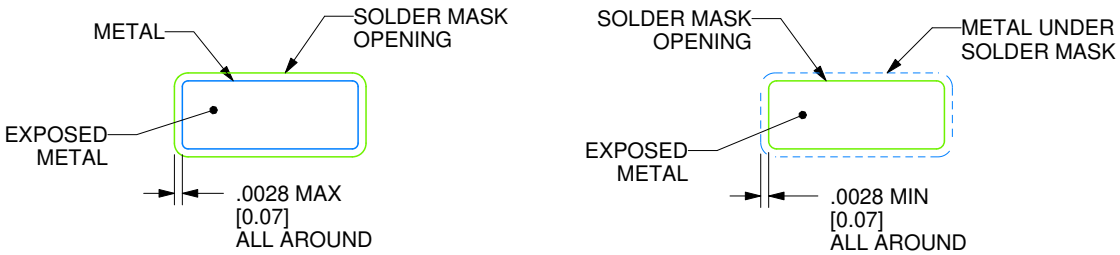



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

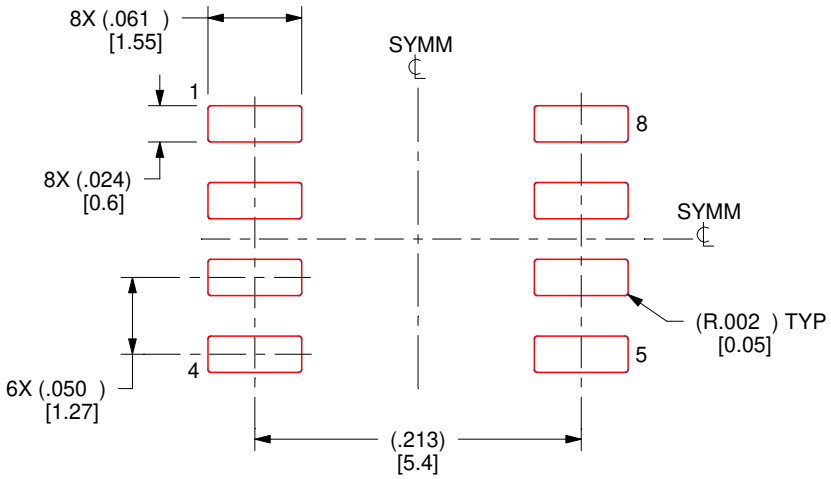
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

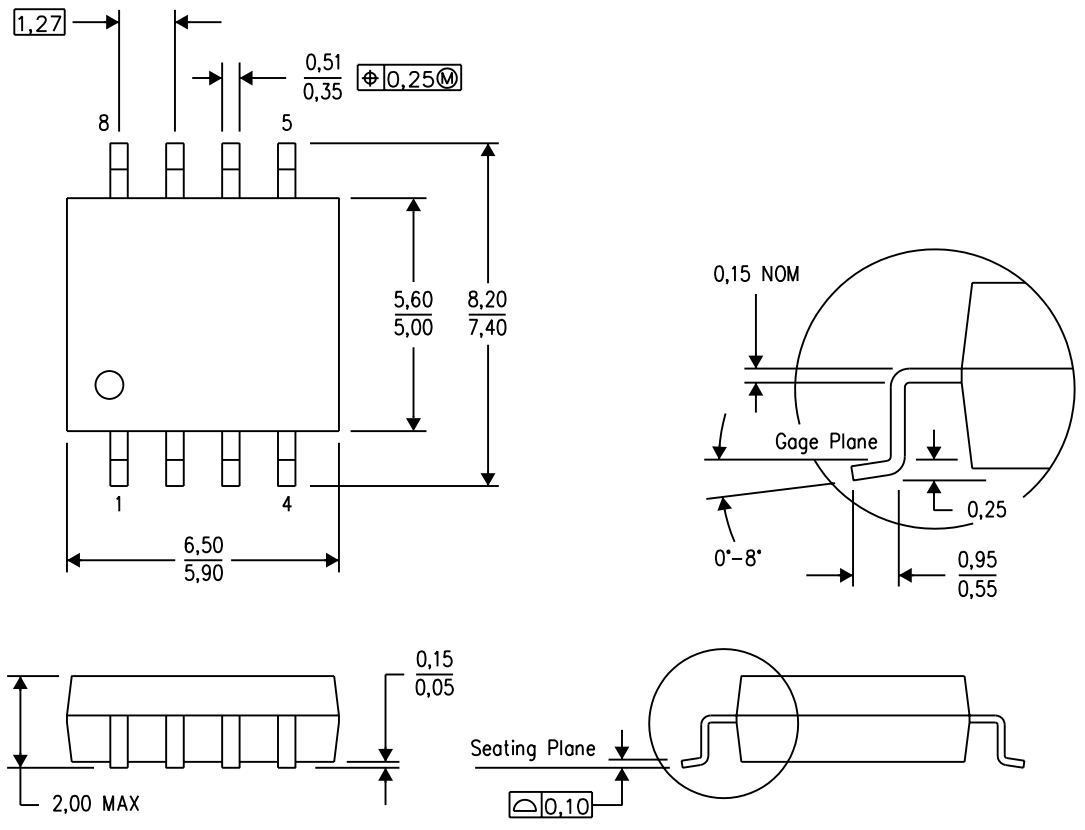
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

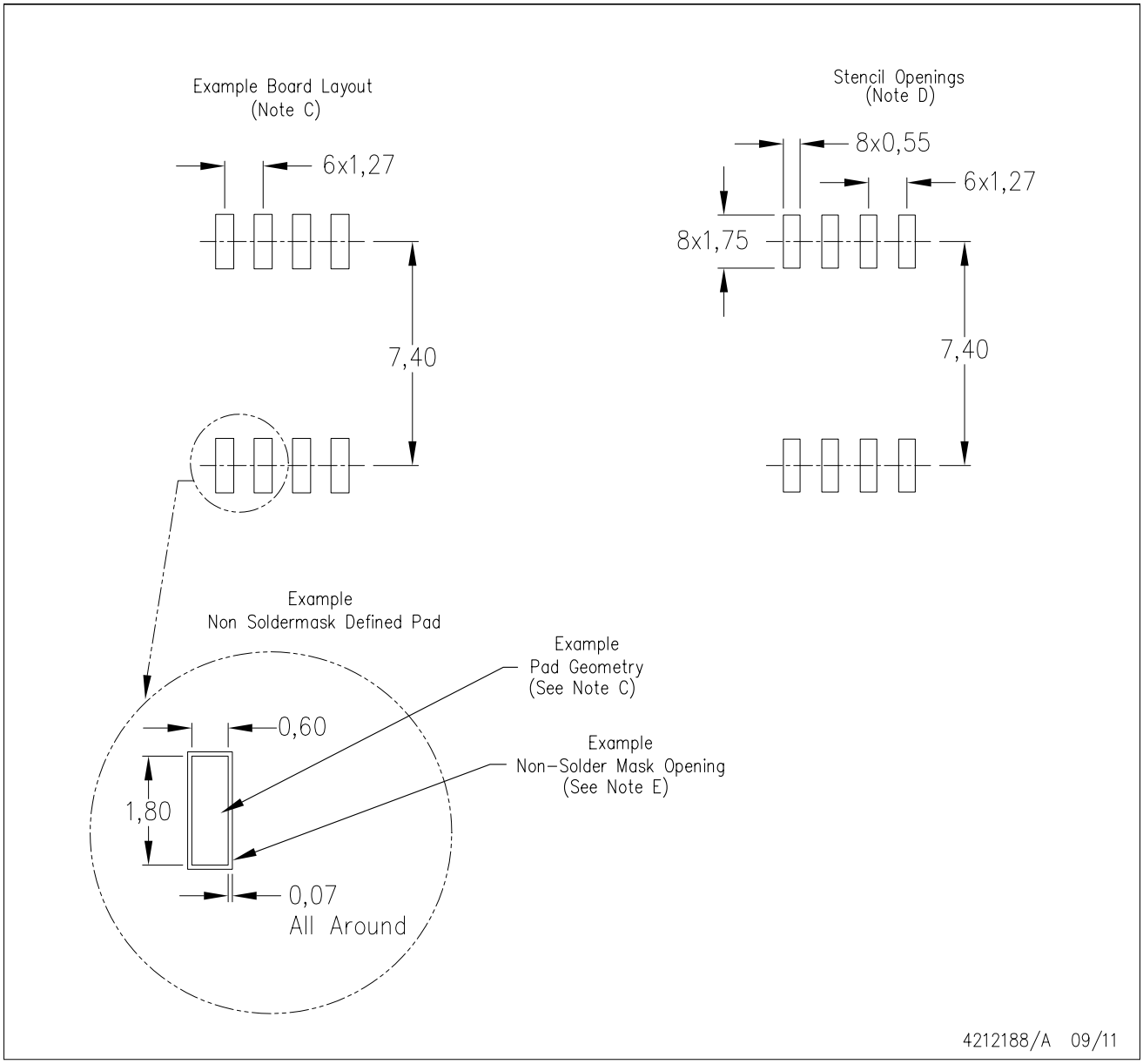
**PS (R-PDSO-G8)** **PLASTIC SMALL-OUTLINE PACKAGE**




4040063/C 03/03

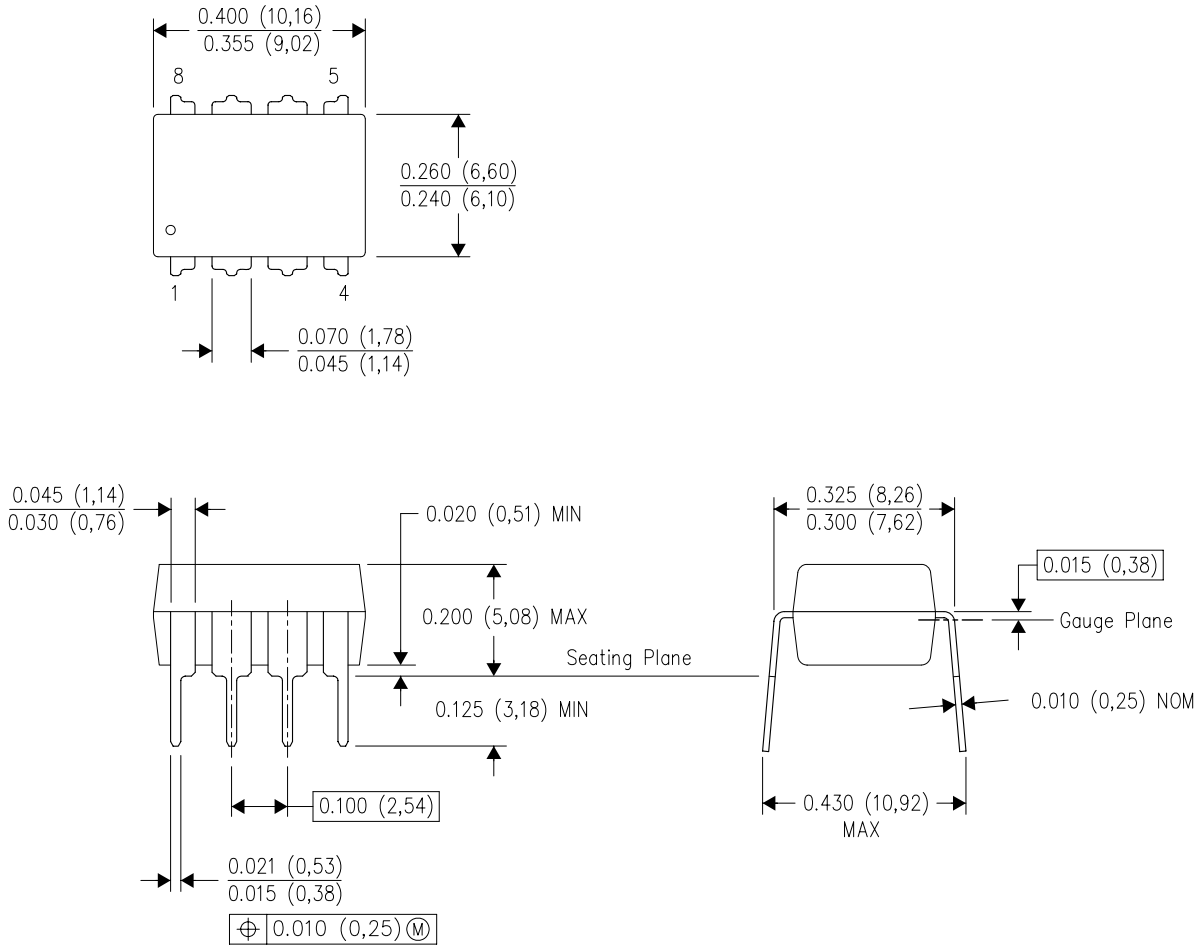
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



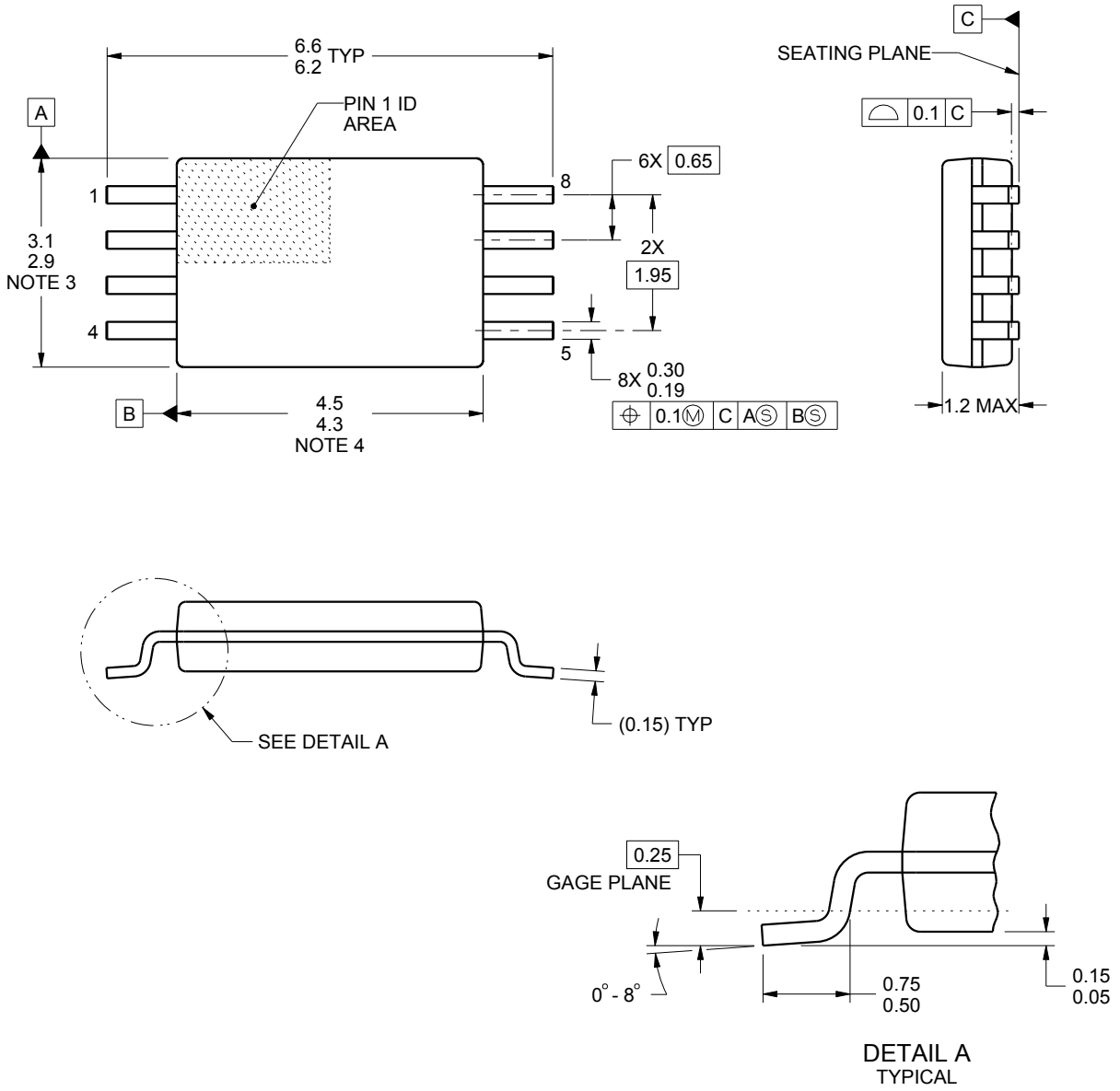

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

# PACKAGE OUTLINE

## PW0008A

## TSSOP - 1.2 mm max height

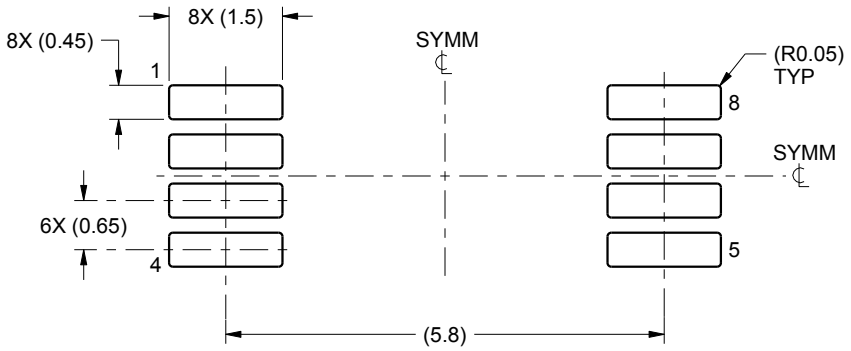
SMALL OUTLINE PACKAGE



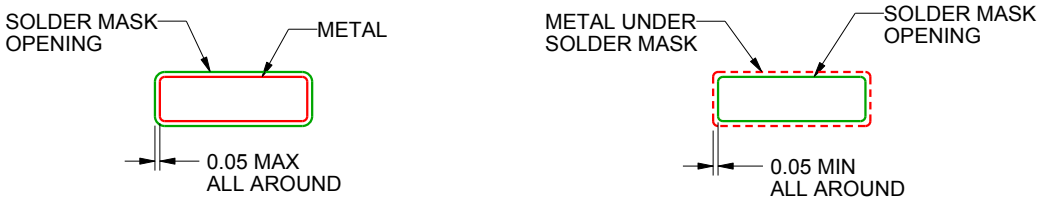

4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.




LAND PATTERN EXAMPLE
SCALE:10X

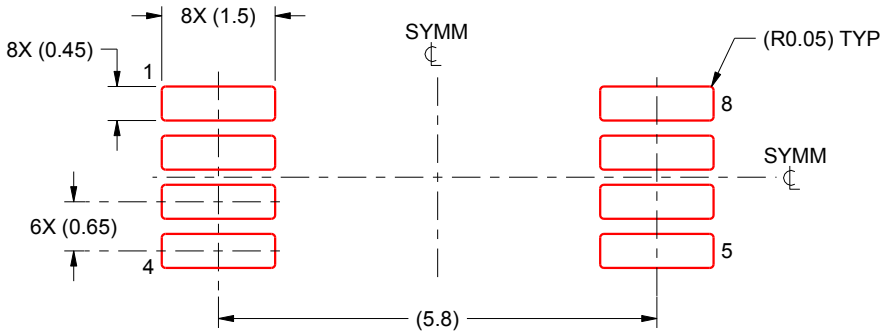



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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