T-37-15

Silicon P-N-P Transistors

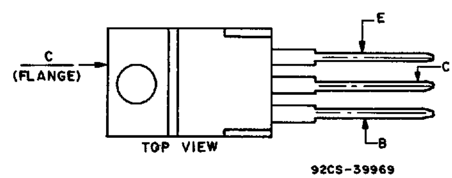
Complementary to the D44VM Series

Features:

- *Very Fast Switching $t_s \leq 500$ ns resistive*
  $t_f \leq 75$ ns
- *Very low $V_{CE\,(sat)} \leq 0.4V$ @ $I_C = 4A$*
- *High gain $H_{FE} \geq 40$ @ $I_C = 4A$*

The D45VM-series of silicon p-n-p power transistors are especially designed for use in switching circuits such as switching regulators, high-frequency inverters/converters, and other applications where very fast switching times and low-saturation voltages are necessary. These devices are tested for parameters that relate directly to the design of high-power switching circuits. Switching times, saturation voltages, and leakage currents are specified at 100°C to provide information necessary for worst-case design..

TERMINAL DESIGNATIONS



JEDEC TO-220AB

MAXIMUM RATINGS (T_A = 25° C) (unless otherwise specified)

RATING	SYMBOL	D45VM1	D45VM4	D45VM7	D45VM10	UNIT
Collector-Emitter Voltage	$V_{CEO(sus)}$	-30	-45	-60	-80	V
Collector-Emitter Voltage	V_{CEX}	-30	-45	-60	-80	V
Collector-Emitter Voltage	V_{CEV}	-50	-70	-80	-100	V
Emitter Base Voltage	V_{EBO}	-7				V
Collector Current — Continuous — Peak (1)	I_C I_{CM}	-8 -20				A
Base Current — Continuous — Peak (1)	I_B I_{BM}	-2 -5				A
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	50 20 0.4				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150				°C

THERMAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	MAX	UNIT
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	74	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	235	°C

(1) Pulse measurement condition PW ≤ 6.0 ms.

ELECTRICAL CHARACTERISTICS (T_C = 25°C) (unless otherwise specified)

CHARACTERISTICS	SYMBOL	MIN	MAX	UNIT
OFF CHARACTERISTICS[1]				
Collector-Emitter Sustaining Voltage[1] (I_C = -100mA, I_B = 0)	$V_{CEO(sus)}$			V
D45VM1		-30	—	
D45VM4		-45	—	
D45VM7		-60	—	
D45VM10		-80	—	
Collector-Emitter Voltage[2] (I_C = -3A, V_{CLAMP} = Rated V_{CEX}, $T_C \leq$ 100°C)	V_{CEX}			V
D45VM1		-30	—	
D45VM4		-45	—	
D45VM7		-60	—	
D45VM10		-80	—	
Collector Cutoff Current	I_{CEV}			μA
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 4.0V)		—	-10	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 4.0V, T_C = 100°C)		—	-100	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	-100	μA
Emitter Cutoff Current (V_{EB} = -7V, I_C = 0)	I_{EBO}	—	-10	μA
SECOND BREAKDOWN				
Second Breakdown with Base Forward Biased	F_{BSOA}	SEE FIGURE 7		
Second Breakdown with Base Reverse Biased	R_{BSOA}	SEE FIGURE 8		
ON CHARACTERISTICS[1]				
DC Current Gain	h_{FE}			—
(I_C = -4A, V_{CE} = -1V)		40	—	
(I_C = -6A, V_{CE} = -1V)		20	—	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			V
(I_C = -4A, I_B = -0.2A)		—	-0.4	
(I_C = -6A, I_B = -0.3A)		—	-0.6	
(I_C = -8A, I_B = -0.8A, T_C = 100°C)		—	-1.0	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			V
(I_C = -4A, I_B = -0.2A)		—	-1.2	
(I_C = -4A, I_B = -0.2A, T_C = 100°C)		—	-1.2	

DYNAMIC CHARACTERISTICS

		Typical	
Current-Gain — Bandwidth Product (I_C = -0.1A, V_{CE} = -10V, f_{test} = 1 MHz)	f_T	50	MHz
Output Capacitance (V_{CB} = -10V, I_E = 0, f_{test} = 1 MHz)	C_{OB}	70	pF

SWITCHING CHARACTERISTICS

			Maximum		
Resistive Load (See Figure 16 for Test Circuit)		T_C	25°C	100°C	
Delay Time	V_{CC} = 30V, I_C = -6A	t_d	30	40	nsec
Rise Time	I_{B1} = I_{B2} = 0.6A	t_r	250	350	nsec
Storage Time	t_p = 25 μsec	t_s	500	600	nsec
Fall Time		t_f	75	250	nsec
Inductive Load, Clamped (See Figure 15 for Test Circuit)					
Storage Time	$V_{CE(CLAMP)}$ = 30V, I_C = -6A	t_s	500	600	nsec
Fall Time	I_{B1} = I_{B2} = 0.6A, $V_{BE(OFF)}$ = 5V	t_f	70	100	nsec
			Typical		
Storage Time	L = 200 μh	t_s	340	430	nsec
Fall Time		t_f	40	57	nsec

(1) Pulse Duration = 300 μsec, Duty Factor ≤ 2%
(2) See Figure 15 for Test Circuit.

TYPICAL DC CHARACTERISTICS

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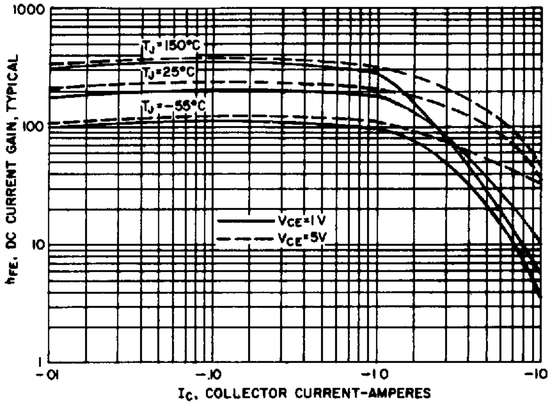

FIGURE 1. DC CURRENT GAIN

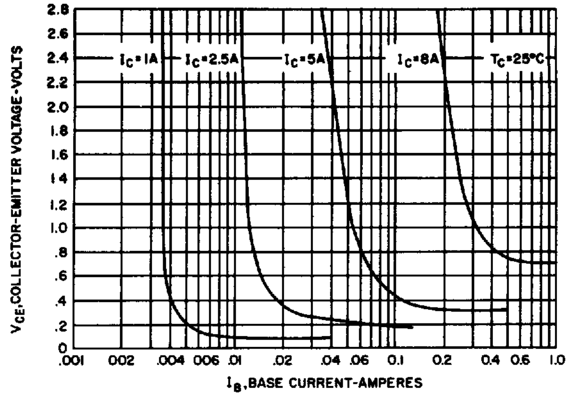

FIGURE 2. COLLECTOR SATURATION REGION

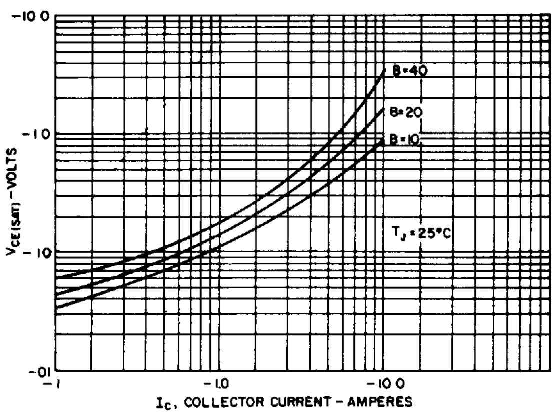

FIGURE 3. $V_{CE(SAT)}$ VS. I_C

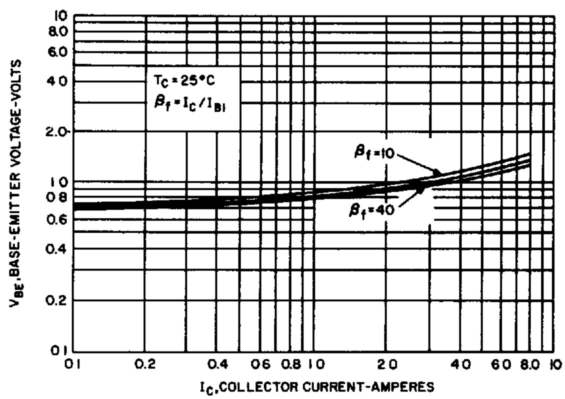

FIGURE 4. $V_{BE(SAT)}$ VS. I_C

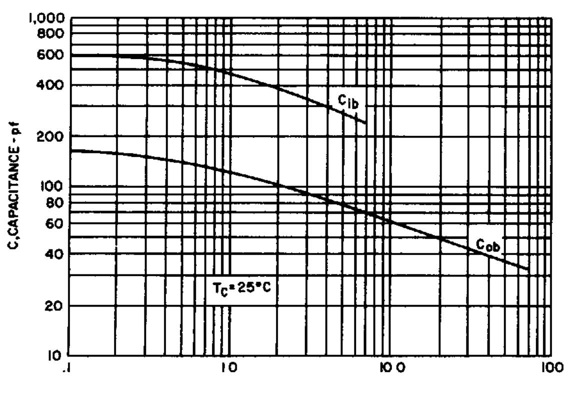

FIGURE 5. CAPACITANCE

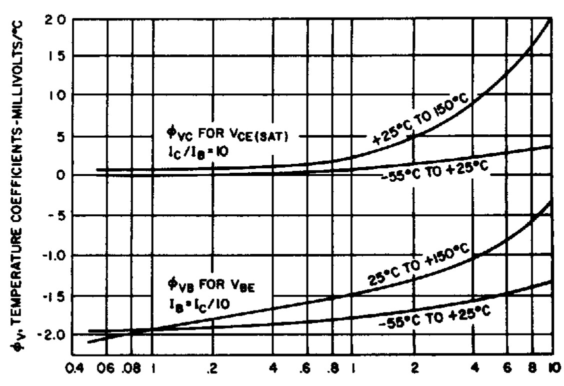

FIGURE 6. SATURATION VOLTAGE TEMPERATURE COEFFICIENTS

SAFE OPERATING AREA

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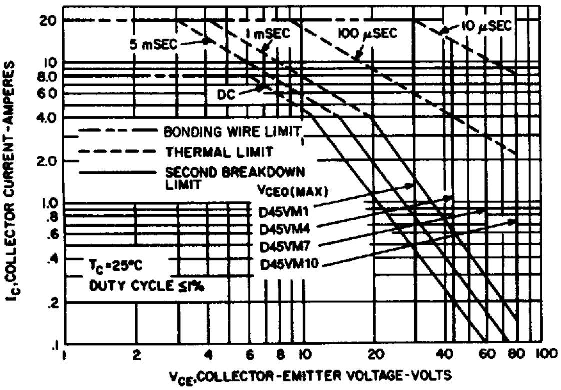


FIGURE 7. FORWARD BIAS SOA

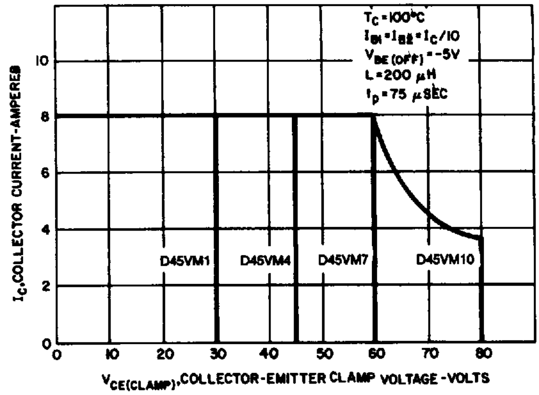


FIGURE 8. CLAMPED REVERSE BIAS SOA

TYPICAL SWITCHING CHARACTERISTICS

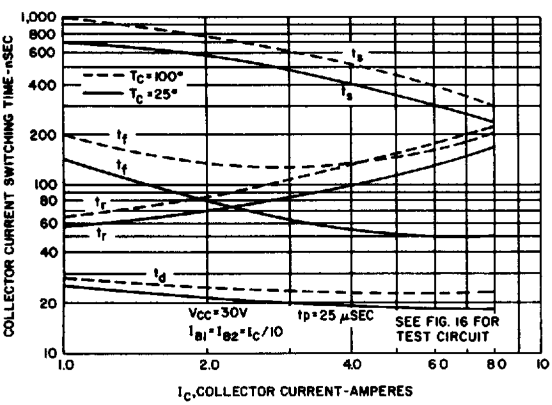


FIGURE 9. RESISTIVE SWITCHING TIME

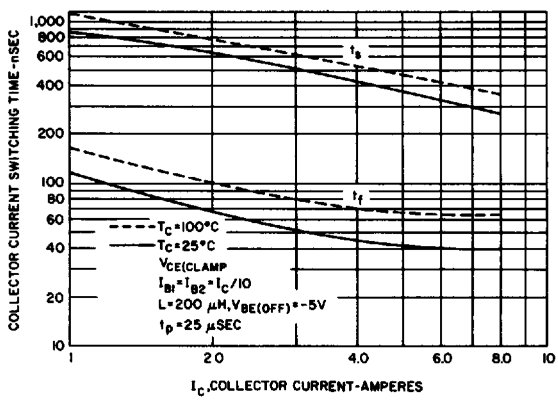


FIGURE 10. CLAMP INDUCTIVE TURN-OFF TIME

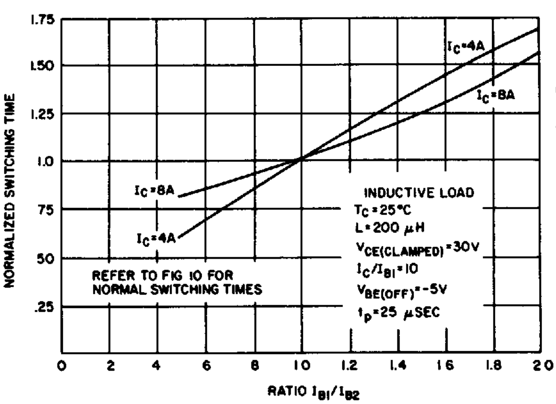


FIGURE 11. STORAGE TIME VARIATION WITH I_{B2}

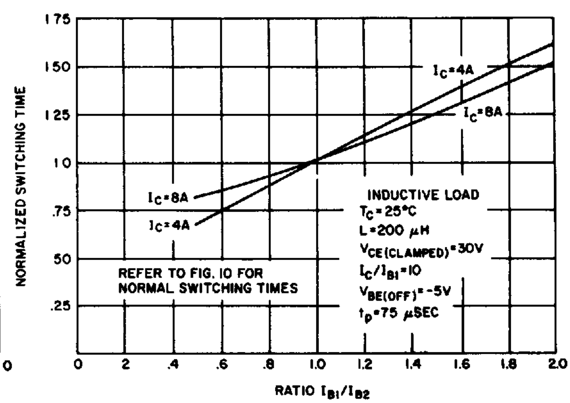


FIGURE 12. FALL TIME VARIATION WITH I_{B2}

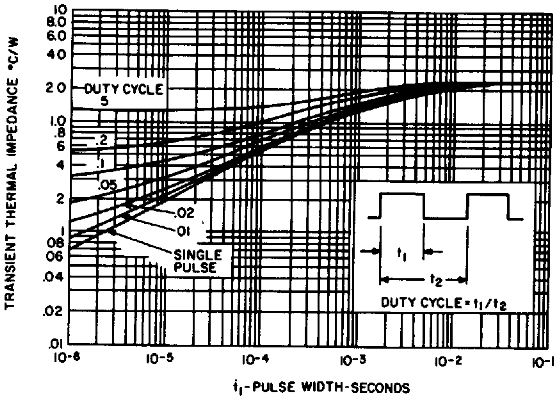


FIGURE 13. TRANSIENT THERMAL RESPONSE

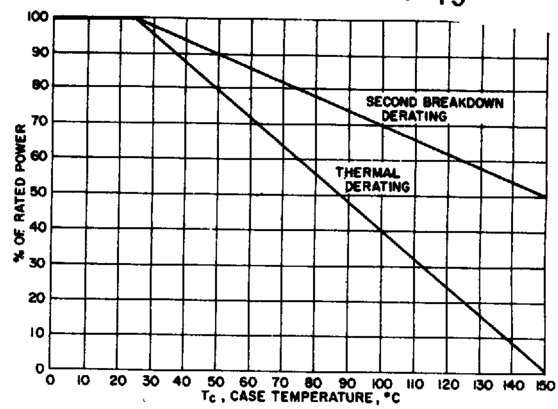
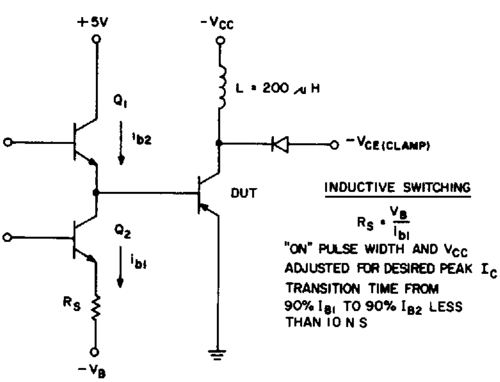
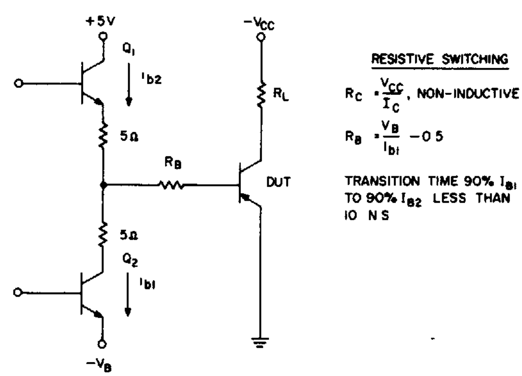


FIGURE 14. POWER DERATING FACTOR

TEST CIRCUITS



15. INDUCTIVE SWITCHING AND V_{CEX}



16. RESISTIVE SWITCHING