XRD9818

3-CHANNEL 16-BIT LINEAR CCD/CIS SENSOR SIGNAL PROCESSOR

JUNE 2004 *REV. 1.0.1*

GENERAL DESCRIPTION

The XRD9818 is a fully integrated, high-performance analog signal processor/digitizer specifically designed for use in 3-channel/2-channel/1-channel CCD/CIS document imaging applications.

Each channel of the XRD9818 includes a Correlated Double Sampler (CDS), Offset adjustment, Programmable Gain Amplifier (PGA). After the gain and offset adjustments the analog inputs are sequentially sampled and digitized by a 16-bit A/D converter. The digital output data is available in 8 or 4-bit wide multiplexed format.

The analog front-end can be configured for use in CCD or CIS data acquisition applications. The CDS mode of operation supports both line and pixel-clamp modes and can be used to achieve significant reduction in system 1/f noise and CCD reset clock feed-through. Five programmable clamp levels are available in CCD mode to adjust for CCD signal swing and reset pulse size. For CIS mode there are 3 selectable reference options, two internally generated and one external applied reference.

Two PGA ranges, programmable through the serial port, help interface the XRD9818 to CCD imagers that have either a 3V or 2V output swings. The range of 1x to 5x is used for 3V inputs and the range of 1.5x to 7.5x is used for 2V inputs. Each channel has an offset range of -180mV to 180mV (1.4mV/step) for fine adjustment and an additional -100mV to 200mV (100mV/step) of gross offset adjustment to correct for any system offsets.

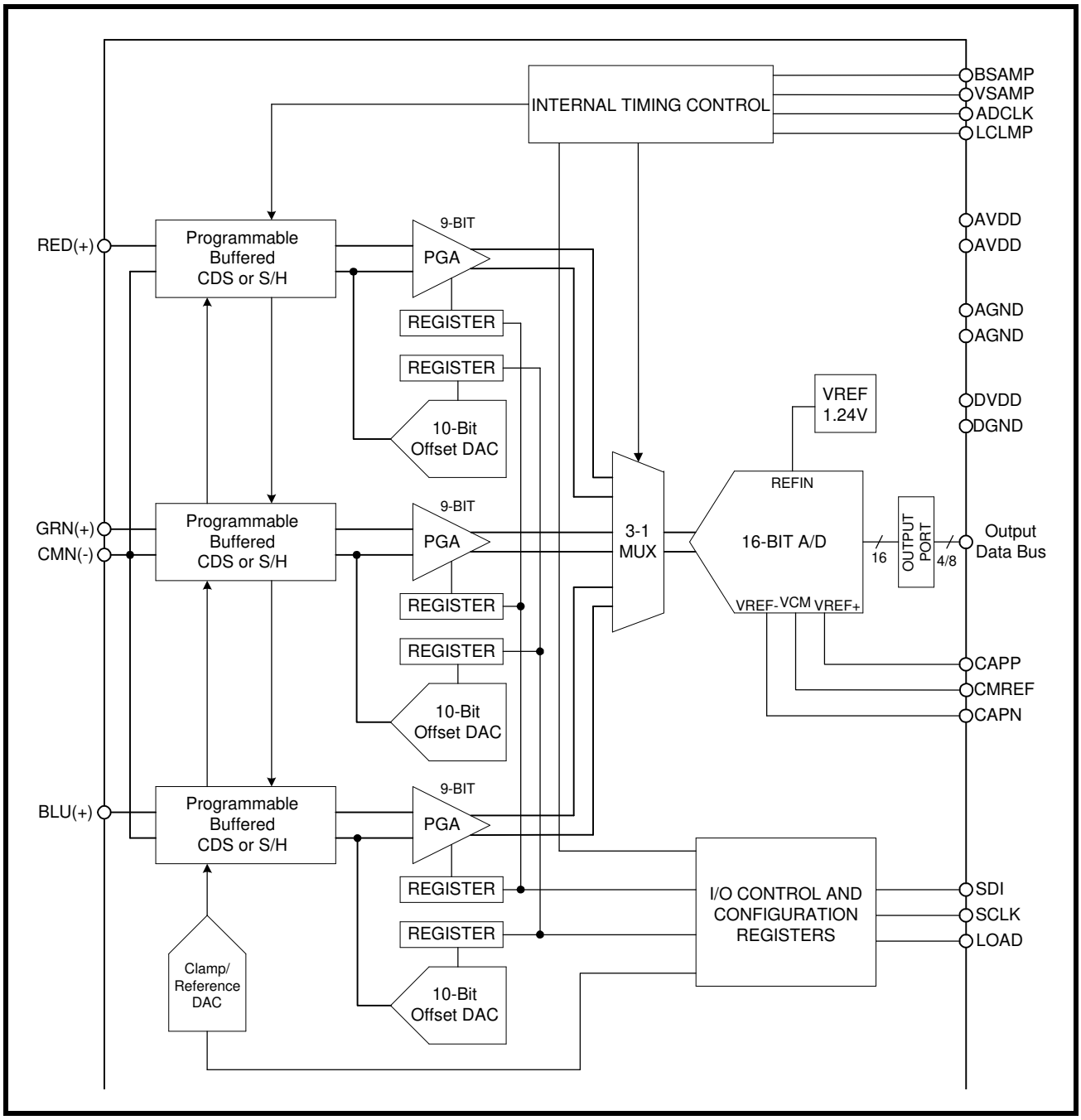
FEATURES

- 16-Bit A/D Converter
- Triple-Channel, 4MSPS Color Scan Mode
- Single-Channel, 8MSPS Monochrome Scan Mode
- Multiplexed 8-Bit or 4-Bit Output Data Formats
- Triple Correlated Double Sampler
- Triple 9-Bit Programmable Gain Amplifier
- Two Programmable Gain Ranges
- Triple 10-Bit Offset Compensation DAC
- -280mV to +380mV Offset Compensation
- 28-pin TSSOP Package
- Internal Voltage Reference
- 3V Operation with 5V Tolerant inputs
- Low Power CMOS: 190mW @ 3.3V (typ), Power Down 1mW (typ)

APPLICATIONS

- 48-Bit Color Scanners
- High-performance CCD or CIS Color Scanners
- Multifunction Peripherals
- Film Scanners

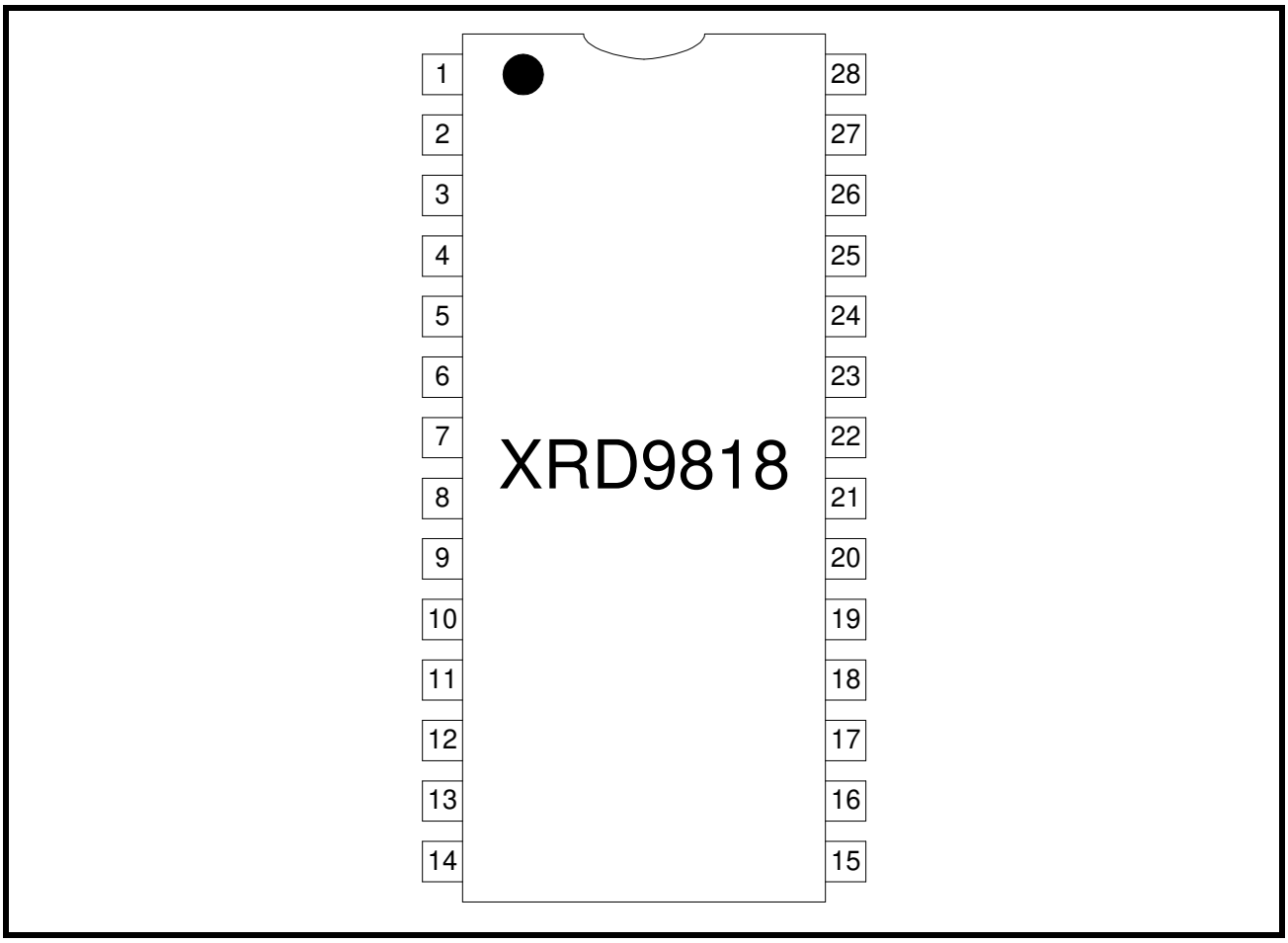
FIGURE 1. BLOCK DIAGRAM OF THE XRD9818



PRODUCT ORDERING INFORMATION

Product Number	Package Type	Operating Temperature Range
XRD9818ACG	28-Lead TSSOP	0°C to +70°C

FIGURE 2. PIN OUT OF THE XRD9818



PIN DESCRIPTIONS

Pin #	Name	Type	Description
1	RED+	analog	RED Analog Positive Input
2	AGND	ground	ANALOG GROUND
3	AVDD	power	ANALOG VDD
4	LCLMP	clock	Line Clamp clock
5	VSAMP	clock	Video Sample clock
6	BSAMP	clock	Black Sample clock
7	ADCLK	clock	ADC clock
8	DGND	ground	Digital GROUND
9	LOAD	digital in	Serial Port Load
10	DVDD	power	Digital VDD
11	SDI	digital in	Serial Port Data Input
12	SCLK	clock	Serial Port Clock
13	ADCO[0]	output	ADC parallel out 0 (8-bit LSB)
14	ADCO[1]	output	ADC parallel out 1
15	ADCO[2]	output	ADC parallel out 2
16	ADCO[3]	output	ADC parallel out 3
17	ADCO[4]	output	ADC parallel out 4 (4-bit LSB)
18	ADCO[5]	output	ADC parallel out 5
19	ADCO[6]	output	ADC parallel out 6
20	ADCO[7]	output	ADC parallel out 7 (8-bit/4-bit MSB)
21	AVDD	power	ANALOG VDD
22	AGND	ground	ANALOG GROUND
23	CAPN	analog	ADC Reference By-Pass
24	CAPP	analog	ADC Reference By-Pass
25	CMREF	analog	Common Mode Reference for ADC
26	CMN-	analog	COMMON Analog Reference Negative Input
27	BLU+	analog	BLUE Analog Positive Input
28	GRN+	analog	GREEN Analog Positive Input

ELECTRICAL CHARACTERISTICS - XRD9818

AVDD=DVDD=3.3V, ADCLK=12MHZ, PGA GAIN=MIN, PIXEL RATE=4MHZ, TA=25C UNLESS OTHERWISE SPECIFIED

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
SYSTEM SPECIFICATIONS (INCLUDES CDS, PGA AND A/D)						
Differential Non-Linearity	DNL	-1.0	-0.9/+0.9	2.5	LSB	PGA Gain = min
Integral Non-Linearity	INL		50		LSB	PGA Gain = min
Output Noise Low Gain	N_{Min}		15		LSB_{rms}	PGA Gain = min, GS=0
Output Noise High Gain	N_{Max}		34		LSB_{rms}	PGA Gain = max, GS=0
System Offset Low Gain	SO_{Min}	-50	20	100	mV	PGA Gain = min
System Offset High Gain	SO_{Max}		20		mV	PGA Gain = max

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
VOLTAGE REFERENCE SPECIFICATIONS						
Vref(+)	CAPP	1.9	2.2	2.5	V	
Vref(-)	CAPN	0.5	0.7	0.9	V	
Delta Vref [Vref(+) - Vref(-)]	ΔVREF	1.25	1.5	1.75	V	
VCMREF	VCM	1.05	1.2	1.35	V	

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
CDS - S/H SPECIFICATIONS						
Input Switch-On Resistance	Ron		150		Ω	Clamp Enabled
Input Switch-Off Resistance	Roff	66	330		MΩ	Clamp Disabled
Internal Voltage Clamp	Vclmp1	2.8	3.0	3.125	V	CL[2:0]=110
Internal Voltage Clamp	Vclmp2	-0.1	0.0	0.1	V	CL[2:0]=001
Max Reset Pulse	Vrst	1.5			V	
Input Voltage Range	INVR		3.0 2.0		V V	GS=0 GS=1

ELECTRICAL CHARACTERISTICS (CONTINUED) - XRD9818

AVDD=DVDD=3.3V, ADCLK=12MHZ, PGA GAIN=MIN, PIXEL RATE=4MHZ, TA=25C UNLESS OTHERWISE SPECIFIED

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
OFFSET SPECIFICATIONS						
Fine Offset Range Min	FOFR-	-255	-180	-120	mV	
Fine Offset Range Max	FOFR+	+120	+180	+255	mV	
Fine Offset Step	FOF_{RES}		1.4		mV	8-bit (256 settings)
Fine Offset Range Linearity	FOFRL		+/-1.5		%FS	
Gross Offset Range Min	GOFR-	-260	-200	-150		
Gross Offset Range Max	GOFR+	+75	+100	+135		
Gross Offset Step	GOF_{RES}		100		mV	2-bit (4 setting)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
PGA SPECIFICATIONS						
Gain Range Min	GR_{Min}	0.84	1	1.2	V/V	default Gain Select, GS=0
Gain Range Max	GR_{Max}	4.5	5	6.20	V/V	default Gain Select, GS=0
Gain Resolution	G_{RES}	-10.0	7.8	-	mV/lsb	default Gain Select ,GS=0
Gain Range Min	GR_{Min}	1.3	1.5	1.7	V/V	Gain Select , GS=1
Gain Range Max	GR_{Max}	6.65	7.5	8.90	V/V	Gain Select , GS=1
Gain Resolution	G_{RES}		11.7		mV/lsb	Gain Select , GS=1

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
DIGITAL INPUT SPECIFICATIONS						
Valid Input Logic Low	V_{il}			0.5	V	
Valid Input Logic High	V_{ih}	2.60			V	
Low Level Input Current	I_{il}	-5	0.1	5	µA	
High Level Input Current	I_{ih}	10	65	150	µA	w/internal 50K pull down R's
Input Capacitance	C_{IN}		10		pf	

ELECTRICAL CHARACTERISTICS (CONTINUED) - XRD9818

AVDD=DVDD=3.3V, ADCLK=12MHZ, PGA GAIN=MIN, PIXEL RATE=4MHZ, TA=25C UNLESS OTHERWISE SPECIFIED

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
DIGITAL OUTPUT SPECIFICATIONS						
Valid Output Logic Low	V_{ol}			0.5	V	I_{Sink} = 2.0mA, C_L=10pf
Valid Output Logic High	V_{oh}	VDD-0.5			V	I_{Source} = 2.0mA, C_L=10pf
Tristate Leakage	IO_{Leak}	-10	0.1	+10	µA	

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
POWER SUPPLIES - 3 CHANNEL MODE						
Analog Power Supply	AVDD	3.0	3.3	3.6	V	
Digital Power Supply	DVDD	3.0	3.3	3.6	V	
Analog IDD	I_{AVDD}	30	57	70	mA	AVDD = DVDD = 3.6V
Digital IDD	I_{DVDD}	0.1	7	20	mA	AVDD = DVDD = 3.6V
IDD Total	IDD	31	64	90	mA	AVDD = DVDD = 3.6V
Power Dissipation	PD	112	230	325	mW	AVDD = DVDD = 3.6V
Power Down Current	IDD_{PDN}		0.2	1.3		

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
POWER SUPPLIES - 1 CHANNEL MODE						
Analog Power Supply	AVDD	3.0	3.3	3.6	V	
Digital Power Supply	DVDD	3.0	3.3	3.6	V	
IDD Total	IDD		40		mA	AVDD = DVDD = 3.6V
Power Dissipation	PD		145		mW	AVDD = DVDD = 3.6V
Power Down Current	IDD_{PDN}		0.2	1.3	mA	

ELECTRICAL CHARACTERISTICS (CONTINUED) - XRD9818

AVDD=DVDD=3.3V, ADCLK=12MHZ, PGA GAIN=MIN, PIXEL RATE=4MHZ, TA=25C UNLESS OTHERWISE SPECIFIED

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
SERIAL PORT WRITE TIMING SPECIFICATIONS						
Data Setup Time	Tds	10			ns	
Data Hold Time	Tdh	10			ns	
Load Setup Time	Tls	10		∞	ns	
Load Hold Time	Tlh	10			ns	
SCLK Period	Tsclk	125			ns	
Load Pulse High Period	Tlpw	125			ns	1 SCLK period

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
TIMING SPECIFICATIONS						
ADCLK Duty Cycle	daclk		50		%	
ADCLK Period	tcp3b tcp3n tcp2b tcp2n tcp1b tcp1n	83.3 41.7 83.3 41.7 125 62.5			ns ns ns ns ns ns	3-CH, 8bit (byte) output 3-CH, 4bit (nibble) output 2-CH, 8bit (byte) output 2-CH, 4bit (nibble) output 1-CH, 8bit (byte) output 1-CH, 4bit (nibble) output
Conversion Period	tcr3 tcr2 tcr1	250 167 125			ns ns ns	3-Channel Mode 2-Channel Mode 1-Channel Mode
BSAMP Pulse Width	tpwb	15	30		ns	
VSAMP Pulse Width	tpwv	15	30		ns	
VSAMP ↓ edge delay from rising ADCLK	tvfcr	12			ns	
Settling time	tstl	15			ns	
Aperture Delay	tap		3		ns	
Output Delay	todv		12		ns	
Latency	lat		9 18		ADCLK cycles	B/N=0 (byte mode) B/N=1 (nibble mode)

PRODUCT DESCRIPTION

1.0 INTRODUCTION

The XRD9818 contains all of the circuitry required to create a complete 3-channel signal processor/digitizer for use in CCD/CIS imaging systems. It can be configured to operate in a 3-CH rotating (RGB), 2-CH rotating (RG, GR, GB or BR), or a 1-CH fixed (R, G or B) mode.

Each channel includes a correlated-double-sampler/sample-hold (CDS/SH), channel offset adjustment and programmable gain amplifier (PGA). After signal conditioning the channel outputs are multiplexed and digitized by a 16-bit A/D converter.

The XRD9818 has selectable 8-bit (byte) or 4-bit (nibble) data output modes. The ADCLK runs up to 12MHz in the 8-bit data output mode or 24MHz in the 4-bit data output mode.

In order to maximize flexibility, the specific operating mode is programmable through internal configuration registers. In addition, the offset and gain of each channel can be independently programmed through separate offset and gain registers. The configuration, offset and gain register information is loaded through a 3-pin serial interface.

2.0 MODES OF OPERATION

2.1 3-CH CCD Mode

In 3-CH mode the XRD9818 simultaneously samples the red, green and blue channel inputs. The CDS extracts the video information which corresponds to the difference between the sample black reference and video level for each pixel. The black reference level is sampled on the falling edge of BSAMP and the video level is sampled on the falling edge of VSAMP. This information is then level shifted and gained up according to the contents of the Offset and PGA registers respectively. The data is then sequentially converted (Red $\rightarrow$ Green $\rightarrow$ Blue) by a 16-bit A/D converter.

In CCD mode, each channel input is sampled with respect to the CMN- input. This provides a sudo-differential input. Typically the CMN- input is connected to the CCD ground through a capacitor. This coupling capacitor should be at least 3 times the capacitor value used to couple the RED+, GRN+ and BLU+ inputs.

The timing for this mode is shown in Figure 15.

2.2 2-CH CCD Mode

The 2-CH mode operates identically to the 3-CH CCD mode except that only 2 channels are actively used to process CCD output signals. The two channels to be used and the order in which they process data is determined from the configuration of the Input-Mux/Channel-Select bits (CH[2:0]) located in the Mode 1 register. There are four possible 2-CH configurations, RG, GR, GB and BR. To conserve power that channel not being utilized is powered down.

The timing for this mode is shown in Figure 16.

2.3 1-CH CCD Mode

The 1-CH mode operates identically to the 3-CH or 2-CH CCD modes except that the channel sampled is fixed to only one input. The channel selection is set by the Input-Mux/Channel-Select bits (CH[2:0]) located in the Mode 1 register. There are three possible one channel modes: R, G or B. The channels not being used will be powered down to conserve power.

The timing for this mode is shown in Figure 17.

2.4 3-CH CIS Mode

In this mode the XRD9818 simultaneously samples (S/H) the red, green and blue channel inputs. The video level is sampled on the falling edge of VSAMP. Each channels S/H extracts the video information from each pixel. This data is level shifted and gained up according to the contents of the Offset and PGA registers respectively. The data is then sequentially converted (Red → Green → Blue) by a 16-bit A/D converter.

In CIS mode, each channel input is sampled with respect to the voltage at the CMN- input. The voltage at CMN- can be either generated by a programmable internal reference (C/R DAC) or supplied by an external source.

The timing for this mode is shown in Figure 18.

2.5 2-CH CIS Mode

The 2-CH mode operates identically to the 3-CH CIS mode except that only 2 channels are actively used to process CIS output signals. The two channels to be used and the order in which they process data is determined from the configuration of the Input-Mux/Channel-Select bits (CH[2:0]) located in the Mode 1 register. There are four possible 2-CH configurations, RG, GR, GB and BR. To conserve power the channel not being utilized is powered down.

2.6 1-CH CIS Mode

The 1-CH mode operates identically to the 3-CH or 2-CH CIS modes except that the channel sampled is fixed to only one input. The channel selection is set by the Input-Mux/Channel-Select bits (CH[2:0]) located in the Mode 1 register. There are three possible one channel modes: R, G or B. The channels not being used will be powered down.

3.0 REGISTER MAP

INTERNAL REGISTER MAP

Register Name	Address				Data Bits									
	A3	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RED Gain	0	0	0	0	msb								lsb	
GREEN Gain	0	0	0	1	msb								lsb	
BLUE Gain	0	0	1	0	msb								lsb	
RED Offset	0	0	1	1	COR[1]	COR[0]	FOR[7]	FOR[6]	FOR[5]	FOR[4]	FOR[3]	FOR[2]	FOR[1]	FOR[0]
GREEN Offset	0	1	0	0	COG[1]	COG[0]	FOG[7]	FOG[6]	FOG[5]	FOG[4]	FOG[3]	FOG[2]	FOG[1]	FOG[0]
BLUE Offset	0	1	0	1	COB[1]	COB[0]	FOB[7]	FOB[6]	FOB[5]	FOB[4]	FOB[3]	FOB[2]	FOB[1]	FOB[0]
MODE 1	0	1	1	0	CH[2]	CH[1]	CH[0]	GS	LC	CCD_{EN}	B/N	C/R[2]	C/R[1]	C/R[0]
MODE 2	0	1	1	1	PD	OE					L_{pol}	ADC_{pol}	B_{pol}	V_{pol}
$BSAMP_{Delay}$	1	0	0	0	BL[4]	BL[3]	BL[2]	BL[1]	BL[0]	BT[4]	BT[3]	BT[2]	BT[1]	BT[0]
$VSAMP_{Delay}$	1	0	0	1	VL[4]	VL[3]	VL[2]	VL[1]	VL[0]	VT[4]	VT[3]	VT[2]	VT[1]	VT[0]
$ADCLK_{Delay}$	1	0	1	0	A[4]	A[3]	A[2]	A[1]	A[0]	DO[4]	DO[3]	DO[2]	DO[1]	DO[0]
TEST	1	0	1	1	*	*	*	*	*	*	*	*	*	*
RESET/RB	1	1	1	1	Reset	READ					RB[3]	RB[2]	RB[1]	RB[0]

Note: * Exar test bits, do not over write the default values.

Shaded cells represent unused bits.

3.1 PGA Gain Registers

There are three PGA registers for individually programming the gain in the RED, GREEN, and BLUE channels. Each gain register has 9 bits of resolution. Bits D[9:1] control the gain while bit D0 is N/A (don't care). The XRD9818 has two gain ranges to help interface to imagers that have 3V or 2V of output signal swing. The GS bit, located in the MODE 1 register, defaults to GS=0 for a gain of 1x to 5x or if GS=1 the gain would be 1.5x to 7.5x. The gain range of 1 to 5x (GS=0) is intended for use with imagers that have a 3V output swing, while the gain range 1.5 to 7.5x is intended for imagers with 2V or less of output swing. The coding for the PGA registers is straight binary. See "Section 4.3, Programmable Gain" on page 20 for a functional description of the XRD9818's gain stage.

GAIN REGISTER SETTINGS

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Gain (V/V)	Gain (V/V)
msb								lsb	N/A	w/GS bit = 0*	w/GS bit = 1
000000000* … 111111111									not used	1x … 5x	1.5x … 7.5x

* Power-on default value

3.2 Offset Registers

There are three Offset registers for individual control of the offsets applied to the RED, GREEN, and BLUE channels. There are separate course and fine controls to set the desired offset compensation for each channel. Bits D9 and D8 set the course offset from -100mV to +200mV in 100mV increments. Bits D7:D0 set the fine offset range from -180mV to +180mV in 1.4mV increments. The polarity of the offset correction is defined as positive for the normal direction in which offsets occur in an imager, see Figure 11. Please see “Section 4.2, Programmable Offset Adjust” on page 19 for a description of the XRD9818’s offset correction circuitry.

OFFSET REGISTER SETTINGS

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
COx[1]	COx[0]	FOx[7]	FOx[6]	FOx[5]	FOx[4]	FOx[3]	FOx[2]	FOx[1]	FOx[0]
Course offset control 00* → 0mV 01→ -100mV 10 → 100mV 11 → 200mV		Fine offset control 01111111 → 150mV … 00000000* → 0mV 10000000 → 0mV … 11111111 → -150mV							

* Power-on default value

3.3 Mode Registers

There are two mode registers that control the configuration and operation of the XRD9818. The Mode 1 register controls the configuration of input mux mode, gain range, Line Clamp enable, CCD or CIS select, byte or nibble data output mode and clamp level select. The Mode 2 register controls the power down, output enable and polarities of the input timing signals.

MODE 1 REGISTER SETTINGS

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CH[2]	CH[1]	CH[0]	GS	LC	CCD_{EN}	B/N	C/R[2]	C/R[1]	C/R[0]
000* → 3CH (RGB) 001 → RED channel 010 → GRN channel 011 → BLU channel 100 → 2CH (RG) 101 → 2CH (GR) 110 → 2CH (GB) 111 → 2CH (BR)			0* → 1x to 5x 1 → 1.5x to 7.5x	0* → Line Clamp Off 1 → Line Clamp On	0* → CCD 1 → CIS	0 → byte output mode 1* → nibble output mode	000 → high Z 001 → 0V 010 → 1.25V 011 → 2.0V 100 → 2.6V 101 → 2.8V 110* →3.0V 111 → VDD		

* Power-on default value

CH[2:0] - Input Mux/Channel select. Selects between 3-CH (RGB), 1-CH RED, 1-CH GRN, 1-CH BLU, 2-CH (RG), 2-CH (GR), 2-CH (GB) or 2-CH (BR) input mux modes.

GS - Gain Range Select. Gain range 1x to 5x for 3V input signals, range 1.5x to 7.5x for 2V signals.

LC- Line Clamp enable. Gates clamping function with the timing signal LCLMP.

CCD_{EN} - CCD enable. Defines operation for a CCD or CIS imager input.

B/N - Byte or Nibble output mode. Defines 8bit (byte) or 4bit (nibble) data output format.

C/R[2:0] - Clamp/Reference Select. The setting determines the clamp/reference voltage applied to the CMN- input. The settings 2.0V through VDD are intended for use in CCD applications. The 0V, 1.25V or "high Z" settings are intended for use for CIS applications. If "high Z" is selected an external source can be applied to CMN- for the reference. For a description of the C/R DAC please See “Section 4.1.2, Clamp/Reference (C/R) DAC” on page 17.

MODE 2 REGISTER SETTINGS

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PD	OE	N/A	N/A	N/A	N/A	L_{POL}	ADC_{POL}	B_{POL}	V_{POL}
0* → Normal Operation 1 → PWR Down	0* → Normal Operation 1 → Data bus tri-stated	Not used	Not used	Not used	Not used	0*→ Non-Inverted 1 → Inverted	0*→ Non-Inverted 1 → Inverted	0*→ Non-Inverted 1 → Inverted	0*→ Non-Inverted 1 → Inverted

* Power-on default lt value

PD - Power Down. Does not affect the internal register settings but does power down the entire part excluding the serial interface. There will be some power up settling time required to reestablish the ADC reference, CAPP and CAPN, voltages.

OE - Output Enable. Tristate control for the output data bus.

L_{POL} - LCLMP input polarity select. (Noninverting pol ⇒ active high, inverted pol ⇒ active low)

ADC_{POL} - ADCLK polarity select. (Noninverting pol ⇒ begins high, inverted pol ⇒ begins low)

B_{POL} - BSAMP polarity select. (Noninverting pol ⇒ active high, inverted pol ⇒ active low)

V_{POL} - VSAMP polarity select. (Noninverting pol ⇒ active high, inverted pol ⇒ active low)

3.4 BSAMP Delay Register

The BSAMP Delay register controls the internal delays added to the leading and the trailing edges of the BSAMP timing signal. The width and position of the BSAMP pulse can be adjusted through the leading and trailing edge delay settings. This is useful to match the sampling requirements of the incoming CCD waveform.

BSAMP DELAY REGISTER SETTINGS

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BL[4]	BL[3]	BL[2]	BL[1]	BL[0]	BT[4]	BT[3]	BT[2]	BT[1]	BT[0]
BSAMP Leading edge delay 00000* → 0ns 00001 → 1ns … 11110 → 30ns 11111 → 31ns					BSAMP Trailing edge delay 00000* → 0ns 00001 → 1ns … 11110 → 30ns 11111 → 31ns				

* Power-on default value

BL[4:0] - Sets the amount of delay added to the leading edge of BSAMP.

BT[4:0] - Sets the amount of delay added to the trailing edge of BSAMP.

3.5 VSAMP Delay Register

The VSAMP Delay register controls the internal delays added to the leading and the trailing edges of the VSAMP timing signal. The width and position of the VSAMP pulse can be adjusted through the leading and trailing edge delay settings. This is useful to match the sampling requirements of the incoming CCD/CIS waveform.

VSAMP DELAY REGISTER SETTINGS

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VL[4]	VL[3]	VL[2]	VL[1]	VL[0]	VT[4]	VT[3]	VT[2]	VT[1]	VT[0]
VSAMP Leading edge delay 00000* → 0ns 00001 → 1ns … 11110 → 30ns 11111 → 31ns					VSAMP Trailing edge delay 00000* → 0ns 00001 → 1ns … 11110 → 30ns 11111 → 31ns				

* Power-on default value

VL[4:0] - Sets the amount of delay added to the leading edge of VSAMP.

VT[4:0] - Sets the amount of delay added to the trailing edge of VSAMP.

3.6 ADCLK Delay Register

The ADCLK Delay register controls the delay added to the ADCLK timing signal and Data Output.

ADCLK DELAY REGISTER SETTINGS

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A[4]	A[3]	A[2]	A[1]	A[0]	DO[4]	DO[3]	DO[2]	DO[1]	DO[0]
ADCLK delay 00000* → 0ns 00001 → 1ns … 11110 → 30ns 11111 → 31ns					Output Data valid delay 00000* → 0ns 00001 → 0.5ns … 11110 → 15.0ns 11111 → 15.5ns				

* Power-on default value

A[4:0] - Sets the amount of internal delay added to the ADCLK signal.

DO[4:0] - Sets the amount of delay from internal ADCLK to valid data out.

3.7 Test Register

The TEST register is used for EXAR internal test requirements. Do not over write this register.

TEST REGISTER SETTINGS

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Test Only	Test Only	Test Only	Test Only	Test Only	Test Only	Test Only	Test Only	Test Only	Test Only
00000000* → Do not modify									

* Power-on default value

3.8 Reset and ReadBack Register

This register controls the reset and readback function of the XRD9818. The part can be reset to its power-up default state by writing to the RESET bit. This will reset all register contents to their default state, reset the serial port contents and counters and configure the input mux to the red input channel. The XRD9818 will automatically recover approximately 10ns after the RESET bit is set high. After the reset recovery the register contents will be reset to their default conditions and the RESET bit will be set back to a low. The readback function is controlled through this register also. The READ bit simply enables the readback function. When the READ bit is set high the contents of the register pointed to by the address in RB[3:0] is put out on the data output bus. The register contents are output to the 10 LSB's and the 6 MSB's are padded with zeros. The output data format is set to either Byte or Nibble format as controlled by the B/N bit (D3) in the MODE 1 register. The register contents will continually be output to the data bus until the readback bit is set low.

RESET/READBACK REGISTER

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reset	Read	N/A	N/A	N/A	N/A	RB[3]	RB[2]	RB[1]	RB[0]
0* → Normal Operation 1 → Reset Device	0* → Normal Operation 1 → Readback Enabled	Not used	Not used	Not used	Not used	Address of register to be read 0000* → RED Gain register 0001 → GREEN Gain register … 1111 → RESET/RB register			

* Power-on default value

Reset - Returns all internal register values back to their default settings.

Read - Readback enable.

RB[3:0] - Readback register address. Points to the internal register of interest to be read.

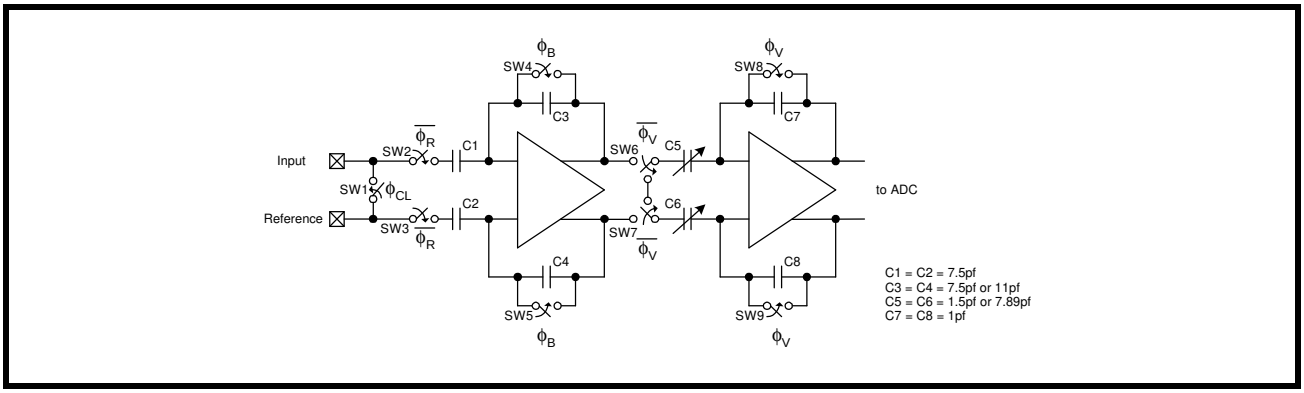
4.0 CIRCUIT OPERATION

4.1 Analog Inputs

4.1.1 Sampling

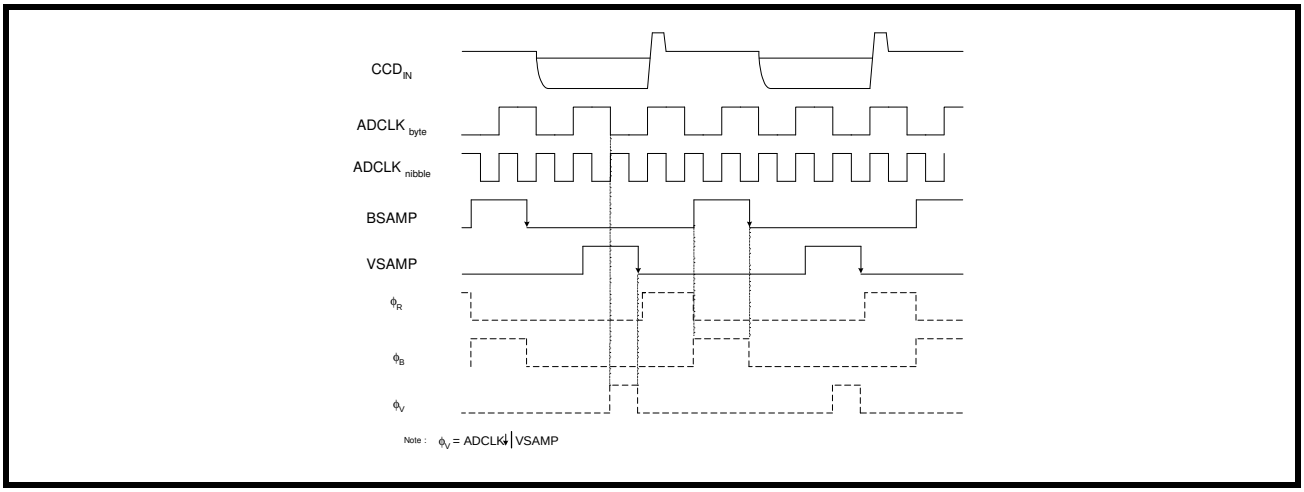
The XRD9818's analog front end (AFE) uses a switched capacitor network to achieve a correlated double sample (CDS) of the input in CCD mode or a sample and hold (S/H) of the input in CIS mode. Figure 3 shows the 9818's AFE (CDS/SH + PGA) which samples and gains the input signal. Figure 4 shows the external and internal timing requirements to achieve a correlated double sample and gain of a CCD input signal.

FIGURE 3. XRD9818 INPUT CIRCUITRY



In addition to sampling and gaining the CCD signal the 9818 input is designed to reject the reset pulse noise present also. The XRD9818 can withstand reset pulses up to 1.5V or more depending upon the input conditions. The timing signal ϕ_R controls SW2 and SW3 is generated internally by the XRD9818. SW2 and SW3 open after a short delay following the sampling edge of VSAMP and close at the leading edge of BSAMP.

FIGURE 4. INTERNAL AFE SAMPLE TIMING (EX. 3CH CCD MODE)



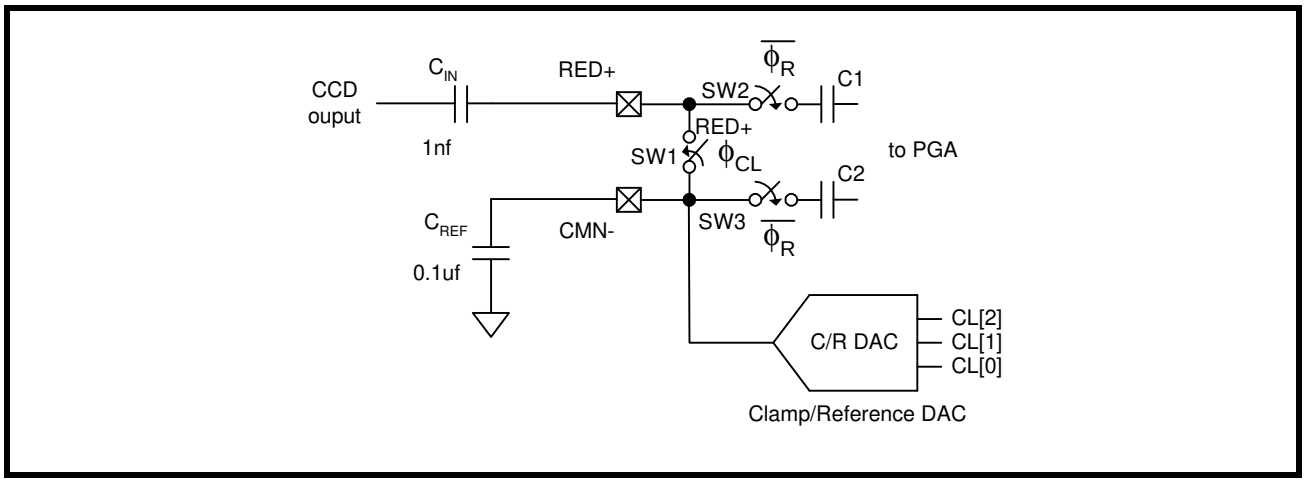
The XRD9818 utilizes a differential input and signal path which samples the CCD reference level on capacitors C1 and C2. When ϕ_B goes high, SW4 and SW5 close storing the CCD reference level on C1 and C2. When ϕ_B goes low a fixed gain is applied to the input signal as it tracks the video input. When ϕ_V goes high the video content is applied to capacitors C5 and C6. The final video level is stored on C5 and C6 when ϕ_V goes low. The video content is then amplified again and sampled by the ADC at the proper time

4.1.2 Clamp/Reference (C/R) DAC

4.1.2.1 Clamp Operation in CCD Mode

In CCD mode a clamp is required to level shift the CCD output signal into XRD9818's input common mode range. The clamp circuitry ensures that the signals present at the analog inputs fall within the operating range of those pins. The clamp operation takes place while BSAMP is active. When BSAMP is active, SW1 is closed connecting the C/R DAC to the analog input pin. This establishes the C/R DAC voltage on the external coupling cap. When SW1 is opened, the C/R DAC voltage is stored on the external coupling cap. This clamping operation will occur while BSAMP is active. The C/R DAC clamp voltage is programmable. This gives the system designer added flexibility to make adjustments for different sensor signal swing and reset pulse characteristics.

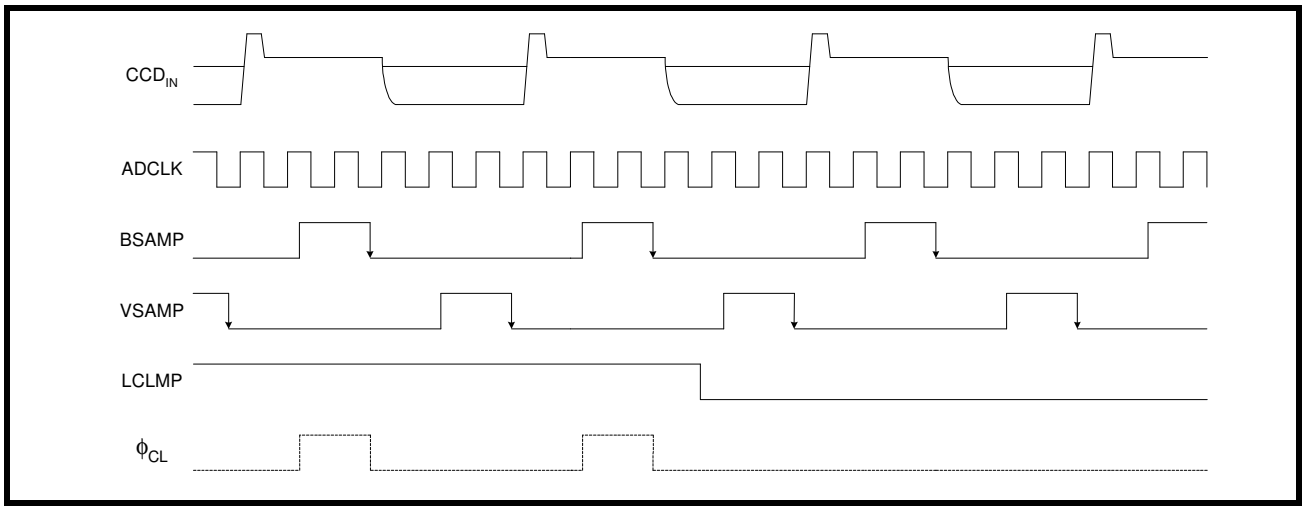
FIGURE 5. CCD MODE INPUT CLAMP (ALL THREE CHANNELS ARE IDENTICAL)



The XRD9818 has 2 clamp modes available for used in CCD applications, Line Clamp and Pixel Clamp.

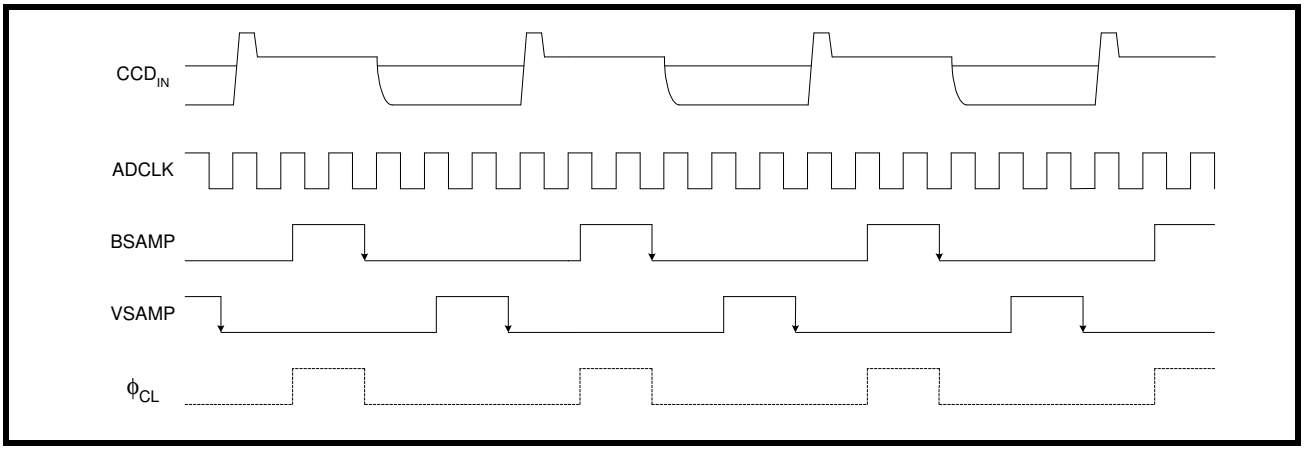
Line Clamp mode only performs the clamp when the LCLMP pin is active. The control timing, ϕ_{CL}, for SW1 is generated by the "ANDing" of the external timing signals LCLMP & BSAMP and is shown in Figure 6.

FIGURE 6. LINE CLAMP MODE TIMING



Pixel Clamp mode eliminates the gating function of BSAMP with LCLMP. In Pixel Clamp mode the clamping function is performed with every BSAMP, see Figure 7. Selection of the Line Clamp or Pixel Clamp modes is defined by the state of the LC bit (D5) located in the MODE 1 register.

FIGURE 7. PIXEL CLAMP MODE TIMING

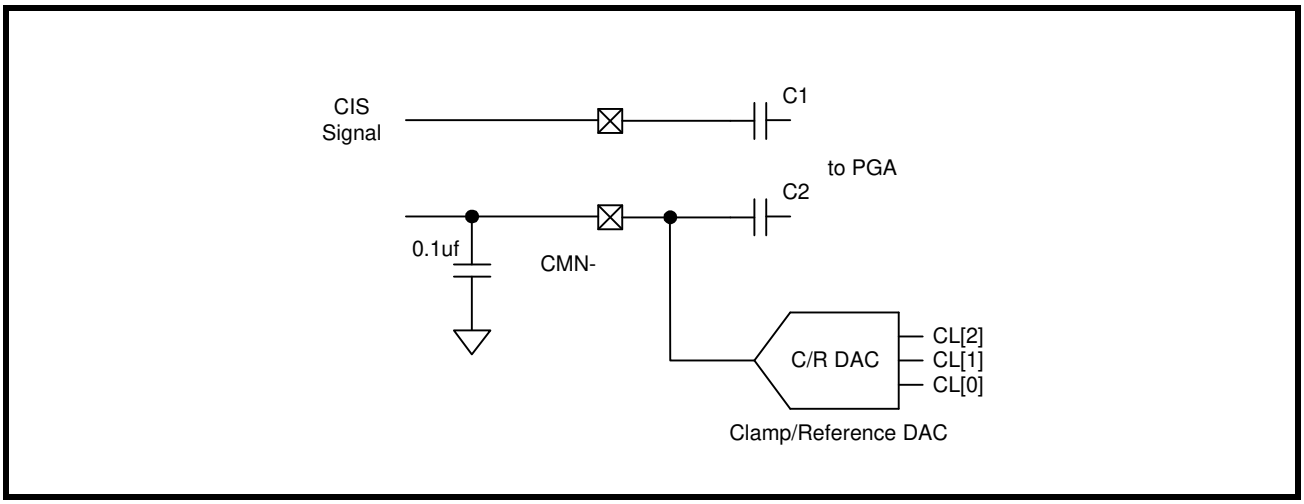


4.1.2.2 Reference Operation in CIS Mode

In most CIS applications the imager output is connected directly to the inputs. With no external coupling capacitor, there is no need to perform a clamp. Unlike a CCD output signal that has a black reference level for each pixel a CIS output is sampled with respect to a black reference voltage. In CIS mode, the C/R DAC is used to provide that reference as shown below in Figure 8. The reference voltage is programmable to help interface to a variety of CIS imagers.

If a CIS imager provides its own reference voltage the C/R DAC can be configured into a "high Z" state so that an external reference can be connected directly to the CMN- pin. See the MODE 1 Register definition of bits C/R[2:0].

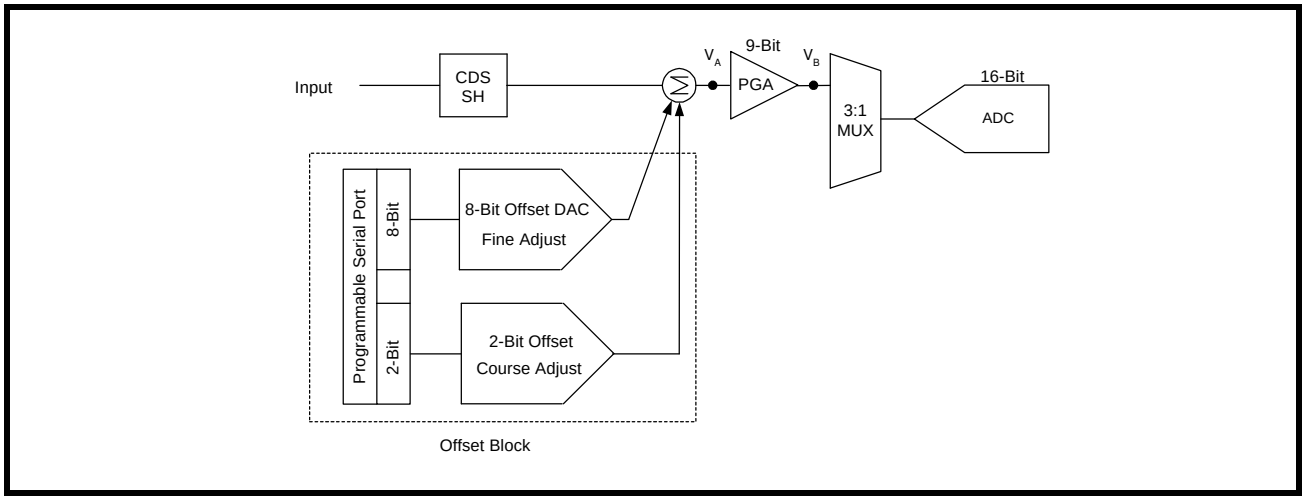
FIGURE 8. CIS MODE REFERENCE (INTERNAL OR EXTERNAL)



4.2 Programmable Offset Adjust

The offset adjustment circuitry of the XRD9818 is designed to compensate for any offsets present in the CCD or CIS output signal and/or overall scanner system. The total range of compensation available is -280mV to +380mV. This is achieved via a 10-bit Offset DAC that applies gain independent offset correction. The 10-bits of control is broken into 2 ranges, course and fine. There are 2 bits of course control that is designed to remove offsets in 100mV increments. The remaining 8-bits determine the fine control and has a range of +/-180mV in 1.4mV increments. Each channel has its own independent offset control.

FIGURE 9. XRD9818 CHANNEL OFFSET BLOCK DIAGRAM

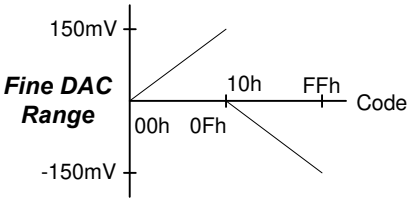


The offset correction range of both the Course and Fine DAC's are shown in Figure 10. The Course DAC has four settings: 0mv, -100mV, 100mV and 200mV. The 2 msb's, D[9:8], select the desired course offset setting. The Fine DAC has a range of +/-180mV. The Offset registers 8 lsb's, D[7:0], select the desired fine setting. Bits D[6:0] program the magnitude while D[7] selects the polarity of the Fine DAC's compensation.

FIGURE 10. OFFSET CORRECTION (COURSE & FINE DAC'S)

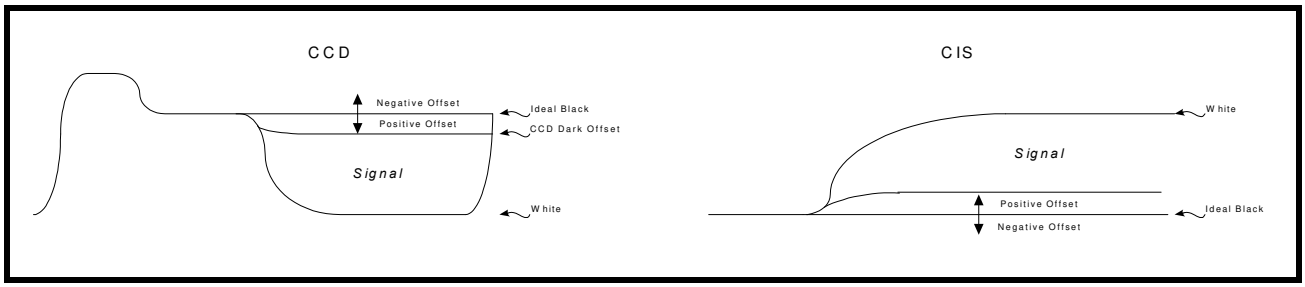
Course DAC Settings

COx[1:0]	Offset (mV)
00	0
01	-100
10	100
11	200



As can be seen in the Course Offset DAC's range settings there is more correction range in the positive direction. This allows the system designer to maximize the usable offset correction range of the XRD9818 for a variety of imagers. Positive offset is defined as the normal offset direction found in either a CCD or CIS input signal, as shown in Figure 11.

FIGURE 11. SIGNAL OFFSET POLARITY (CCD AND CIS)



The affect of the XRD9818's offset correction DAC's (Course & Fine) is defined as follows:

$$V_A = V_{Input} - (VOS_{Course} + VOS_{Fine}) \quad \textit{note: positive offset values subtract from the input signal}$$

The course DAC value, VOS_{COURSE}, is defined in Figure 10 and the Fine DAC value is determined as follows:

$$VOS_{Fine} = FBx[7] \times \left[\frac{Offset\ Code\ (FBx[6:0])}{127}\right] \times 150mV \qquad Note : FB[7] = 0 \rightarrow (+),\ FB[7] = 1 \rightarrow (-)$$

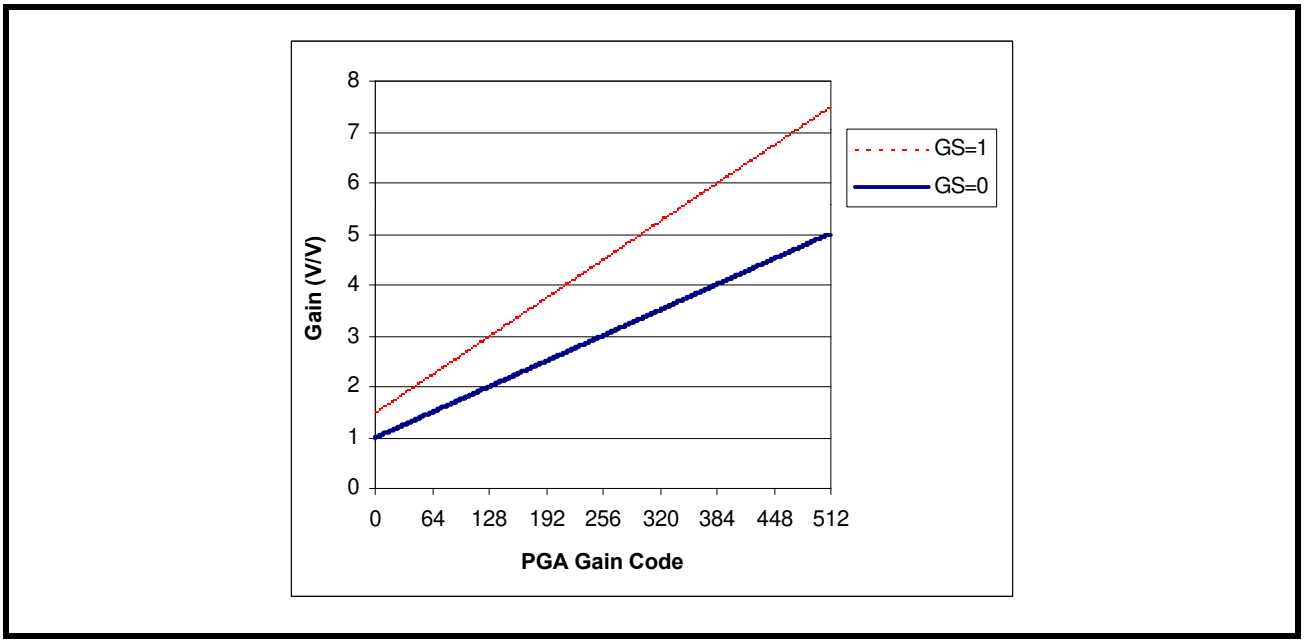
The XRD9818 offset adjustment range is designed to maximize the correction range whether being used in a CCD or CIS application.

4.3 Programmable Gain

There are three independent PGA's, one for each input channel: Red, Green and Blue. The individual gain values are controlled by separate Red, Green and Blue gain registers. Each PGA has 9 bits of control for the full gain range. See Figure 12 for the PGA transfer function. The gain increments in a binary fashion from a minimum at code 0 to a maximum at code 511.

The PGA has two gain ranges 1x to 5x and 1.5x to 7.5x to help interface to imagers with 3V or 2V outputs respectively. To select the 1x to 5x gain range for an imager that has a 3V single swing the GS bit in the MODE 1 register must be set low, GS=0 (default). To select the 1.5x to 7.5x gain range for use with imagers that have a 2V maximum signal swing the GS bit in the MODE 1 register must be set high, GS=1.

FIGURE 12. XRD9818 PGA TRANSFER FUNCTION



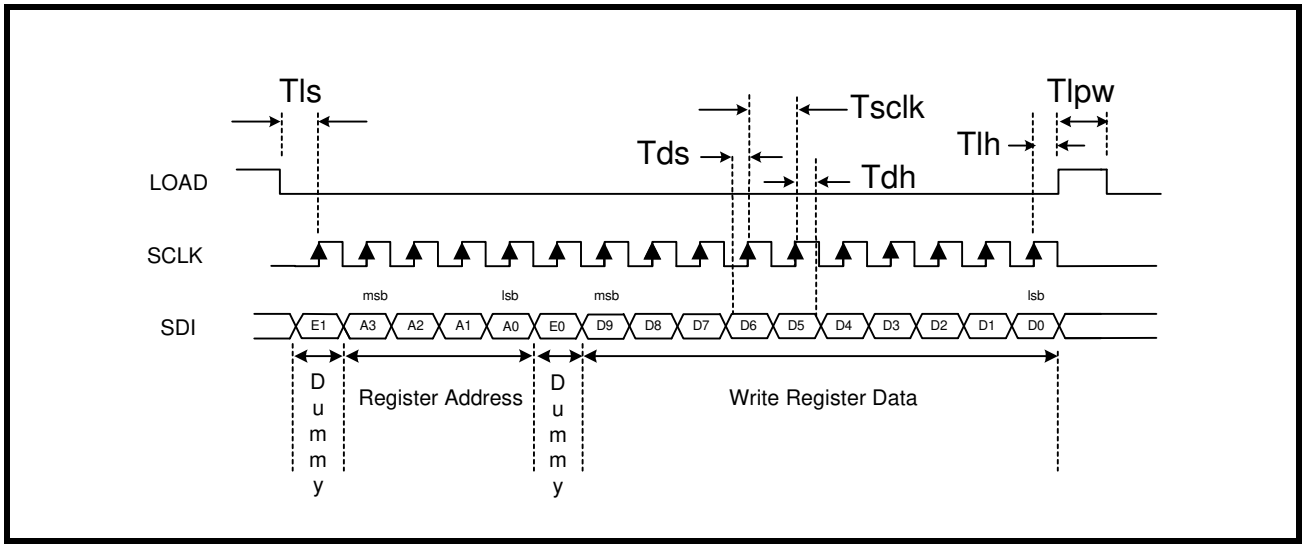
The XRD9818 channel gain equations are as follows:

$$Gain_{1\ to\ 5} = 4 \times \left[\frac{Gain\ Code}{511}\right] + 1 \qquad \text{or} \qquad Gain_{1.5\ to\ 7.5} = 6.0 \times \left[\frac{Gain\ Code}{511}\right] + 1.5$$

5.0 SERIAL PORT INTERFACE

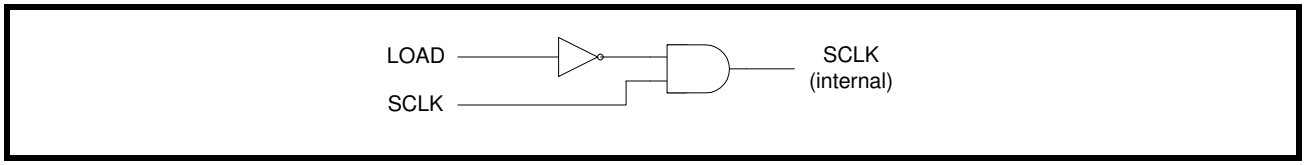
The XRD9818 can be configured through a three pin interface (LOAD, SDI, and SCLK) with the serial port write timing shown below. Each write will include 4 bits of address, two dummy bits and 10 bits of data. To insure a valid write operation, the serial port control must detect minimum of 16 rising SCLK edges. Upon a valid write the XRD9818 will latch the last 16 bits of data presented at the rising edge of LOAD. The register address will be decoded and the 10bits of data will over write the contents of the addressed register. The LOAD setup time "Tls" can be indefinitely long.

FIGURE 13. SERIAL PORT WRITE TIMING



LOAD is used to gate the SCLK input into the XRD9818. In order to eliminate any unintended high speed clocks into the part it is recommended that the LOAD signal only be active during the write operation.

FIGURE 14. LOAD GATING OF SCLK



6.0 TIMING

FIGURE 15. 3-CH CCD MODE SYSTEM TIMING (BYTE & NIBBLE MODES)

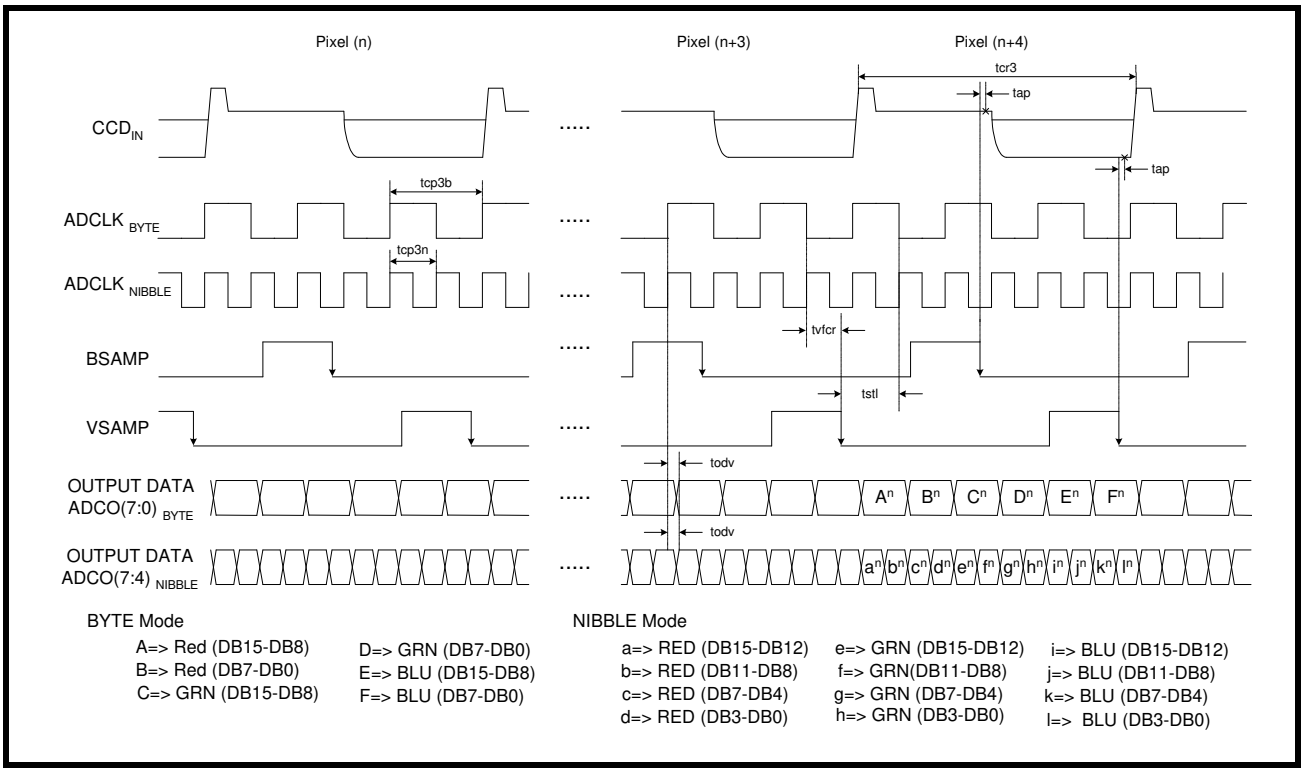


FIGURE 16. 2-CH CCD MODE SYSTEM TIMING (BYTE & NIBBLE MODES)

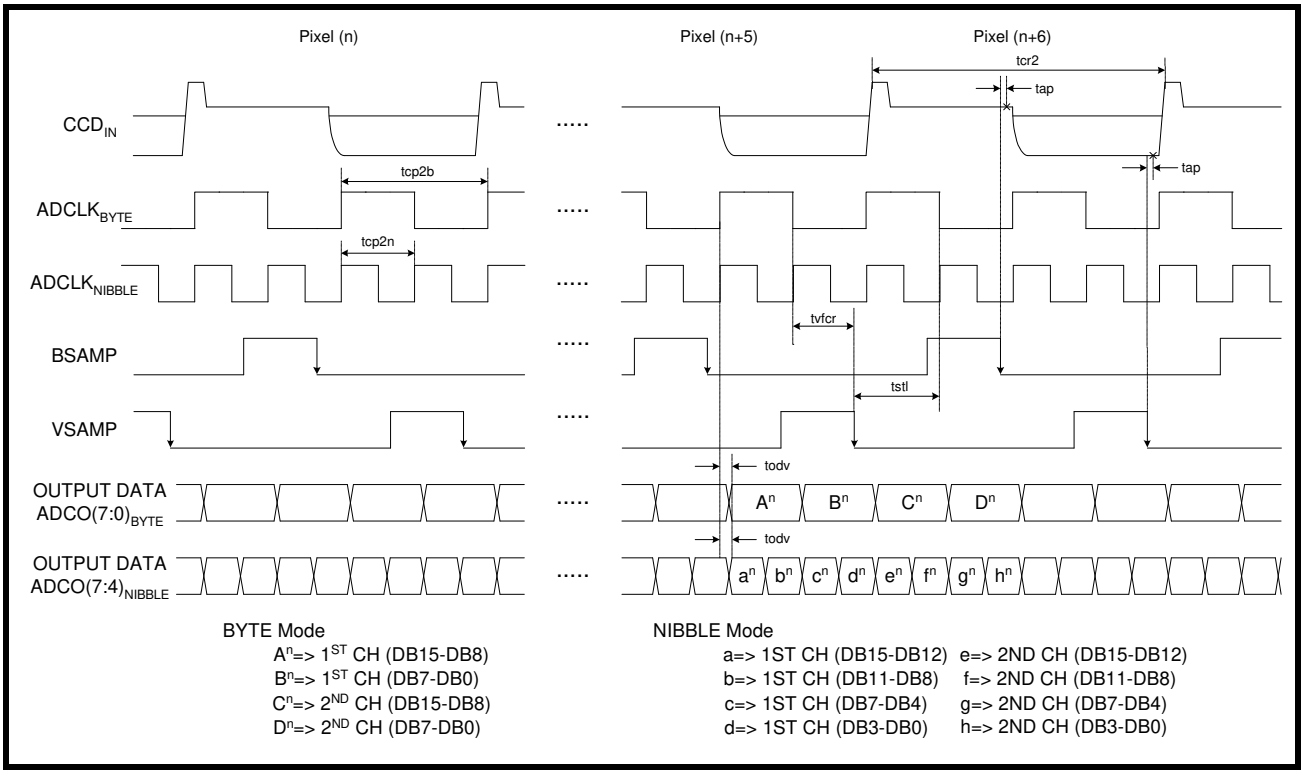


FIGURE 17. 1-CH CCD MODE SYSTEM TIMING (BYTE & NIBBLE MODES)

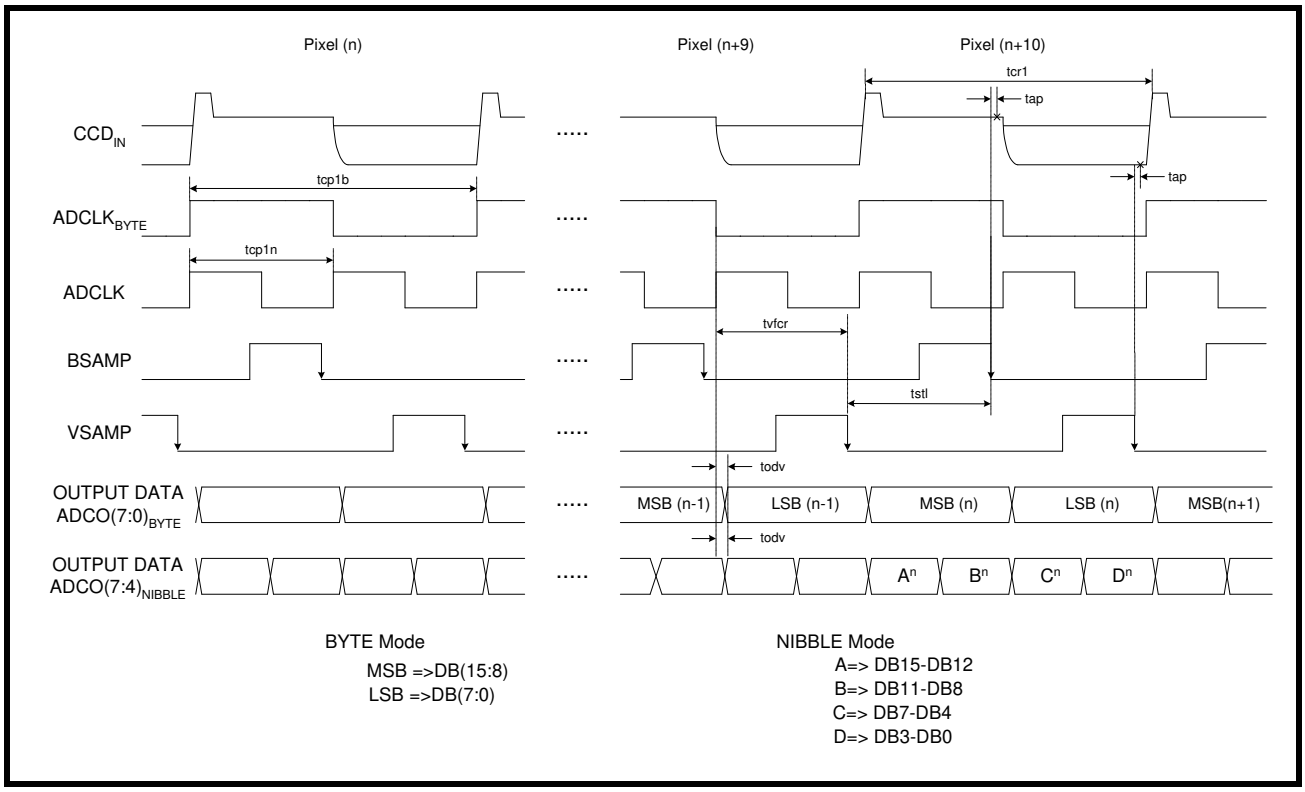
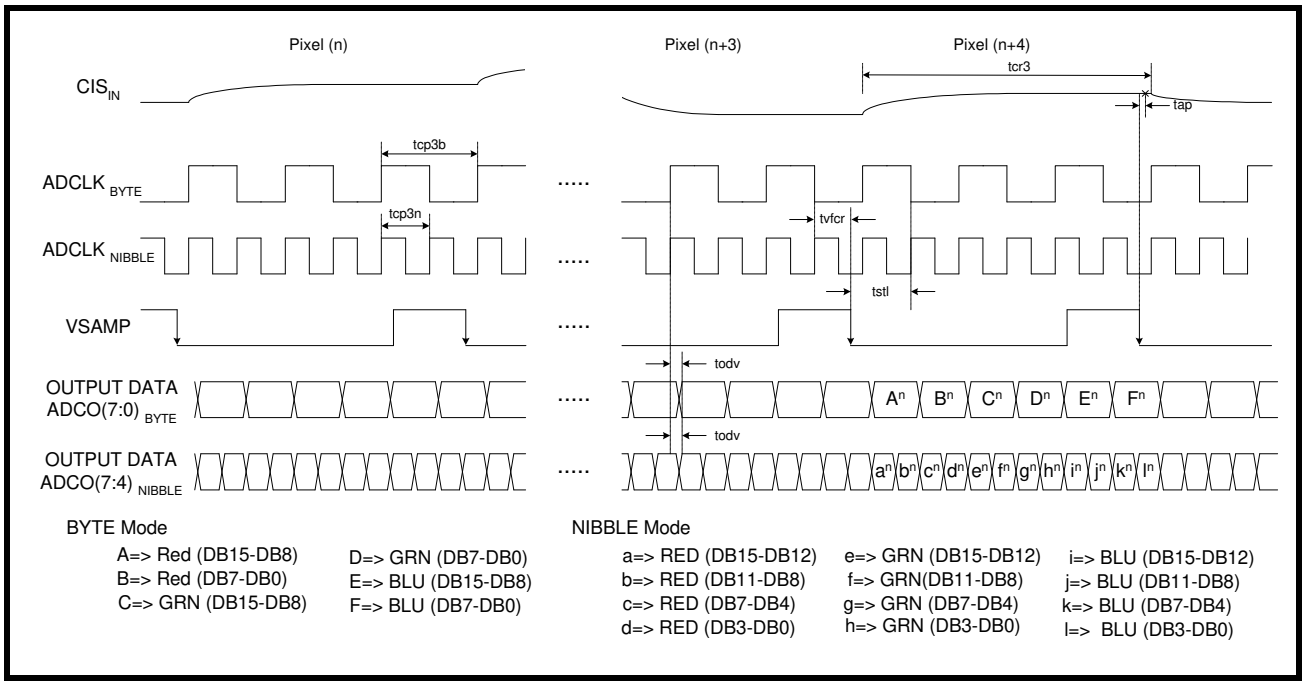
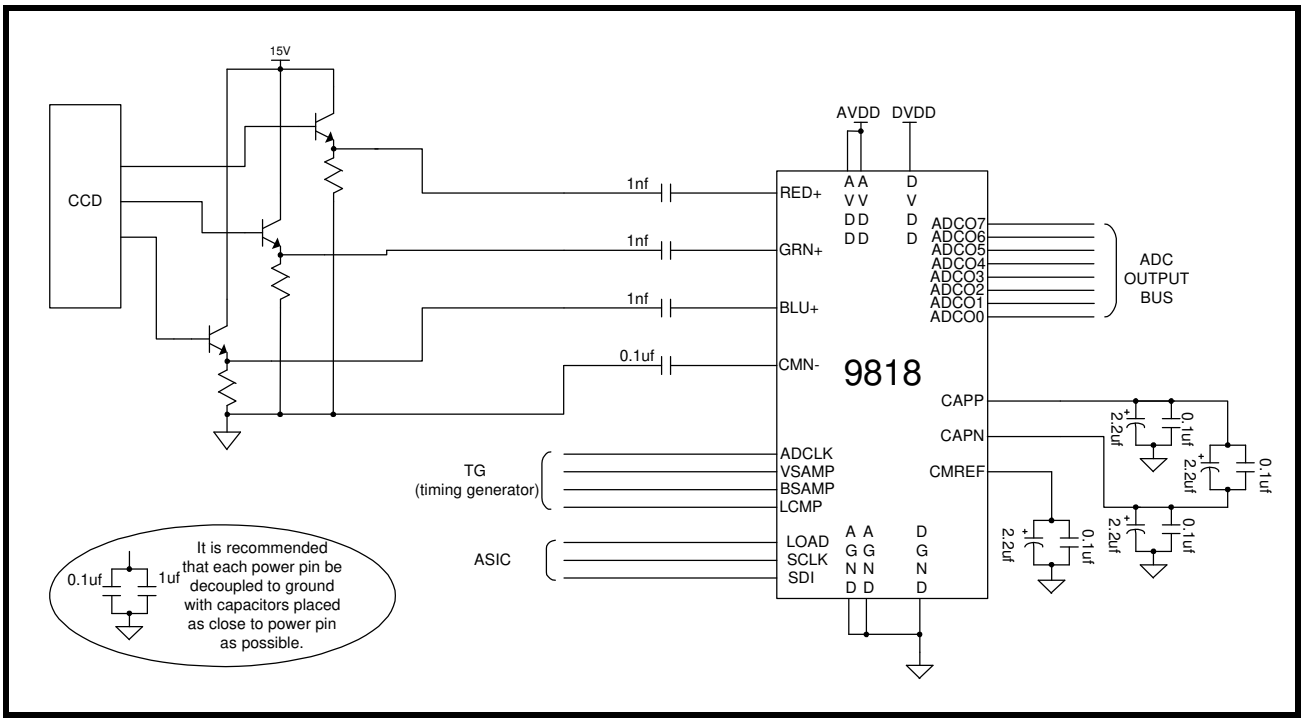


FIGURE 18. 3-CH CIS MODE SYSTEM TIMING (BYTE & NIBBLE MODES)



7.0 APPLICATION HOOK-UP DIAGRAMS

FIGURE 19. TYPICAL HOOK-UP DIAGRAM FOR THE XRD9818 (AC COUPLED, CCD EXAMPLE)



8.0 PERFORMANCE DATA

FIGURE 20. SYSTEM DNL, 3-CH OPERATION

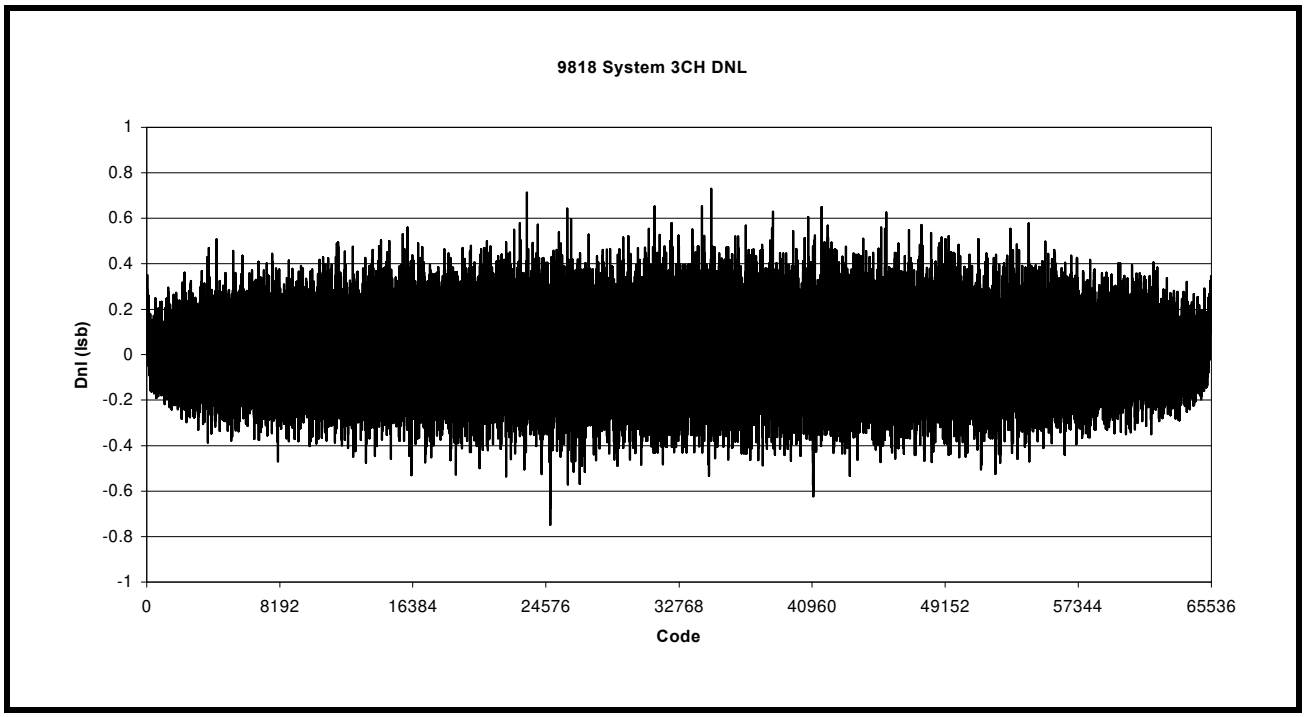


FIGURE 21. XRD9818 IDD VS TEMPERATURE

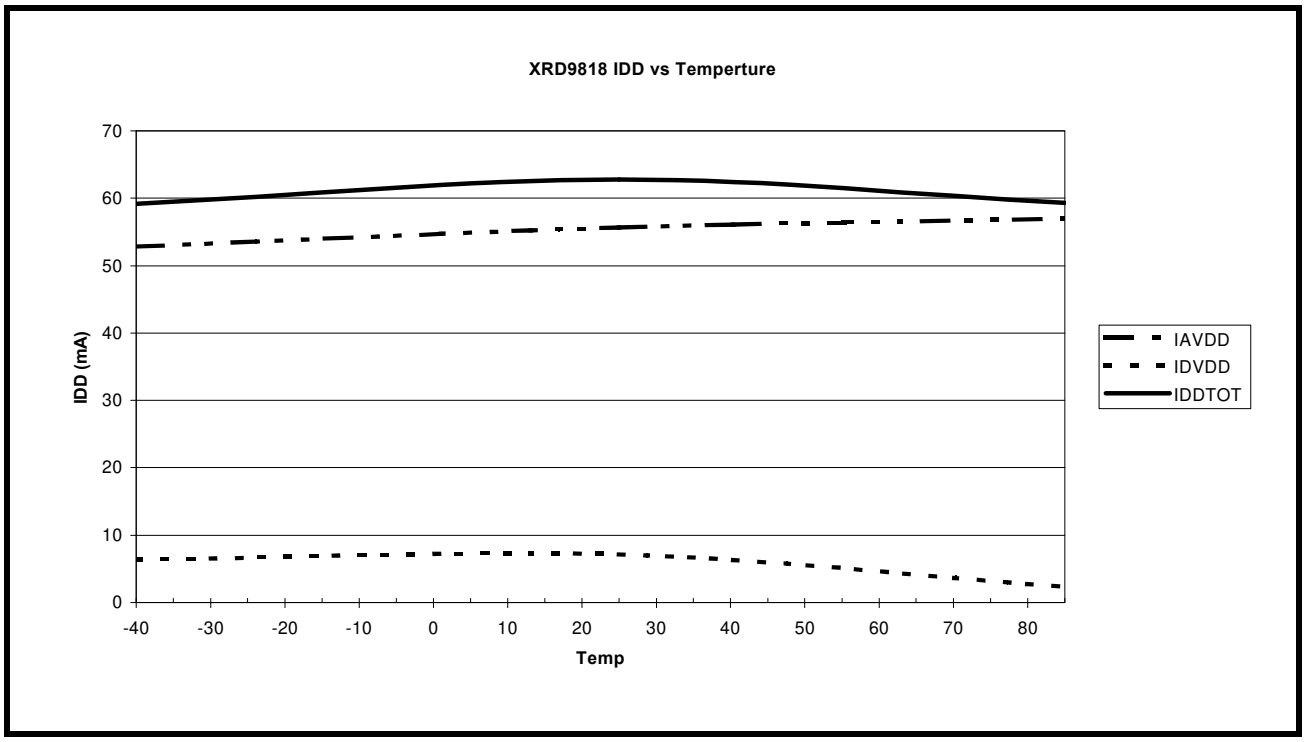
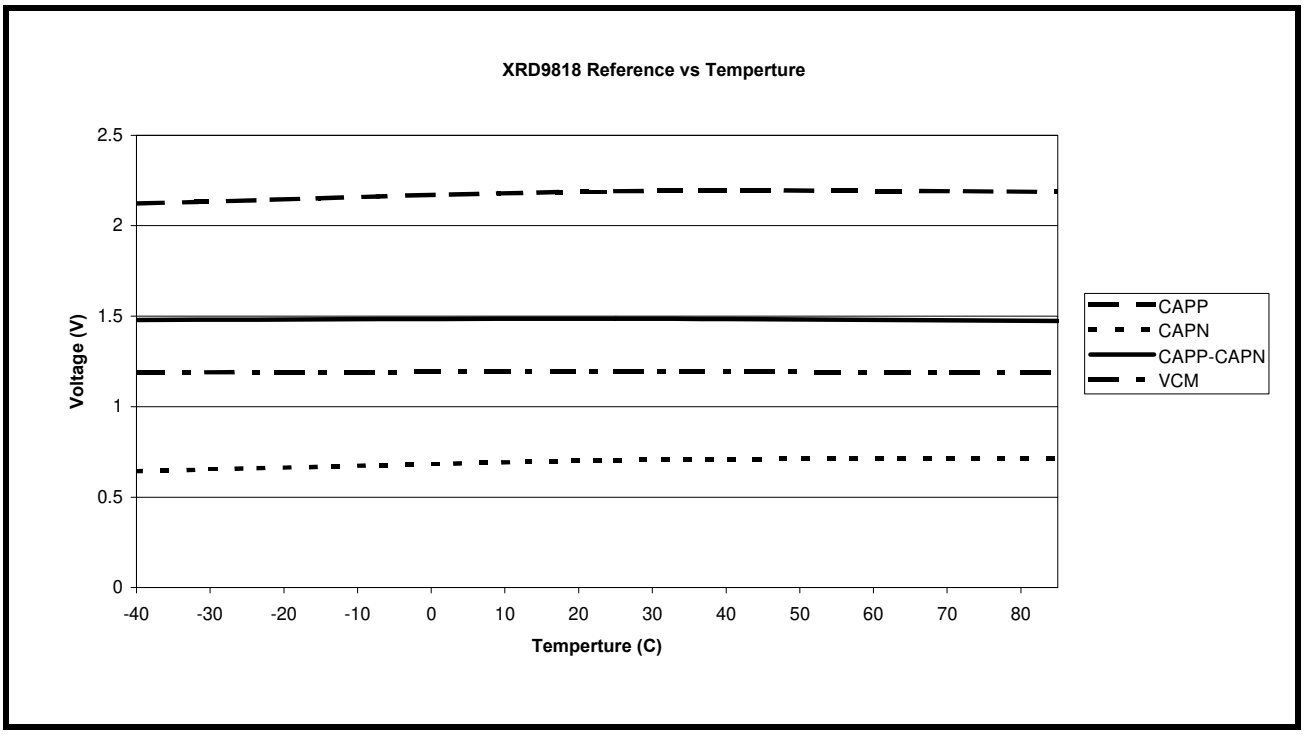
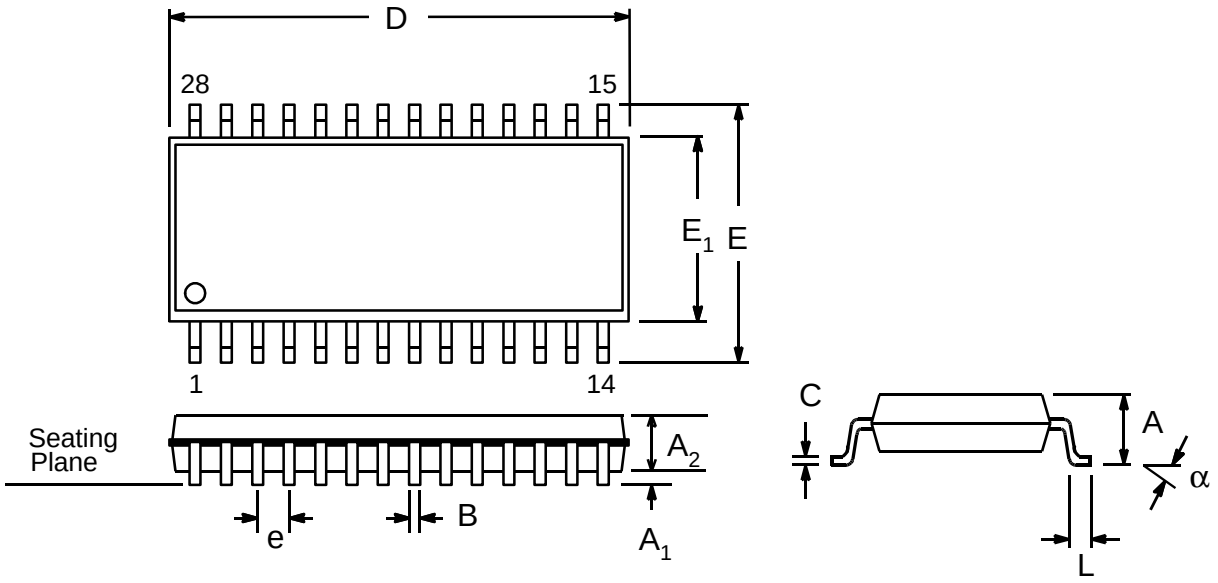


FIGURE 22. XRD9818 REFERENCE VS TEMPERATURE



PACKAGE DIMENSIONS

28 LEAD THIN SHRINK SMALL OUTLINE
(4.4mm TSSOP)
Rev. 2.00



	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.033	0.047	0.85	1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.378	0.386	9.60	9.80
E	0.248	0.260	6.30	6.60
E1	0.169	0.177	4.30	4.50
e	0.0256 BSC		0.65 BSC	
L	0.018	0.030	0.45	0.75
α	0°	8°	0°	8°

Note: The control dimension is in millimeter column

REVISION HISTORY

Revision #	Date	Description
A1.0.0	08/20/02	1st release of the XRD9818 advanced data sheet.
A1.0.1	09/26/02	Modified Serial Port Read/Write timing diagrams, system specs INL, IRN_{MIN} and IRN_{MAX}
A1.1.0	10/17/02	Changed definition of PGA to 9bit & overall system gain 1x to 5x, redefined serial port timing, added 3-CH & 1-CH timing diagrams for 8bit and 4bit data output modes,
A1.2.0	11/13/02	Added pin def, updated black diagram including VCMREF pin & removing LCLP pin, updated 8bit 1-CH timing diagram
A1.3.0	1/30/03	Updated pin def type for CMREF. Updated serial port timing diagram. Added input signal swing, reset pulse, Load pulse width and PGA spec's to elec tables. Added register map & bit definitions. Remove IB spec from CDS-S/H Specifications.
P1.0.0	11/14/03	Changed data sheet to Preliminary status. Added timing diagrams, functional descriptions and electrical table updates to reflect part performance.
1.0.0	1/29/04	Released version. Updated electrical tables & document with char data, some minor text edits to advance description, added performace data and application hook-up diagram.

Datasheet June 2004.