HA5023

Dual 125MHz Video CurrentFeedback Amplifier

FN3393
Rev 9.00
September 30, 2015

The HA5023 is a wide bandwidth high slew rate dual amplifier optimized for video applications and gains between 1 and 10. It is a current feedback amplifier and thus yields less bandwidth degradation at high closed loop gains than voltage feedback amplifiers.

The low differential gain and phase, 0.1dB gain flatness, and ability to drive two back terminated 75Ω cables, make this amplifier ideal for demanding video applications.

The current feedback design allows the user to take advantage of the amplifier's bandwidth dependency on the feedback resistor. By reducing R_F, the bandwidth can be increased to compensate for decreases at higher closed loop gains or heavy output loads.

The performance of the HA5023 is very similar to the popular Intersil HA-5020.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA5023IPZ (Note) **(No longer available, recommended replacement: HA5023IBZ)**	HA5023IPZ	-40 to 85	8 Ld PDIP* (Pb-free)	E8.3
HA5023IBZ (Note)	5023IBZ	-40 to 85	8 Ld SOIC (Pb-free)	M8.15
HA5023IBZ96 (Note)	5023IBZ	-40 to 85	8 Ld SOIC Tape and Reel (Pb-free)	M8.15

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

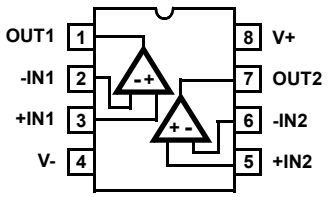
- Wide Unity Gain Bandwidth 125MHz
- Slew Rate 475V/µs
- Input Offset Voltage 800µV
- Differential Gain 0.03%
- Differential Phase . . . . . 0.03°
- Supply Current (per Amplifier) 7.5mA
- ESD Protection 4000V
- Guaranteed Specifications at ±5V Supplies
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Video Gain Block
- Video Distribution Amplifier/RGB Amplifier
- Flash A/D Driver
- Current to Voltage Converter
- Medical Imaging
- Radar and Imaging Systems
- Video Switching and Routing

Pinout

HA5023
(PDIP, SOIC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
DC Input Voltage (Note 3) . . . . . $\pm V_{SUPPLY}$
Differential Input Voltage 10V
Output Current (Note 4) . . . . . .Short Circuit Protected
ESD Rating (Note 3)
Human Body Model (Per MIL-STD-883 Method 3015.7). . . 2000V

Operating Conditions

Temperature Range . . . . . .-40°C to 85°C
Supply Voltage Range (Typical) . . . . . ±4.5V to ±15V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package*	130
SOIC Package	160

Maximum Junction Temperature (Note 1) . . . . . 175°C
Maximum Junction Temperature (Plastic Package, Note 1) . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain junction temperature below 175°C for die, and below 150°C for plastic packages. See Application Information section for safe operating area information.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. The non-inverting input of unused amplifiers must be connected to GND.
4. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 15mA for maximum reliability.

Electrical Specifications

V_{SUPPLY} = ±5V, R_F = 1kΩ, A_V = +1, R_L = 400Ω, C_L ≤ 10pF, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 9) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage (V_{IO})		A	25	-	0.8	3	mV
		A	Full	-	-	5	mV
Delta V_{IO} Between Channels		A	Full	-	1.2	3.5	mV
Average Input Offset Voltage Drift		B	Full	-	5	-	µV/°C
V_{IO} Common Mode Rejection Ratio	Note 5	A	25	53	-	-	dB
		A	Full	50	-	-	dB
V_{IO} Power Supply Rejection Ratio	±3.5V ≤ V_S ≤ ±6.5V	A	25	60	-	-	dB
		A	Full	55	-	-	dB
Input Common Mode Range	Note 5	A	Full	±2.5	-	-	V
Non-Inverting Input (+IN) Current		A	25	-	3	8	µA
		A	Full	-	-	20	µA
+IN Common Mode Rejection ($+I_{BCMR} = \frac{1}{+R_{IN}}$)	Note 5	A	25	-	-	0.15	µA/V
		A	Full	-	-	0.5	µA/V
+IN Power Supply Rejection	±3.5V ≤ V_S ≤ ±6.5V	A	25	-	-	0.1	µA/V
		A	Full	-	-	0.3	µA/V
Inverting Input (-IN) Current		A	25, 85	-	4	12	µA
		A	-40	-	10	30	µA
Delta -IN BIAS Current Between Channels		A	25, 85	-	6	15	µA
		A	-40	-	10	30	µA

Electrical Specifications V_{SUPPLY} = ±5V, R_F = 1kΩ, A_V = +1, R_L = 400Ω, C_L ≤ 10pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 9) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
-IN Common Mode Rejection	Note 5	A	25	-	-	0.4	µA/V
		A	Full	-	-	1.0	µA/V
-IN Power Supply Rejection	±3.5V ≤ V_S ≤ ±6.5V	A	25	-	-	0.2	µA/V
		A	Full	-	-	0.5	µA/V
Input Noise Voltage	f = 1kHz	B	25	-	4.5	-	nV/√Hz
+Input Noise Current	f = 1kHz	B	25	-	2.5	-	pA/√Hz
-Input Noise Current	f = 1kHz	B	25	-	25.0	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Transimpedence	Note 11	A	25	1.0	-	-	MΩ
		A	Full	0.85	-	-	MΩ
Open Loop DC Voltage Gain	R_L = 400Ω, V_{OUT} = ±2.5V	A	25	70	-	-	dB
		A	Full	65	-	-	dB
Open Loop DC Voltage Gain	R_L = 100Ω, V_{OUT} = ±2.5V	A	25	50	-	-	dB
		A	Full	45	-	-	dB
OUTPUT CHARACTERISTICS							
Output Voltage Swing	R_L = 150Ω	A	25	±2.5	±3.0	-	V
		A	Full	±2.5	±3.0	-	V
Output Current	R_L = 150Ω	B	Full	±16.6	±20.0	-	mA
Output Current, Short Circuit	V_{IN} = ±2.5V, V_{OUT} = 0V	A	Full	±40	±60	-	mA
POWER SUPPLY CHARACTERISTICS							
Supply Voltage Range		A	25	5	-	15	V
Quiescent Supply Current		A	Full	-	7.5	10	mA/Op Amp
AC CHARACTERISTICS (A_V = +1)							
Slew Rate	Note 6	B	25	275	350	-	V/µs
Full Power Bandwidth	Note 7	B	25	22	28	-	MHz
Rise Time	Note 8	B	25	-	6	-	ns
Fall Time	Note 8	B	25	-	6	-	ns
Propagation Delay	Note 8	B	25	-	6	-	ns
Overshoot		B	25	-	4.5	-	%
-3dB Bandwidth	V_{OUT} = 100mV	B	25	-	125	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	B	25	-	75	-	ns

Electrical Specifications V_{SUPPLY} = ±5V, R_F = 1kΩ, A_V = +1, R_L = 400Ω, C_L ≤ 10pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 9) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
AC CHARACTERISTICS (A_V = +2, R_F = 681Ω)							
Slew Rate	Note 6	B	25	-	475	-	V/µs
Full Power Bandwidth	Note 7	B	25	-	26	-	MHz
Rise Time	Note 8	B	25	-	6	-	ns
Fall Time	Note 8	B	25	-	6	-	ns
Propagation Delay	Note 8	B	25	-	6	-	ns
Overshoot		B	25	-	12	-	%
-3dB Bandwidth	V_{OUT} = 100mV	B	25	-	95	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	B	25	-	100	-	ns
Gain Flatness	5MHz	B	25	-	0.02	-	dB
	20MHz	B	25	-	0.07	-	dB
AC CHARACTERISTICS (A_V = +10, R_F = 383Ω)							
Slew Rate	Note 6	B	25	350	475	-	V/µs
Full Power Bandwidth	Note 7	B	25	28	38	-	MHz
Rise Time	Note 8	B	25	-	8	-	ns
Fall Time	Note 8	B	25	-	9	-	ns
Propagation Delay	Note 8	B	25	-	9	-	ns
Overshoot		B	25	-	1.8	-	%
-3dB Bandwidth	V_{OUT} = 100mV	B	25	-	65	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	75	-	ns
Settling Time to 0.1%	2V Output Step	B	25	-	130	-	ns
VIDEO CHARACTERISTICS							
Differential Gain (Note 10)	R_L = 150Ω	B	25	-	0.03	-	%
Differential Phase (Note 10)	R_L = 150Ω	B	25	-	0.03	-	°

NOTES:

5. V_{CM} = ±2.5V. At -40°C Product is tested at V_{CM} = ±2.25V because Short Test Duration does not allow self heating.
6. V_{OUT} switches from -2V to +2V, or from +2V to -2V. Specification is from the 25% to 75% points.
7. $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; V_{PEAK} = 2V .
8. R_L = 100Ω, V_{OUT} = 1V. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
9. A. Production Tested; B. Typical or Guaranteed Limit based on characterization; C. Design Typical for information only.
10. Measured with a VM700A video tester using an NTC-7 composite VITS.
11. V_{OUT} = ±2.5V. At -40°C Product is tested at V_{OUT} = ±2.25V because Short Test Duration does not allow self heating.

Test Circuits and Waveforms

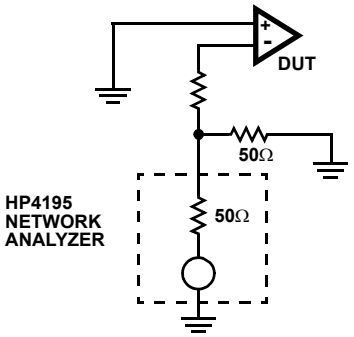


FIGURE 1. TEST CIRCUIT FOR TRANSIMPEDANCE MEASUREMENTS

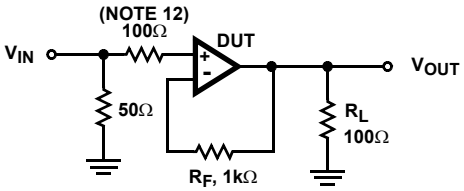


FIGURE 2. SMALL SIGNAL PULSE RESPONSE CIRCUIT

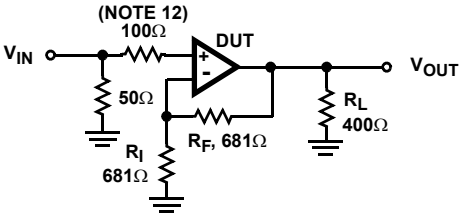
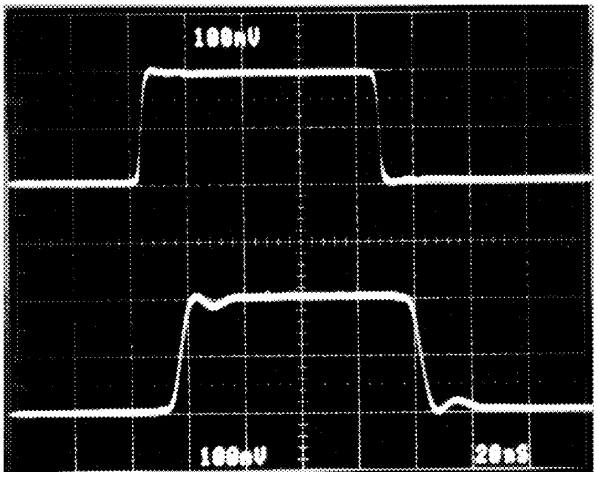


FIGURE 3. LARGE SIGNAL PULSE RESPONSE CIRCUIT

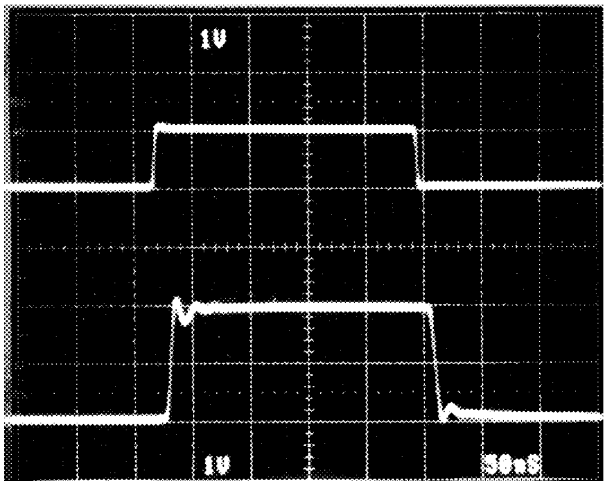
NOTE:

12. A series input resistor of ≥100Ω is recommended to limit input currents in case input signals are present before the HA5023 is powered up.



Vertical Scale: V_{IN} = 100mV/Div., V_{OUT} = 100mV/Div.
Horizontal Scale: 20ns/Div.

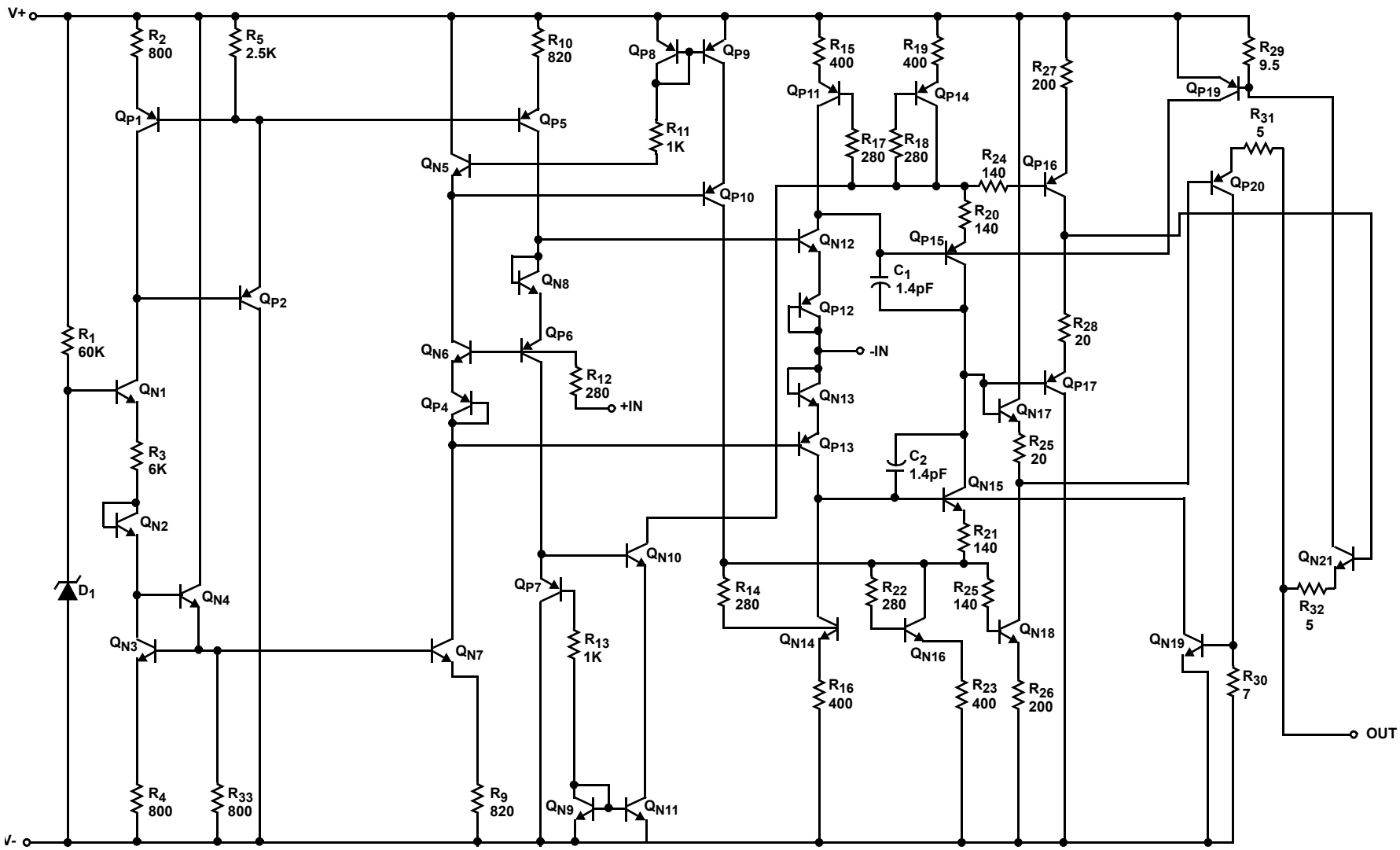
FIGURE 4. SMALL SIGNAL RESPONSE



Vertical Scale: V_{IN} = 1V/Div., V_{OUT} = 1V/Div.
Horizontal Scale: 50ns/Div.

FIGURE 5. LARGE SIGNAL RESPONSE

Schematic Diagram (One Amplifier of Two)



Application Information

Optimum Feedback Resistor

The plots of inverting and non-inverting frequency response, see Figure 8 and Figure 9 in the typical performance section, illustrate the performance of the HA5023 in various closed loop gain configurations. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HA5023 design is optimized for a 1000Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	750	100
+1	1000	125
+2	681	95
+5	1000	52
+10	383	65
-10	750	22

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. The use of low inductance components such as chip resistors and chip capacitors is strongly recommended. If leaded components are used the leads must be kept short especially for the power supply decoupling components and those components connected to the inverting input.

Attention must be given to decoupling the power supplies. A large value (10μF) tantalum or electrolytic capacitor in parallel with a small value (0.1μF) chip capacitor works well in most cases.

A ground plane is strongly recommended to control noise. Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. It is recommended that the ground plane be removed under traces connected to -IN, and that connections to -IN be kept as short as possible to minimize the capacitance from this node to ground.

Driving Capacitive Loads

Capacitive loads will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases the oscillation can be avoided by placing an isolation resistor (R) in series with the output as shown in Figure 6.

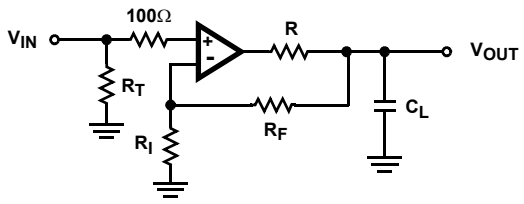


FIGURE 6. PLACEMENT OF THE OUTPUT ISOLATION RESISTOR, R

The selection criteria for the isolation resistor is highly dependent on the load, but 27Ω has been determined to be a good starting value.

Power Dissipation Considerations

Due to the high supply current inherent in dual amplifiers, care must be taken to insure that the maximum junction temperature (T_J, see Absolute Maximum Ratings) is not exceeded. Figure 7 shows the maximum ambient temperature versus supply voltage for the available package styles (Plastic DIP, SOIC). At $\pm 5V_{DC}$ quiescent operation both package styles may be operated over the full industrial range of -40°C to 85°C. It is recommended that thermal calculations, which take into account output power, be performed by the designer.

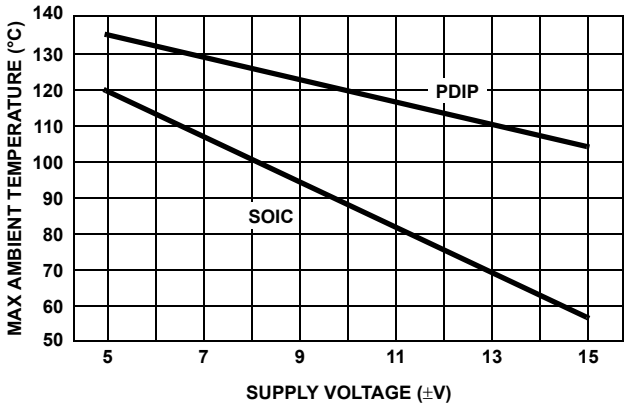


FIGURE 7. MAXIMUM OPERATING AMBIENT TEMPERATURE vs SUPPLY VOLTAGE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25°C$, Unless Otherwise Specified

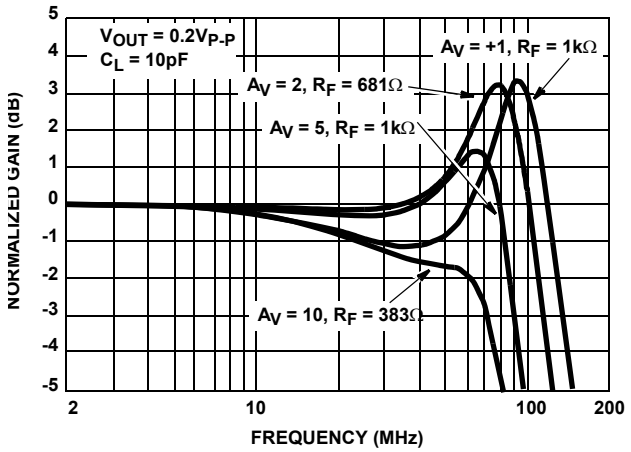


FIGURE 8. NON-INVERTING FREQENCY RESPONSE

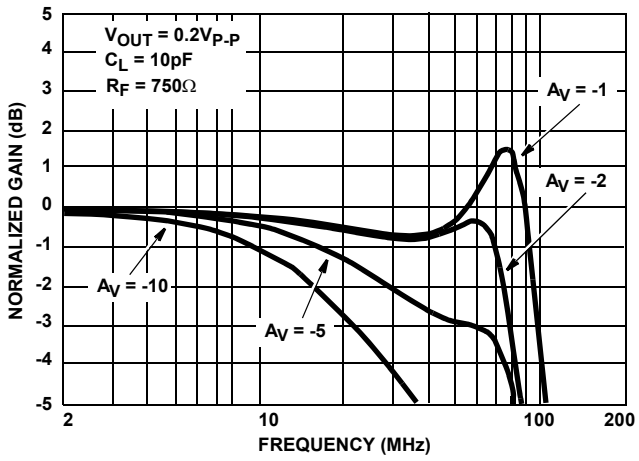


FIGURE 9. INVERTING FREQUENCY RESPONSE

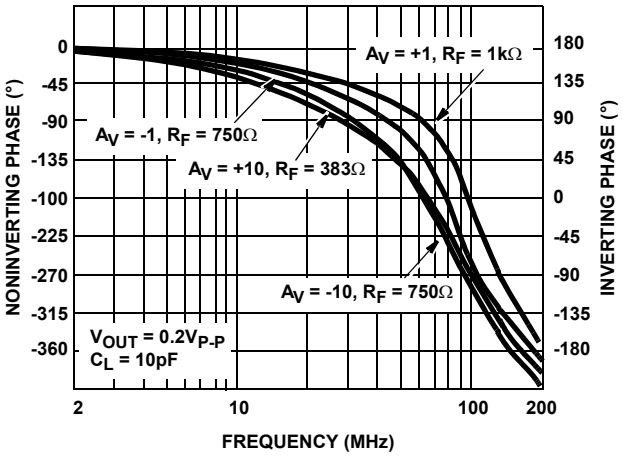


FIGURE 10. PHASE RESPONSE AS A FUNCTION OF FREQUENCY

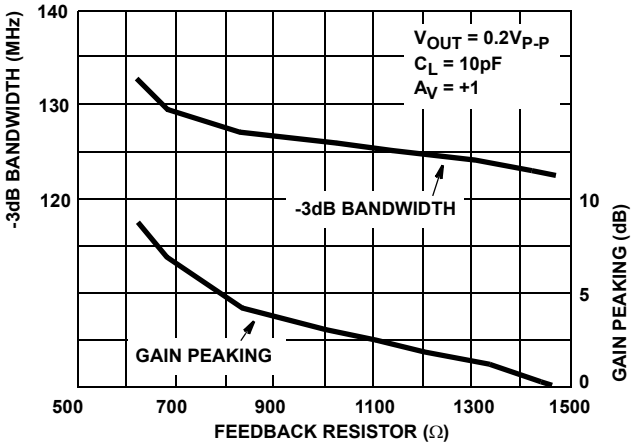


FIGURE 11. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

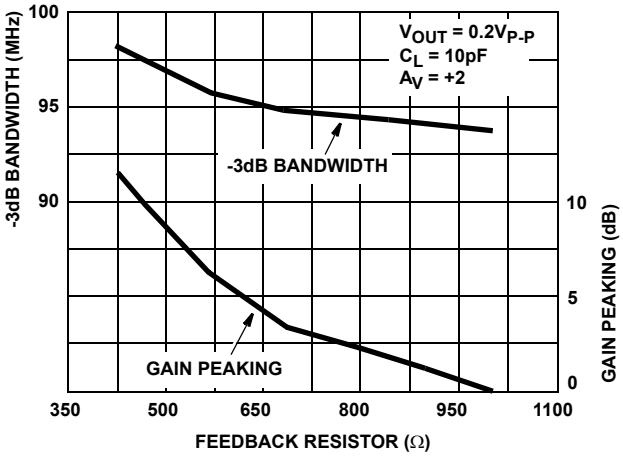


FIGURE 12. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

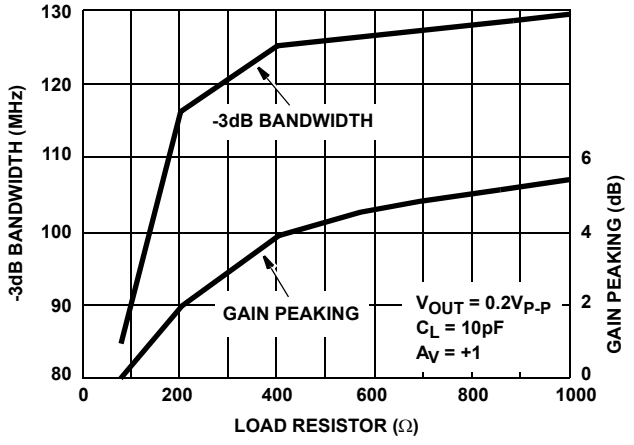


FIGURE 13. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25°C$, Unless Otherwise Specified **(Continued)**

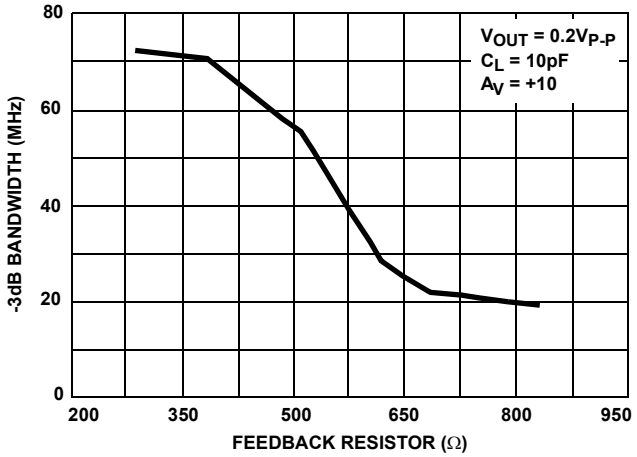


FIGURE 14. BANDWIDTH vs FEEDBACK RESISTANCE

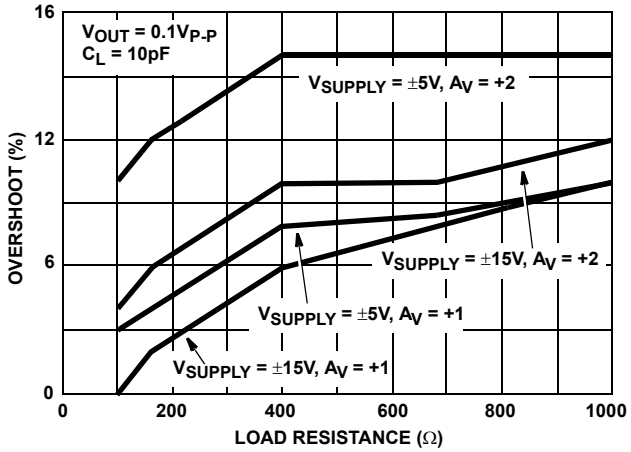


FIGURE 15. SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE

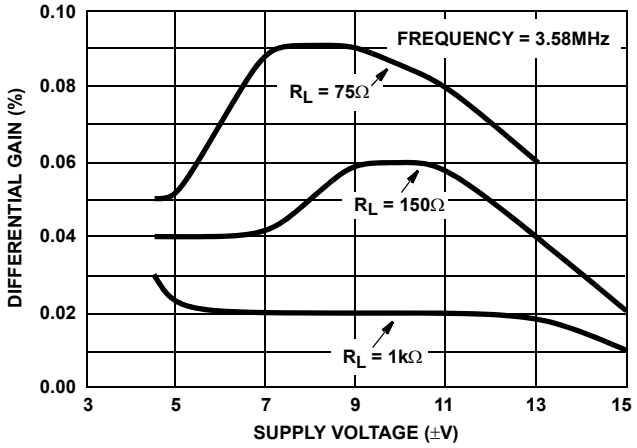


FIGURE 16. DIFFERENTIAL GAIN vs SUPPLY VOLTAGE

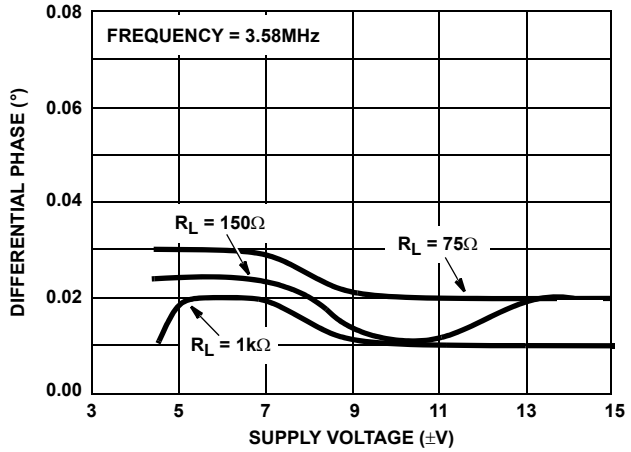


FIGURE 17. DIFFERENTIAL PHASE vs SUPPLY VOLTAGE

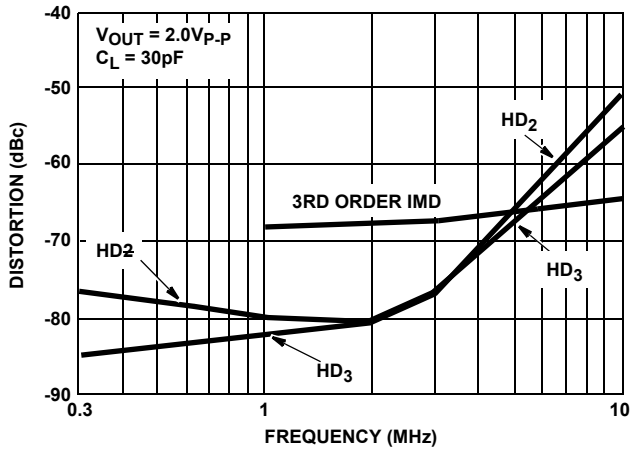


FIGURE 18. DISTORTION vs FREQUENCY

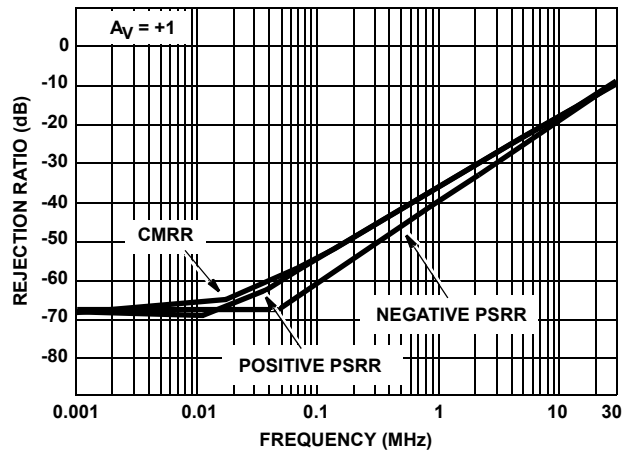


FIGURE 19. REJECTION RATIOS vs FREQUENCY

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25°C$, Unless Otherwise Specified **(Continued)**

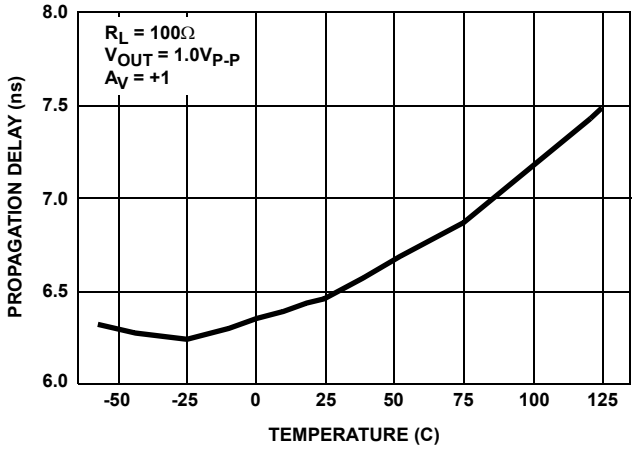


FIGURE 20. PROPAGATION DELAY vs TEMPERATURE

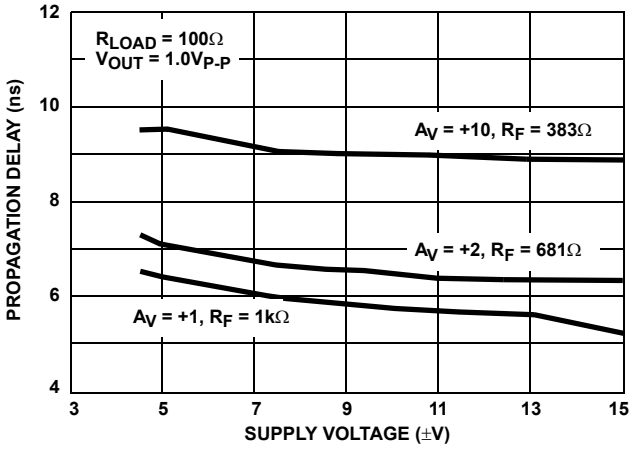


FIGURE 21. PROPAGATION DELAY vs SUPPLY VOLTAGE

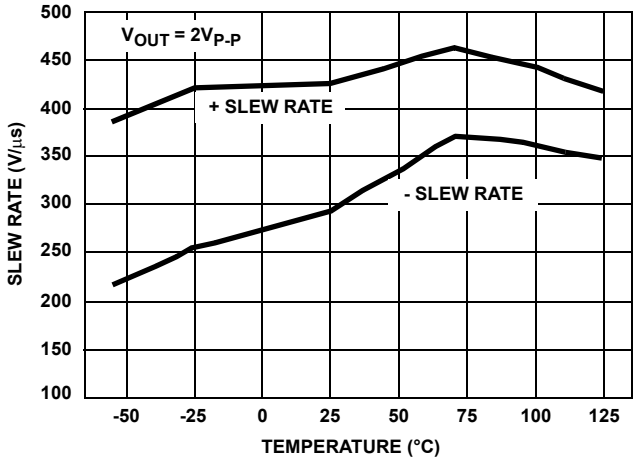


FIGURE 22. FIGURE 22. SLEW RATE vs TEMPERATURE

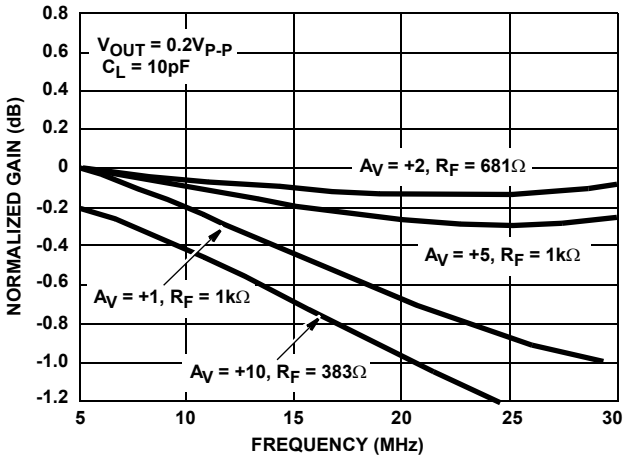


FIGURE 23. NON-INVERTING GAIN FLATNESS vs FREQUENCY

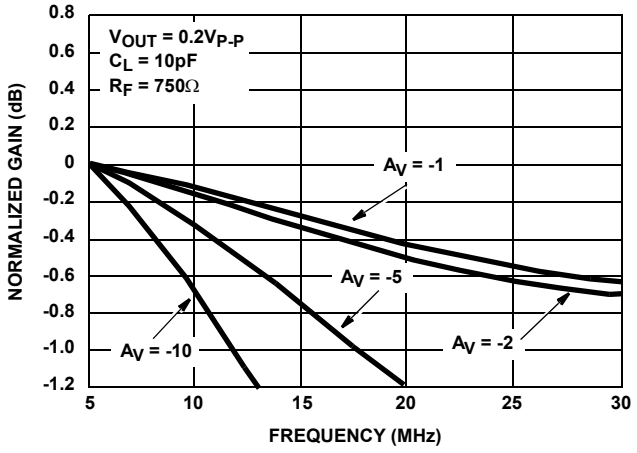


FIGURE 24. INVERTING GAIN FLATNESS vs FREQUENCY

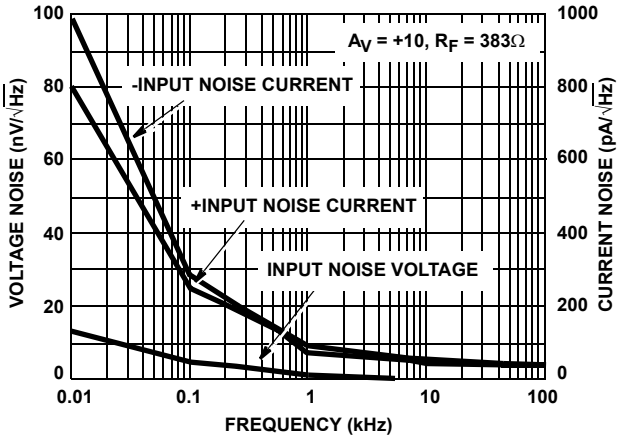


FIGURE 25. INPUT NOISE CHARACTERISTICS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25°C$, Unless Otherwise Specified **(Continued)**

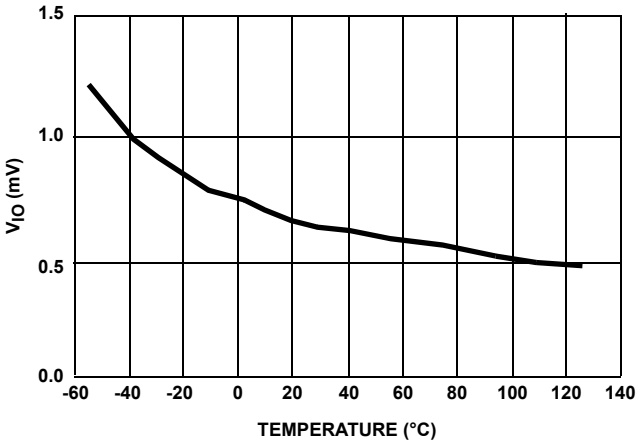


FIGURE 26. INPUT OFFSET VOLTAGE vs TEMPERATURE

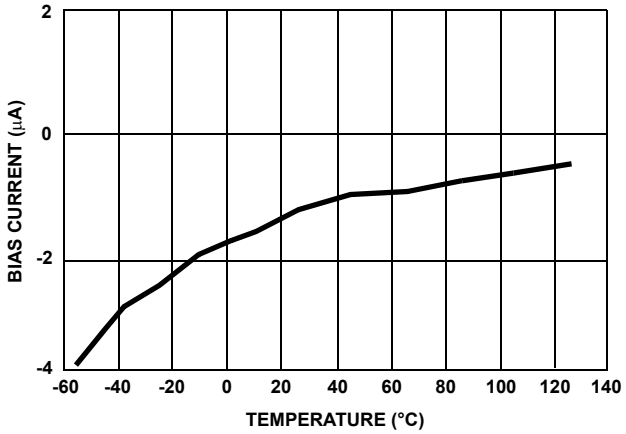


FIGURE 27. +INPUT BIAS CURRENT vs TEMPERATURE

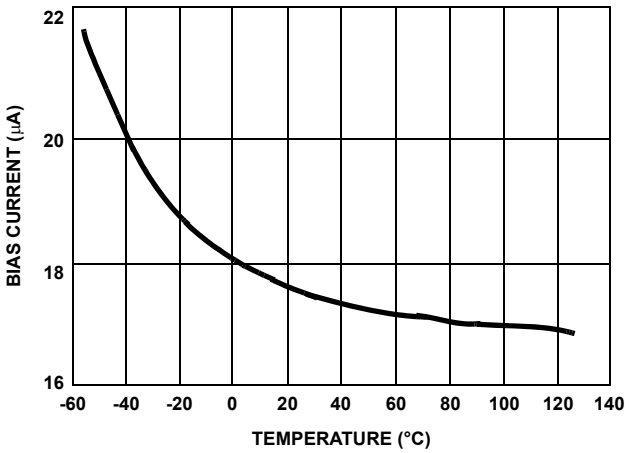


FIGURE 28. -INPUT BIAS CURRENT vs TEMPERATURE

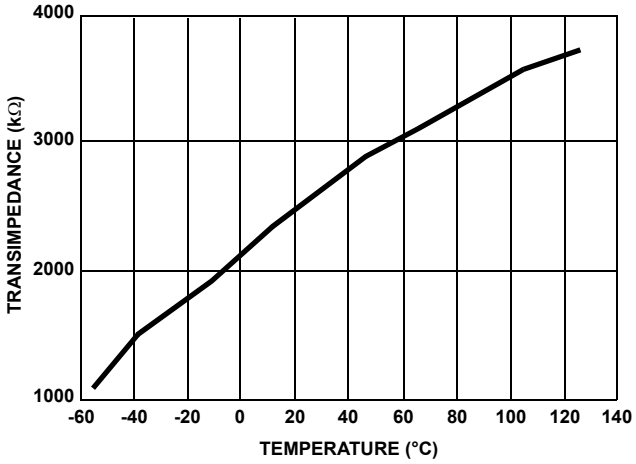


FIGURE 29. TRANSIMPEDANCE vs TEMPERATURE

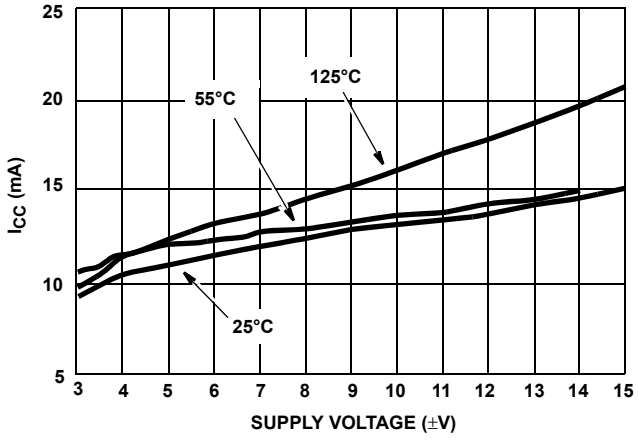


FIGURE 30. SUPPLY CURRENT vs SUPPLY VOLTAGE

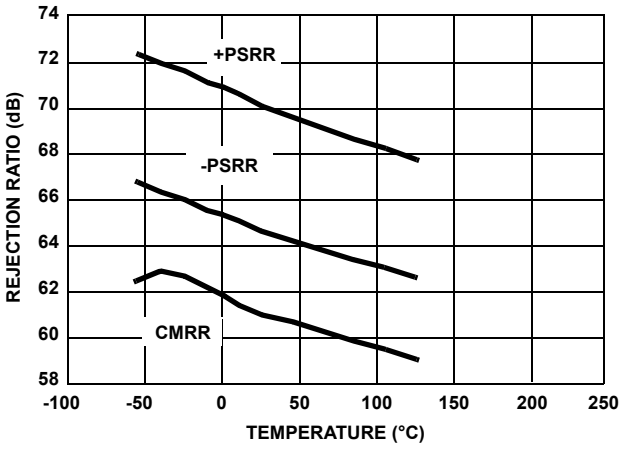


FIGURE 31. REJECTION RATIO vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25°C$, Unless Otherwise Specified **(Continued)**

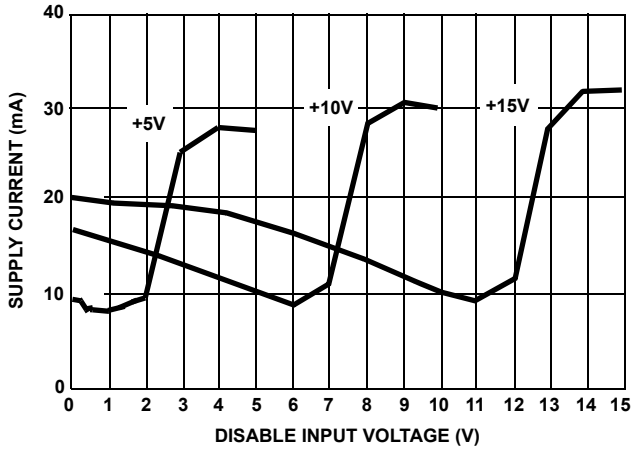


FIGURE 32. SUPPLY CURRENT vs DISABLE INPUT VOLTAGE

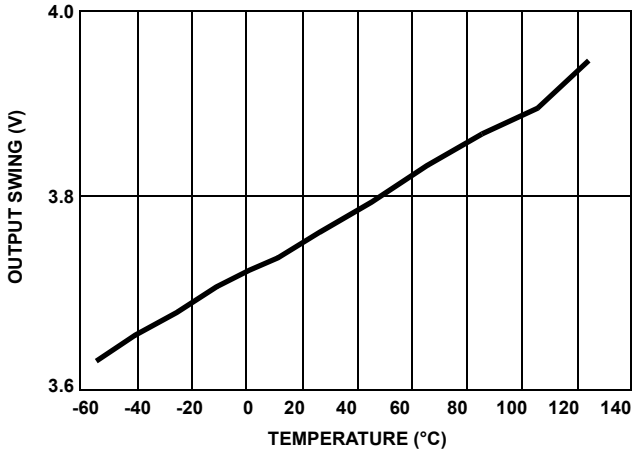


FIGURE 33. OUTPUT SWING vs TEMPERATURE

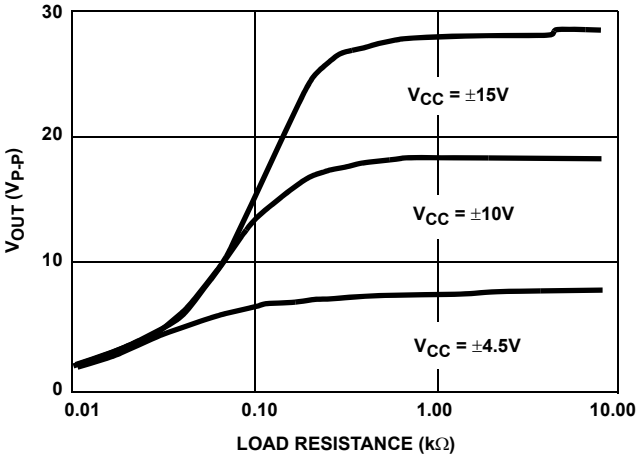


FIGURE 34. OUTPUT SWING vs LOAD RESISTANCE

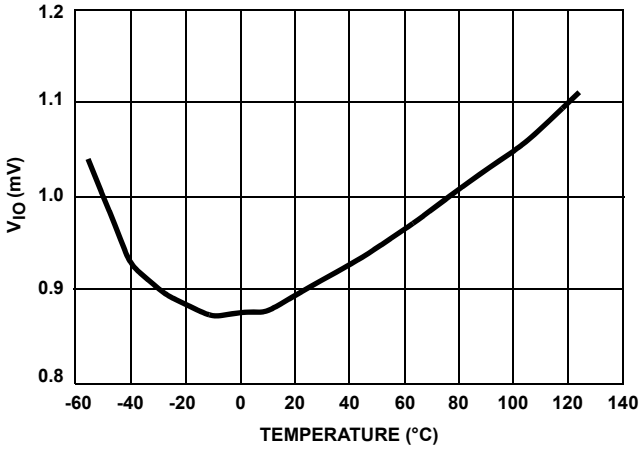


FIGURE 35. INPUT OFFSET VOLTAGE CHANGE BETWEEN CHANNELS vs TEMPERATURE

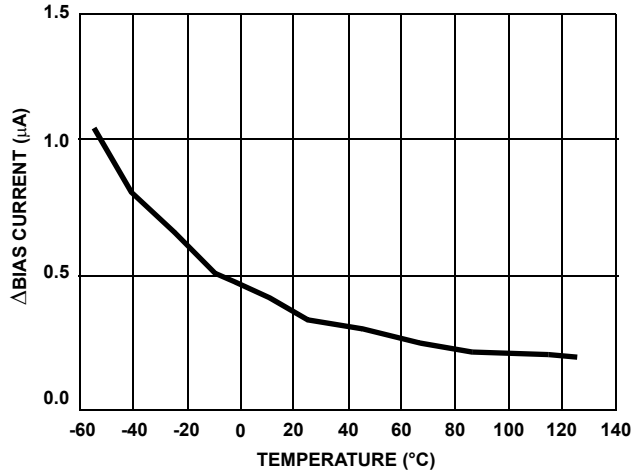


FIGURE 36. INPUT BIAS CURRENT CHANGE BETWEEN CHANNELS vs TEMPERATURE

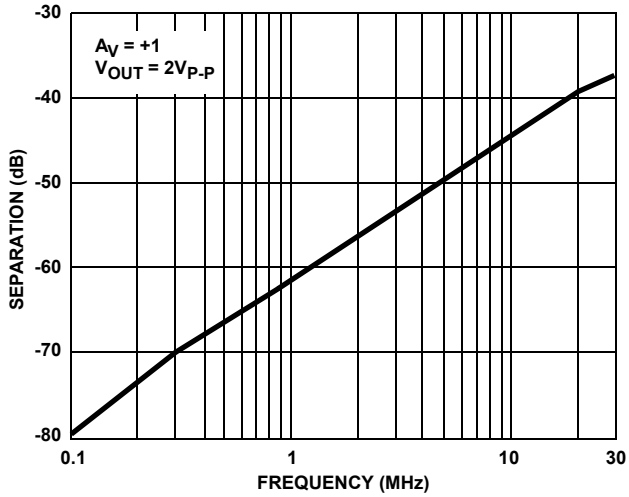


FIGURE 37. CHANNEL SEPARATION vs FREQUENCY

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25°C$, Unless Otherwise Specified **(Continued)**

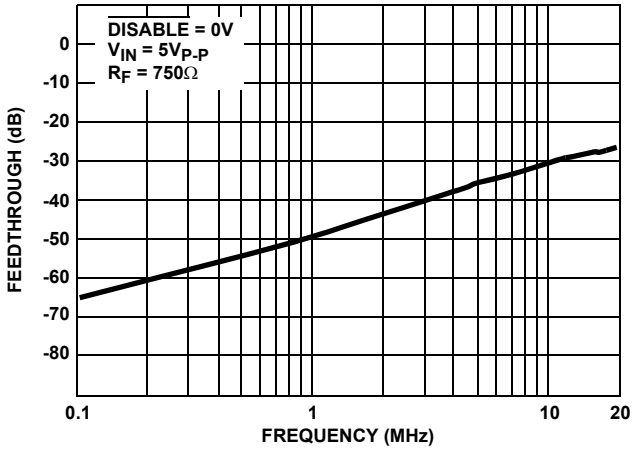


FIGURE 38. DISABLE FEEDTHROUGH vs FREQUENCY

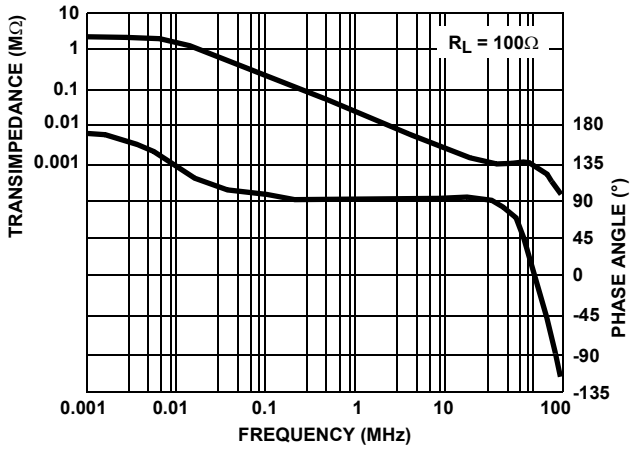


FIGURE 39. TRANSIMPEDANCE vs FREQUENCY

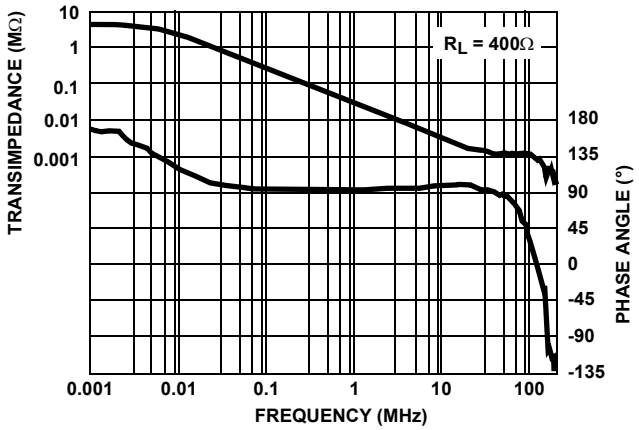


FIGURE 40. TRANSIMPEDENCE vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

1650µm x 2540µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu (1%)
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu (1%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.4kÅ

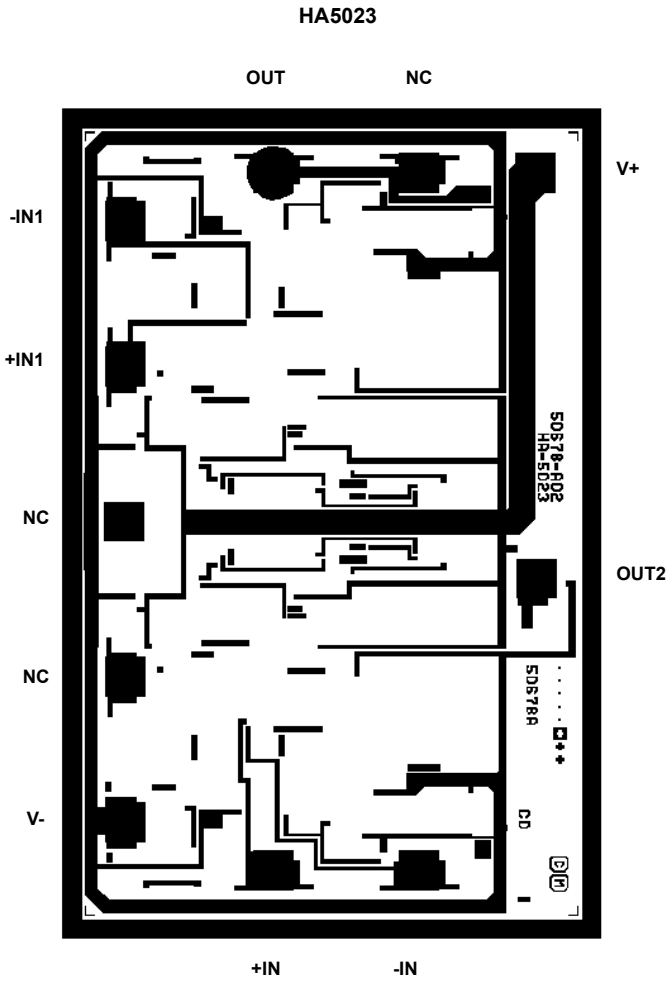
TRANSISTOR COUNT:

124

PROCESS:

High Frequency Bipolar Dielectric Isolation

Metallization Mask Layout



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
September 30, 2015	FN3393.9	- Updated Ordering Information Table on page 1. - Added Revision History. - Added About Intersil Verbiage. - Updated POD M8.15 to latest revision changes are as follow: -Revision 1 to Revision 2 Changes: Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern -Revision 2 to Revision 3 Changes: Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) -Revision 3 to Revision 4 Changes: Changed Note 1 "1982" to "1994"

About Intersil

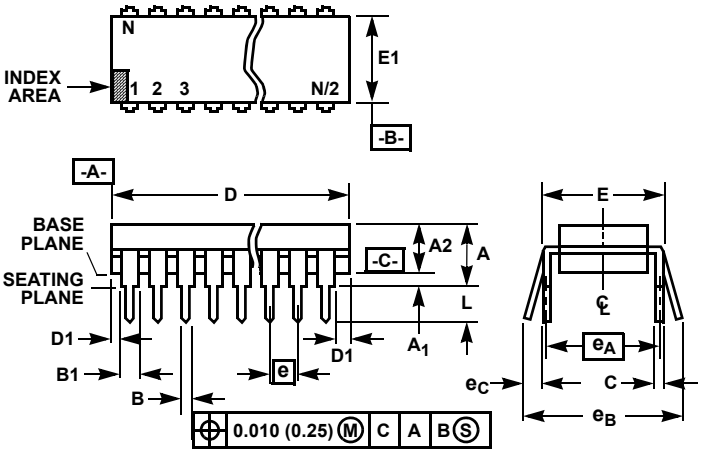
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

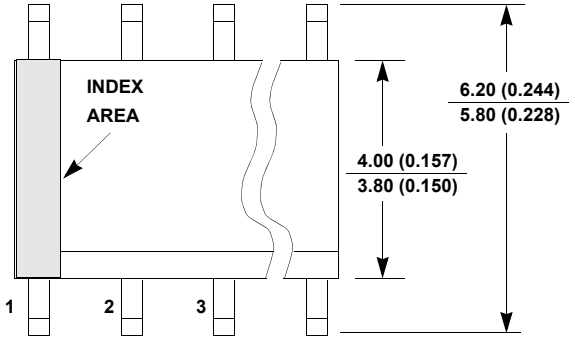
Rev. 0 12/93

Package Outline Drawing

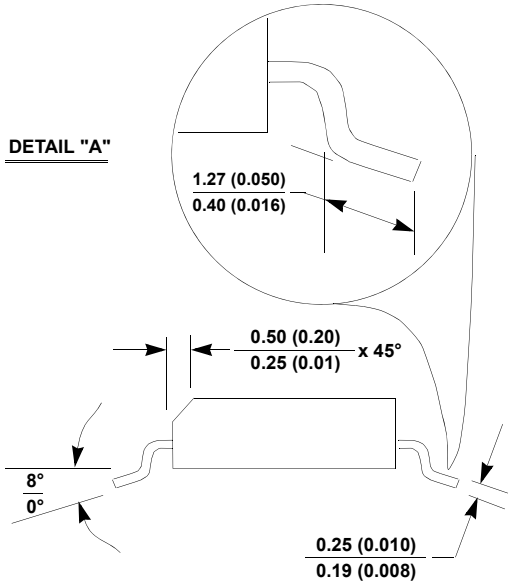
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

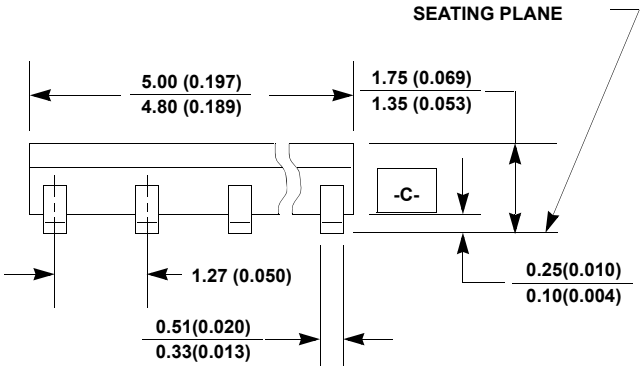
Rev 4, 1/12



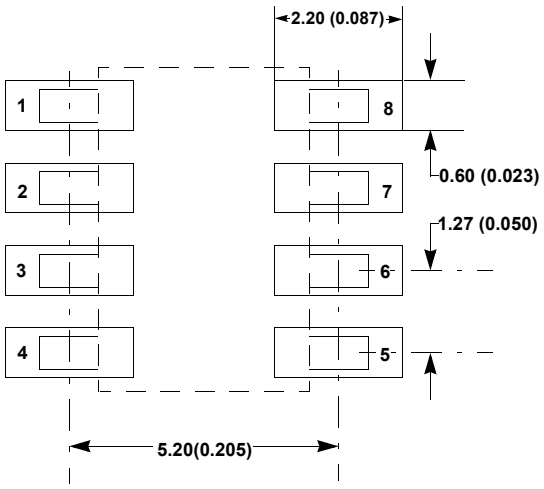
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.