HCPL-2602, HCPL-2612

High CMR Line Receiver Optocouplers

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

The HCPL-2602/12 are optically coupled line receivers that combine a GaAsP light emitting diode, an input current regulator and an integrated high gain photo detector. The input regulator serves as a line termination for line receiver applications. It clamps the line voltage and regulates the LED current so line reflections do not interfere with circuit performance.

The regulator allows a typical LED current of 8.5 mA before it starts to shunt excess current. The output of the detector IC is an open collector Schottky clamped transistor. An enable input gates the detector. The internal detector shield provides a guaranteed common mode transient immunity specification of 1000 V/ms for the 2602, and 3500 V/ms for the 2612.

DC specifications are defined similar to TTL logic. The optocoupler ac and dc operational parameters are guaranteed from 0°C to 70°C allowing trouble-free interfacing with digital logic circuits. An input current of 5 mA will sink an eight gate fan-out (TTL) at the output.

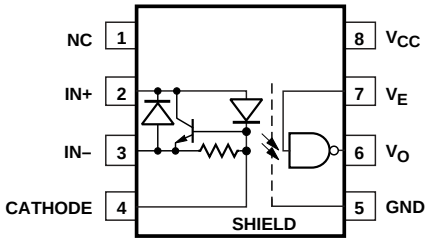
Features

- 1000 V/∝s minimum Common Mode Rejection (CMR) at V_{CM} = 50 V for HCPL-2602 and 3.5 kV/∝s minimum CMR at V_{CM} = 300 V for HCPL-2612
- Line termination included – no extra circuitry required
- Accepts a broad range of drive conditions
- LED protection minimizes LED efficiency degradation
- High speed: 10 MBd (limited by transmission line in many applications)
- Guaranteed AC and DC performance over temperature: 0°C to 70°C
- External base lead allows "LED peaking" and LED current adjustment
- Safety approval
  UL recognized – 3750 V rms for 1 Minute
  CSA approved
- MIL-PRF-38534 hermetic version available (HCPL-1930/1)

Applications

- Isolated line receiver
- Computer-peripheral interface
- Microprocessor system interface
- Digital isolation for A/D, D/A conversion
- Current sensing
- Instrument input/output isolation
- Ground loop elimination
- Pulse transformer replacement
- Power transistor isolation in motor drives

Functional Diagram



TRUTH TABLE
(POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H
ON	NC	L
OFF	NC	H

A 0.1∝F bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

The HCPL-2602/12 are useful as line receivers in high noise environments that conventional line receivers cannot tolerate. The higher LED threshold voltage provides improved immunity to differential noise and the internally shielded detector provides orders of magnitude improvement in common mode rejection with little or no sacrifice in speed.

Selection Guide

Minimum CMR		Input		8-Pin DIP (300 Mil)		Small-Outline SO-8(400 Mil)		Widebody Hermetic	Hermetic
dV/ dt (V/ ∝s)	V_{CM} (V)	On-Current (mA)	Output Enable	Single Channel Package	Dual Channel Package	Single Channel Package	Dual Channel Package	Single Channel Package	Single and Dual Channel Packages
NA	NA	5	YES	6N137		HCPL-0600		HCNW137	
			NO		HCPL-2630		HCPL-0630		
5,000	50		YES	HCPL-2601		HCPL-0601		HCNW2601	
			NO		HCPL-2631		HCPL-0631		
10,000	1,000		YES	HCPL-2611		HCPL-0611		HCNW2611	
			NO		HCPL-4661		HCPL-0661		
1,000	50		YES	HCPL-2602[1]					
3,500	300		YES	HCPL-2612[1]					
1,000	50	3	YES	HCPL-261A		HCPL-061A			
			NO		HCPL-263A		HCPL-063A		
1,000[2]	1,000		YES	HCPL-261N		HCPL-061N			
			NO		HCPL-263N		HCPL-063N		
1,000	50	12.5	[3]						HCPL-193X HCPL-56XX HCPL-66XX

Notes:

1. HCPL-2602/ 2612 devices include input current regulator.
2. 15 kV/ ∝s with V_{CM} = 1 kV can be achieved using Avago application circuit.
3. Enable is available for single channel products only, except for HCPL-193X devices.

Ordering Information

HCPL-2602/HCPL-2612 is UL Recognized with 3750 Vrms for 1 minute per UL1577.

Part Number	Option		Package	Surface Mount	Gull Wing	Tape & Reel	Quantity
	RoHS Compliant	non RoHS Compliant					
HCPL-2602	-000E	no option	300 mil DIP-8				50 per tube
HCPL-2612	-300E	#300		X	X		50 per tube
	-500E	#500		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

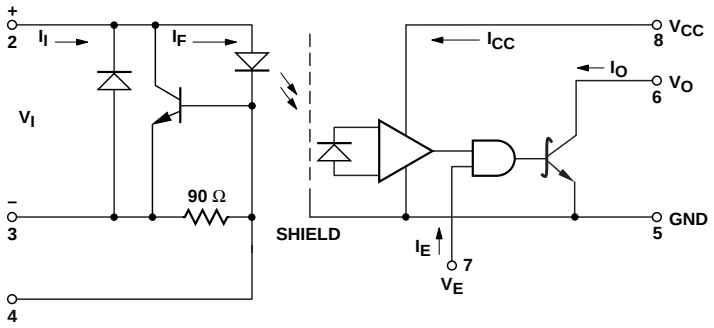
Example 1:
HCPL-2602-500E to order product of Gull Wing Surface Mount package in Tape and Reel packaging and RoHS compliant.

Example 2:
HCPL-2612 to order product of 300 mil DIP package in Tube packaging and non RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since July 15, 2001 and RoHS compliant will use '–XXXE.'

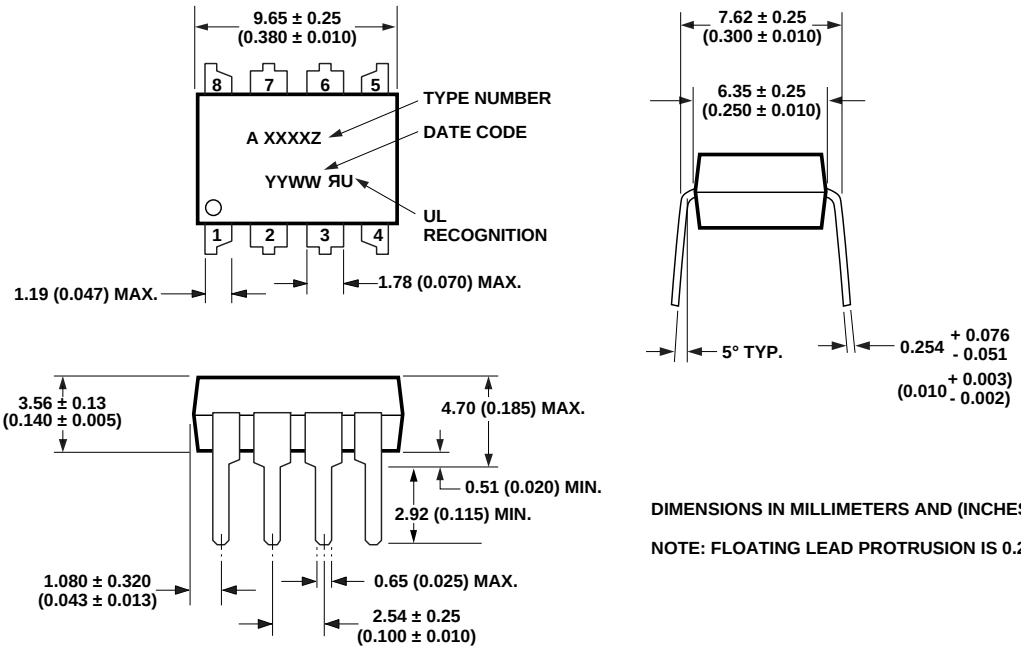
Schematic



USE OF A 0.1 µF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS REQUIRED (SEE NOTE 1).

Package Outline Drawings

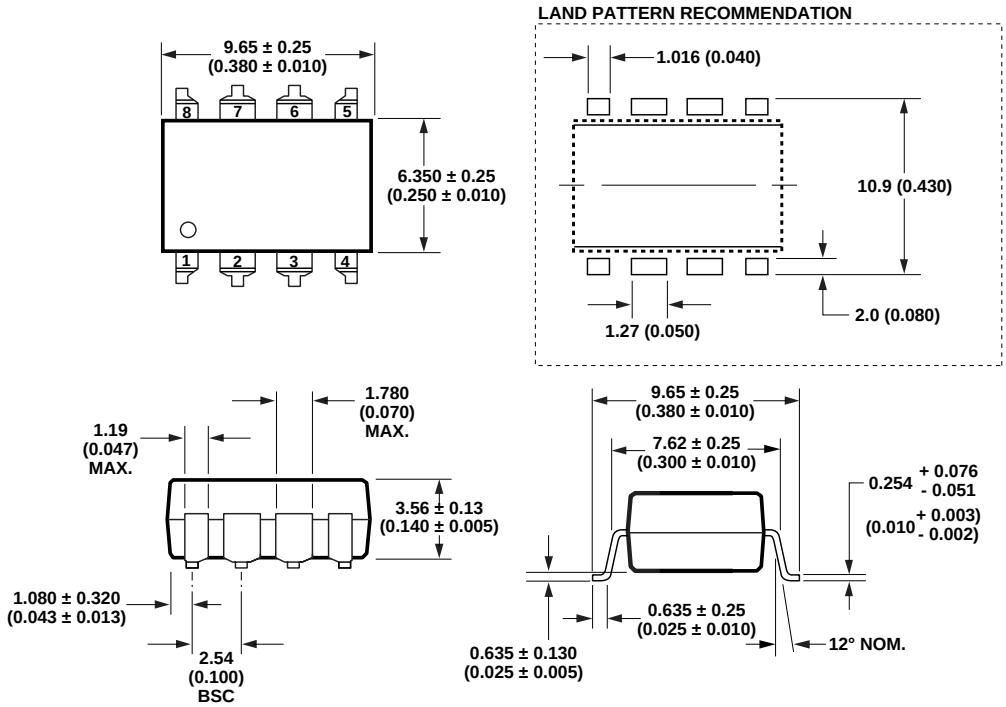
8-Pin DIP Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

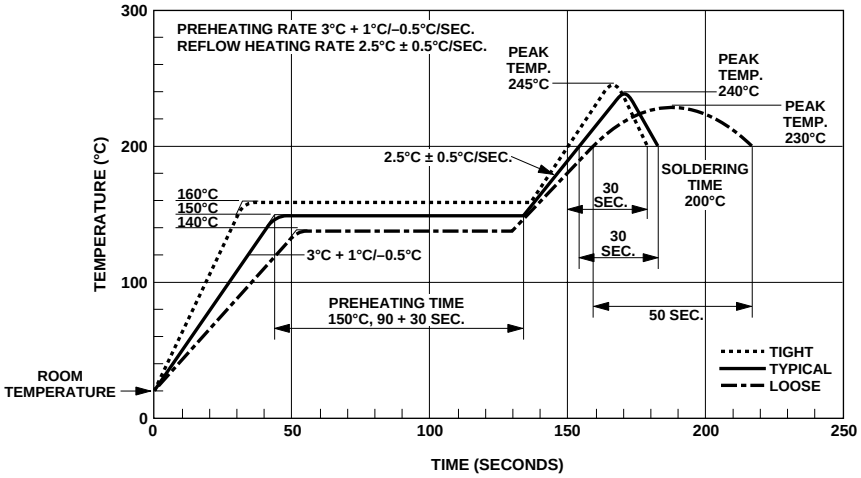
8-Pin DIP Package with Gull Wing Surface Mount Option 300



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

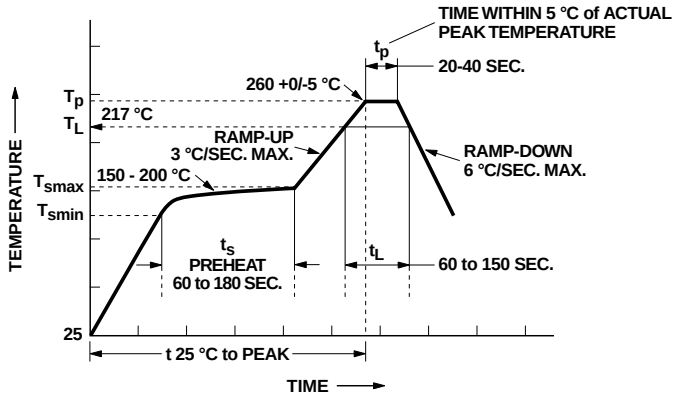
NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Solder Reflow Thermal Profile



Note: Non-halide flux should be used.

Recommended Pb-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

Note: Non-halide flux should be used.

Regulatory Information

The HCPL-2602/2612 have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(I01)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air.
Min. External Tracking Path (External Creepage)	L(I02)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body.
Min. Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	V	DIN IEC 112/ VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/ 89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings (No Derating Required up to 85°C)

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-55	125	°C
Operating Temperature	T_A	-40	85	°C
Forward Input Current	I_I		60	mA
Reverse Input Current	I_{IR}		60	mA
Input Current, Pin 4		-10	10	mA
Supply Voltage (1 Minute Maximum)	V_{CC}		7	V
Enable Input Voltage (Not to Exceed V_{CC} by more than 500 mV)	V_E		V_{CC} + 0.5	V
Output Collector Current	I_O		50	mA
Output Collector Voltage (Selection for Higher Output Voltages up to 20 V is Available.)	V_O		7	V
Output Collector Power Dissipation	P_O		40	mW
Lead Solder Temperature	T_{LS}	260°C for 10 sec., 1.6 mm below seating plane		
Solder Reflow Temperature Profile		See Package Outline Drawings section		

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{IL}	0	250	∝A
Input Current, High Level	I_{IH}	5*	60	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (@R_L = 1 kΩ)	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4 K	Ω
Operating Temperature	T_A	0	70	°C

*The initial switching threshold is 5 mA or less. It is recommended that an input current between 6.3 mA and 10 mA be used to obtain best performance and to provide at least 20% LED degradation guardband.

Electrical Characteristics

Over recommended temperature (T_A = 0°C to +70°C) unless otherwise specified. See note 1.

Parameter	Sym.	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}		5.5	100	∝A	V_{CC} = 5.5 V, V_O = 5.5 V, I_I = 250 ∝A, V_E = 2.0 V	1	
Low Level Output Voltage	V_{OL}		0.35	0.6	V	V_{CC} = 5.5 V, I_I = 5 mA, V_E = 2.0 V, I_{OL} (Sinking) = 13 mA	2, 4, 5, 14	
High Level Supply Current	I_{CCH}		7.5	10	mA	V_{CC} = 5.5 V, I_I = 0 mA, V_E = 0.5 V		
Low Level Supply Current	I_{CCL}		10	13	mA	V_{CC} = 5.5 V, I_I = 60 mA, V_E = 0.5 V		
High Level Enable Current	I_{EH}		-0.7	-1.6	mA	V_{CC} = 5.5 V, V_E = 2.0 V		
Low Level Enable Current	I_{EL}		-0.9	-1.6	mA	V_{CC} = 5.5 V, V_E = 0.5 V		
High Level Enable Voltage	V_{EH}	2.0			V			10
Low Level Enable Voltage	V_{EL}			0.8	V			
Input Voltage	V_I		2.0	2.4	V	I_I = 5 mA	3	
			2.3	2.7		I_I = 60 mA		
Input Reverse Voltage	V_R		0.75	0.95	V	I_R = 5 mA		
Input Capacitance	C_{IN}		90		pF	V_I = 0 V, f = 1 MHz		

*All typicals at V_{CC} = 5 V, T_A = 25°C.

Switching Specifications

Over recommended temperature (T_A = 0°C to +70°C), V_{CC} = 5 V, I_I = 7.5 mA, unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}		20	48	75	ns	T_A = 25°C		6, 7, 8	3
					100	ns				
Propagation Delay Time to Low Output Level	t_{PHL}		25	50	75	ns	T_A = 25°C		6, 7, 8	4
					100	ns				
Pulse Width Distortion	$\lvert t_{PHL}-t_{PLH}\rvert$			3.5	35	ns	R_L = 350 Ω, C_L = 15 pF		9	13
Propagation Delay Skew	t_{PSK}				40	ns				12, 13
Output Rise Time (10-90%)	t_r			24		ns			12	
Output Fall Time (90-10%)	t_f			10		ns			12	
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}			30		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V		10, 11	5
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}			20		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V		10, 11	6
Common Mode Transient Immunity at High Output Level	$\lvert CM_H\rvert$	HCPL-2602	1000	10,000		V/ ∝s	V_{CM} = 50 V	$V_{O(MIN)}$ = 2 V, R_L = 350 Ω, I_I = 0 mA, T_A = 25°C	13	7, 9, 10
		HCPL-2612	3500	15,000			V_{CM} = 300 V			
Common Mode Transient Immunity at Low Output Level	$\lvert CM_L\rvert$	HCPL-2602	1000	10,000		V/ ∝s	V_{CM} = 50 V	$V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, I_I = 7.5 mA, T_A = 25°C	13	8, 9 10
		HCPL-2612	3500	15,000			V_{CM} = 300 V			

*All typicals at V_{CC} = 5 V, T_A = 25°C.

Package Characteristics

All Typicals at T_A = 25°C

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	3750			V rms	RH ≤ 50%, t = 1 min., T_A = 25°C		2, 11
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc		2
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz		2

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/ EN/ DIN EN 60747-5-2 Insulation Characteristics Table (if applicable), your equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Bypassing of the power supply line is required, with a 0.1 ∝F ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 15. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20 mm.
2. Device considered a two terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
3. The t_{PLH} propagation delay is measured from the 3.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
4. The t_{PHL} propagation delay is measured from the 3.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.
5. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the falling edge of the enable input pulse to the 1.5 V point on the rising edge of the output pulse.
6. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the rising edge of the enable input pulse to the 1.5 V point on the falling edge of the output pulse.
7. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., $V_{OUT} > 2.0$ V).
8. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., $V_{OUT} < 0.8$ V).
9. For sinusoidal voltages,
$$\left|\frac{dv_{CM}}{dt}\right|_{max} = \pi f_{CM} V_{CM} \text{ (p-p)}$$
10. No external pull up is required for a high logic state on the enable input. If the V_E pin is not used, tying V_E to V_{CC} will result in improved CMR performance.
11. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage of ≥ 4500 for one second (leakage detection current limit, $I_{i-o} \leq 5$ ∝A).
12. t_{PSK} is equal to the worst case difference in t_{PHL} and/ or t_{PLH} that will be seen between units at any given temperature within the operating condition range.
13. See application section titled "Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew" for more information.

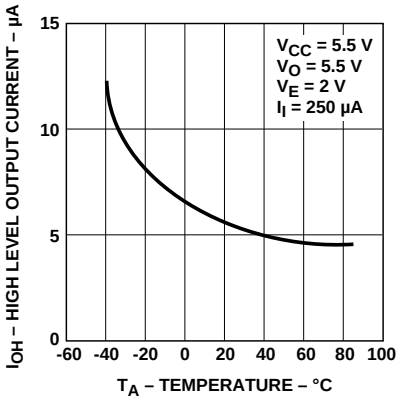


Figure 1. Typical high level output current vs. temperature.

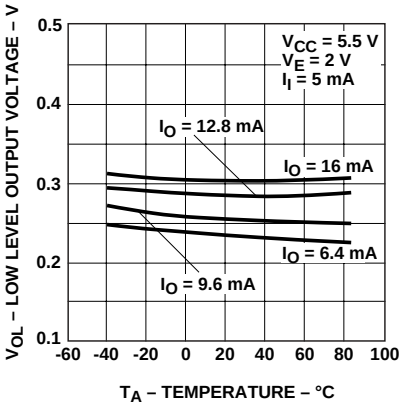


Figure 2. Typical low level output voltage vs. temperature.

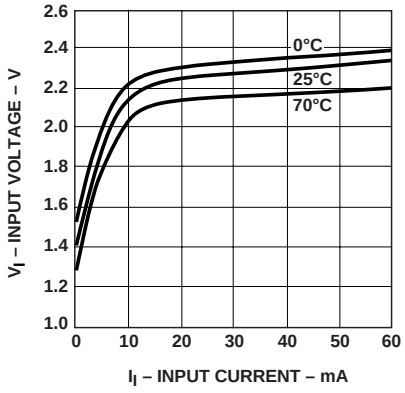


Figure 3. Typical input characteristics.

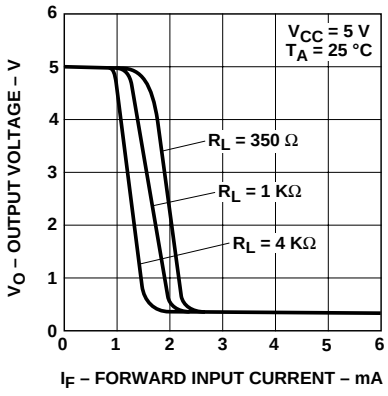


Figure 4. Typical output voltage vs. forward input current.

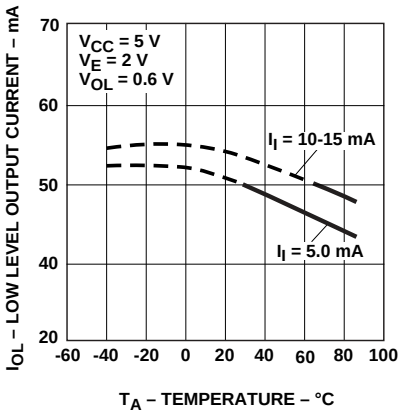


Figure 5. Typical low level output current vs. temperature.

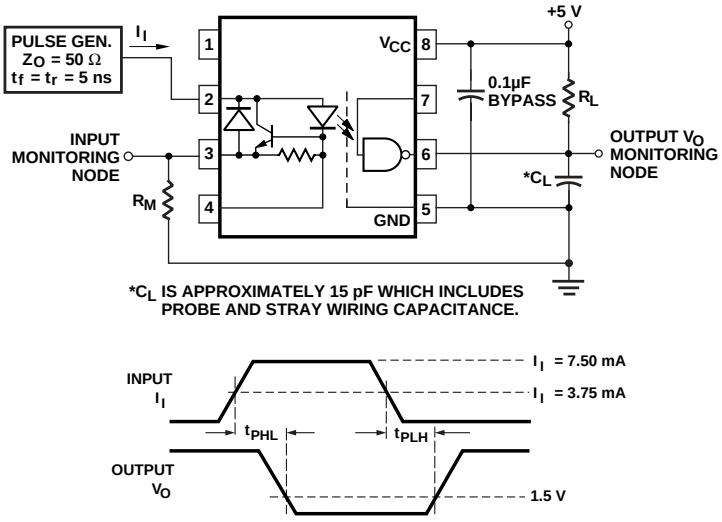


Figure 6. Test circuit for t_{PHL} and t_{PLH}.

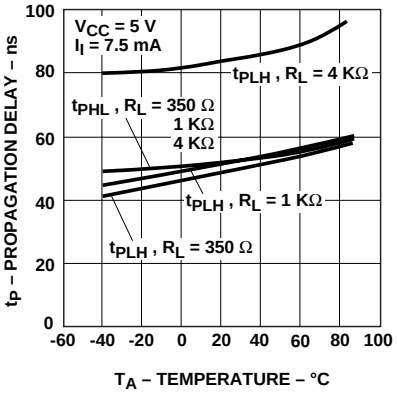


Figure 7. Typical propagation delay vs. temperature.

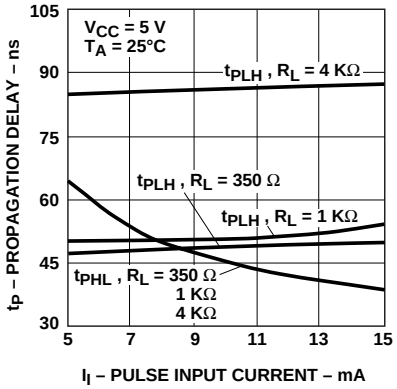


Figure 8. Typical propagation delay vs. pulse input current.

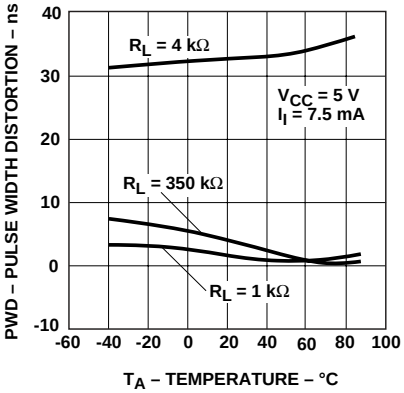


Figure 9. Typical pulse width distortion vs. temperature.

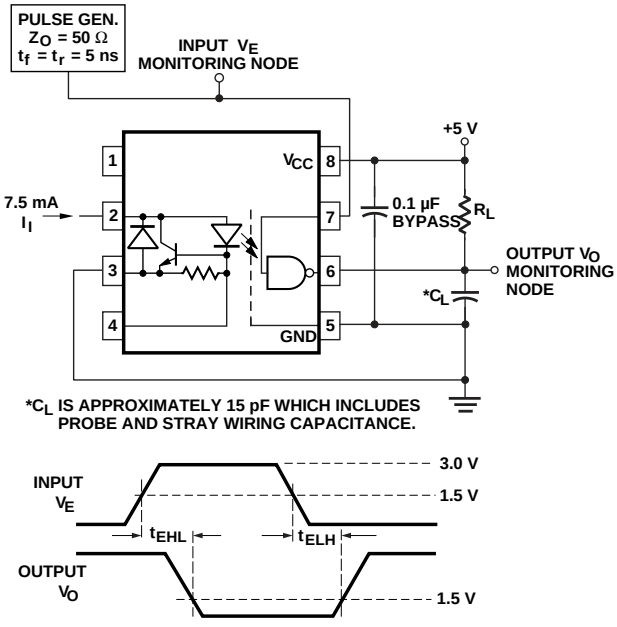


Figure 10. Test circuit for t_{EHL} and t_{ELH}.

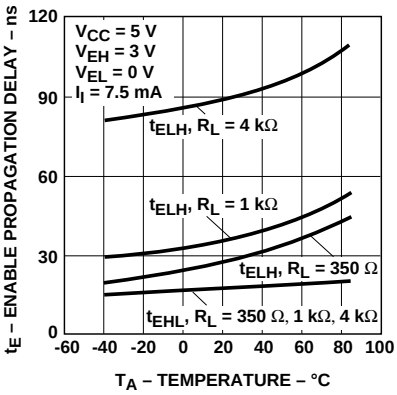


Figure 11. Typical enable propagation delay vs. temperature.

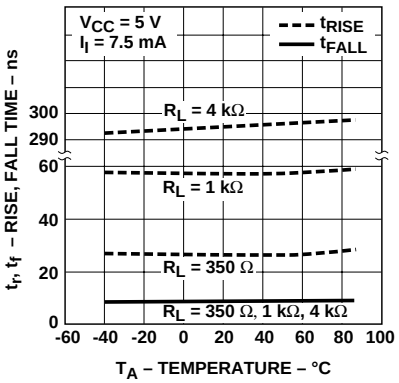


Figure 12. Typical rise and fall time vs. temperature.

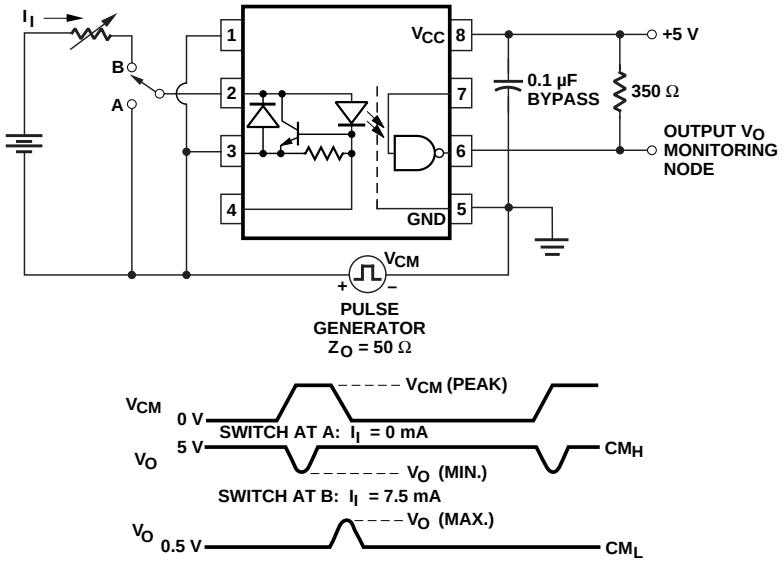


Figure 13. Test circuit for common mode transient immunity and typical waveforms.

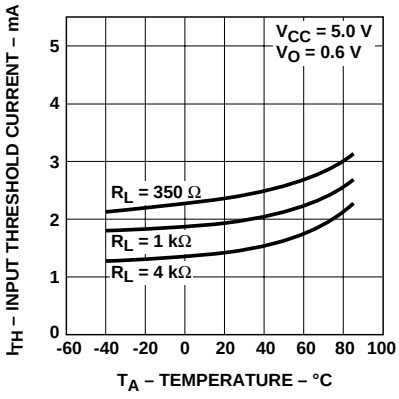


Figure 14. Typical input threshold current vs. temperature.

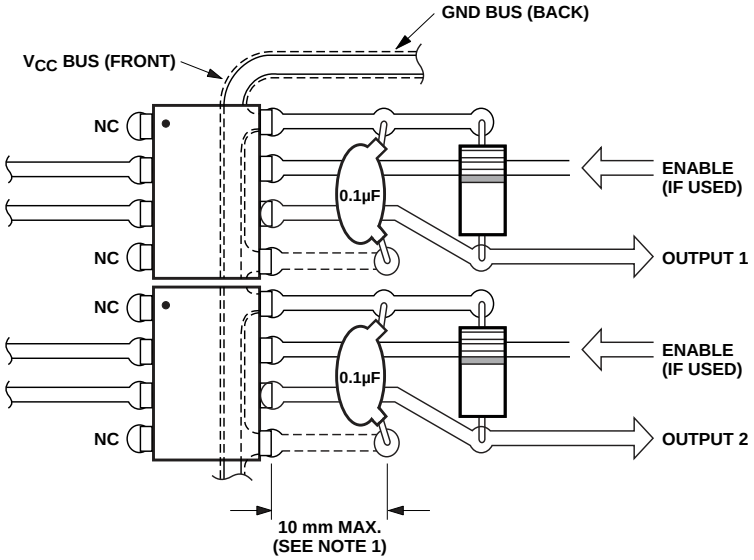


Figure 15. Recommended printed circuit board layout.

Using the HCPL-2602/ 12 Line Receiver Optocouplers

The primary objectives to fulfill when connecting an optocoupler to a transmission line are to provide a minimum, but not excessive, LED current and to properly terminate the line. The internal regulator in the HCPL-2602/12 simplifies this task. Excess current from variable drive conditions such as line length variations, line driver differences, and power supply fluctuations are shunted by the regulator. In fact, with the LED current regulated, the line current can be increased to improve the immunity of the system to differential-mode-noise and to enhance the data rate capability. The designer must keep in mind the 60 mA input current maximum rating of the HCPL-2602/12 in such cases, and may need to use series limiting or shunting to prevent overstress.

Design of the termination circuit is also simplified; in most cases the transmission line can simply be connected directly to the input terminals of the HCPL-2602/12 without the need for additional series or shunt resistors. If reversing line drive is used it may be desirable to use two HCPL-2602/12 or an external Schottky diode to optimize data rate.

Polarity Non-Reversing Drive

High data rates can be obtained with the HCPL-2602/12 with polarity non-reversing drive. Figure (a) illustrates how a 74S140 line driver can be used with the HCPL-2602/12 and shielded, twisted pair or coax cable without any additional components. There are some reflections due to the "active termination," but they do not interfere with circuit performance because the regulator clamps the line voltage. At longer line lengths, t_{PLH} increases faster than t_{PHL} since the switching threshold is not exactly halfway between asymptotic line conditions. If optimum data rate is desired, a series resistor and peaking capacitor can be used to equalize t_{PLH} and t_{PHL}. In general, the peaking capacitance should be as large as possible; however, if it is too large it may keep the regulator from achieving turn-off during the negative (or zero) excursions of the input signal. A safe rule:

make $C \leq 16t$

where:
C = peaking capacitance in picofarads
t = data bit interval in nanoseconds

Polarity Reversing Drive

A single HCPL-2602/12 can also be used with polarity reversing drive (Figure b). Current reversal is obtained by way of the substrate isolation diode (substrate to collector). Some reduction of data rate occurs, however, because the substrate diode stores charge, which must be removed when the current changes to the forward direction. The effect of this is a longer t_{PHL}. This effect can be eliminated and data rate improved considerably by use of a Schottky diode on the input of the HCPL-2602/12.

For optimum noise rejection as well as balanced delays, a split-phase termination should be used along with a flip-flop at the output (Figure c). The result of current reversal in split-phase operation is seen in Figure (c) with switches A and B both OPEN. The coupler inputs are then connected in ANTI-SERIES; however, because of the higher steady-state termination voltage, in comparison to the single HCPL-2602/12 termination, the forward current in the substrate diode is lower and consequently there is less junction charge to deal with when switching.

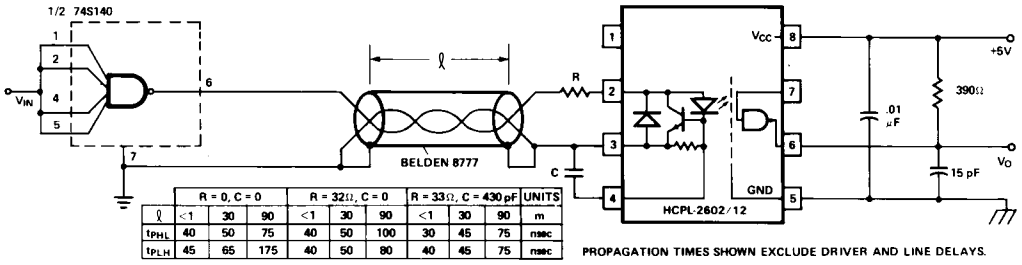
Closing switch B with A open is done mainly to enhance common mode rejection, but also reduces propagation delay slightly because line-to-line capacitance offers a slight peaking effect. With switches A and B both CLOSED, the shield acts as a current return path which prevents either input substrate diode from becoming reversed biased. Thus the data rate is optimized as shown in Figure (c).

Improved Noise Rejection

Use of additional logic at the output of two HCPL-2602/12s, operated in the split phase termination, will greatly improve system noise rejection in addition to balancing propagation delays as discussed earlier.

A NAND flip-flop offers infinite common mode rejection (CMR) for NEGATIVELY sloped common mode transients but requires $t_{PHL} > t_{PLH}$ for proper operation. A NOR flip-flop has infinite CMR for POSITIVELY sloped transients but requires $t_{PHL} < t_{PLH}$ for proper operation. An exclusive-OR flip-flop has infinite CMR for common mode transients of EITHER polarity and operates with either $t_{PHL} > t_{PLH}$ or $t_{PHL} < t_{PLH}$.

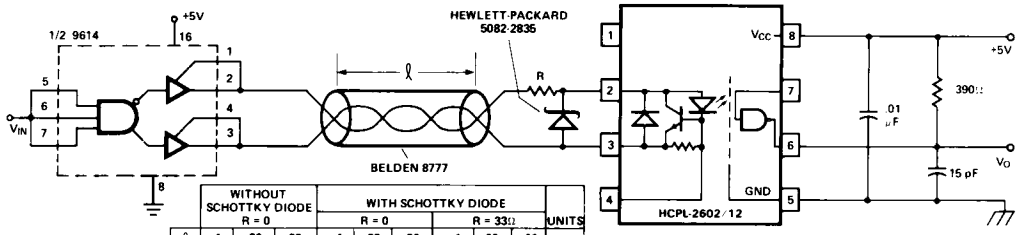
With the line driver and transmission line shown in Figure (c), $t_{PHL} > t_{PLH}$, so NAND gates are preferred in the R-S flip-flop. A higher drive amplitude or



	R = 0, C = 0			R = 32Ω, C = 0			R = 33Ω, C = 430 pF			UNITS
ℓ	<1	30	90	<1	30	90	<1	30	90	m
t_{PHL}	40	50	75	40	50	100	30	45	75	nsec
t_{PLH}	45	65	175	40	50	80	40	45	75	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

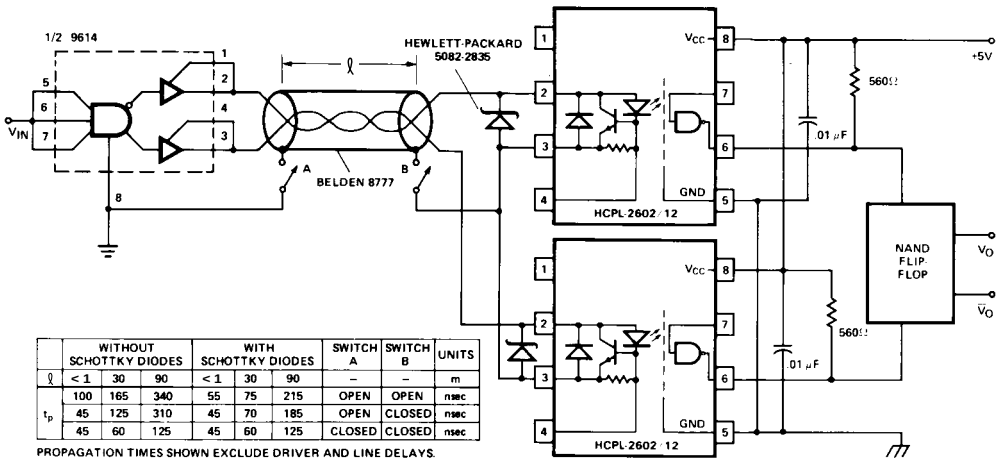
Figure a. Polarity non-reversing.



	WITHOUT SCHOTTKY DIODE R = 0			WITH SCHOTTKY DIODE R = 0			WITH SCHOTTKY DIODE R = 33Ω			UNITS
ℓ	<1	30	90	<1	30	90	<1	30	90	m
t_{PHL}	210	365	450	50	80	235	50	70	200	nsec
t_{PLH}	35	45	60	35	45	60	35	45	60	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

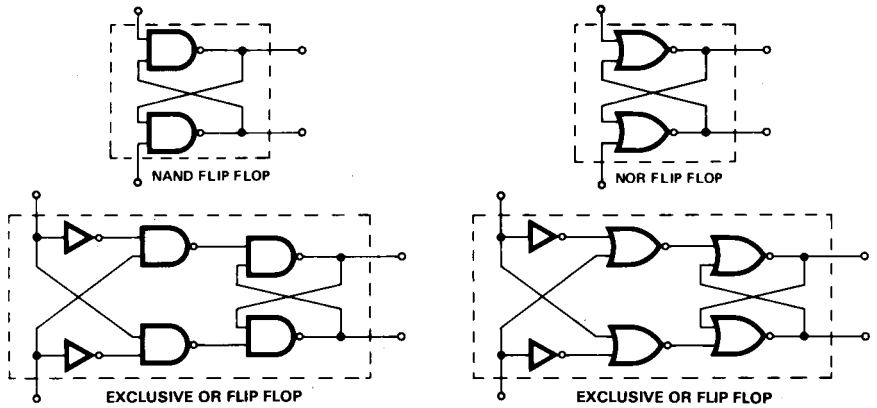
Figure b. Polarity reversing, single ended.



	WITHOUT SCHOTTKY DIODES			WITH SCHOTTKY DIODES			SWITCH A	SWITCH B	UNITS
ℓ	< 1	30	90	< 1	30	90	–	–	m
t_p	100	165	340	55	75	215	OPEN	OPEN	nsec
	45	125	310	45	70	185	OPEN	CLOSED	nsec
	45	60	125	45	60	125	CLOSED	CLOSED	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

Figure c. Polarity reversing, split phase.



NAND flip flop tolerates simultaneously HIGH inputs; NOR flip flop tolerates simultaneously LOW inputs; EXCLUSIVE-OR flip flop tolerates simultaneously HIGH OR LOW inputs without causing either of the outputs to change.

Figure d. Flip-flop configurations.

different circuit configuration could make $t_{PHL} < t_{PLH}$, in which case NOR gates would be preferred. If it is not known whether $t_{PHL} > t_{PLH}$ or $t_{PHL} < t_{PLH}$, or if the drive conditions may vary over the boundary for these conditions, the exclusive-OR flip-flop of Figure (d) should be used.

RS-422 and RS-423

Line drivers designed for RS-422 and RS-423 generally provide adequate voltage and current for operating the HCPL-2602/12. Most drivers also have characteristics allowing the HCPL-2602/12 to be connected directly to the driver terminals. Worst case drive conditions, however, would require current shunting to prevent overstress of the HCPL-2602/12.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 6).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 16, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PHL} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 17 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 17 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{PSK} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, input current, and power supply ranges.

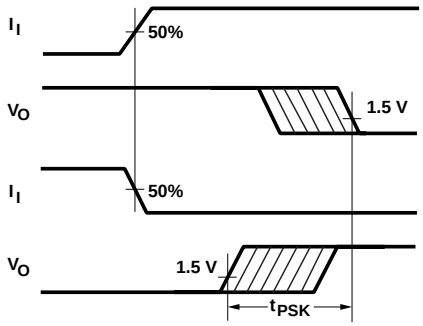


Figure 16. Illustration of propagation delay skew - t_{PSK}.

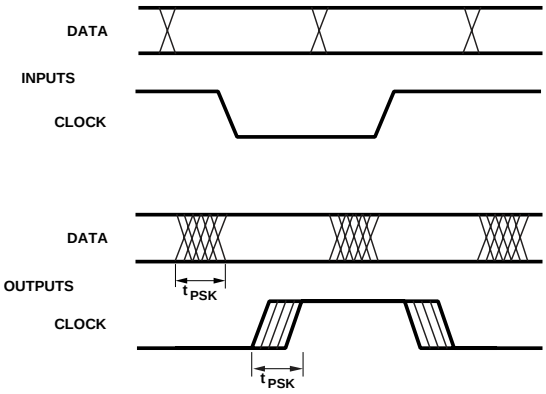


Figure 17. Parallel data transmission example.

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

AV01-0568EN July 18, 2007