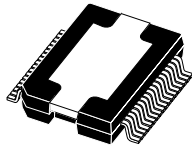


## 40 V, 4.5 A quad power half bridge



PowerSO-36  
with exposed pad up

### Features

- Multipower BCD technology
- Minimum input output pulse width distortion
- 200 m $\Omega$  R<sub>dsON</sub> complementary DMOS output stage
- CMOS compatible logic input
- Thermal protection
- Thermal warning output
- Undervoltage protection

### Description

**STA508** is a monolithic quad half bridge stage in Multipower BCD technology. The device can be used as dual bridge or reconfigured, by connecting CONFIG pin to V<sub>dd</sub> pin, as single bridge with double current capability, and as half bridge (Binary mode) with half current capability.

The device is particularly designed to make the output stage of a stereo all-digital high efficiency (DDX™) amplifier capable to deliver 80 + 80 W @ THD = 10 % at V<sub>CC</sub> = 35 V output power on 8  $\Omega$  load.

In single BTL configuration is also capable to deliver a peak of 160 W @ THD = 10 % at V<sub>CC</sub> = 35 V on 4  $\Omega$  load. The input pins have threshold proportional to V<sub>L</sub> pin voltage.

#### Maturity status link

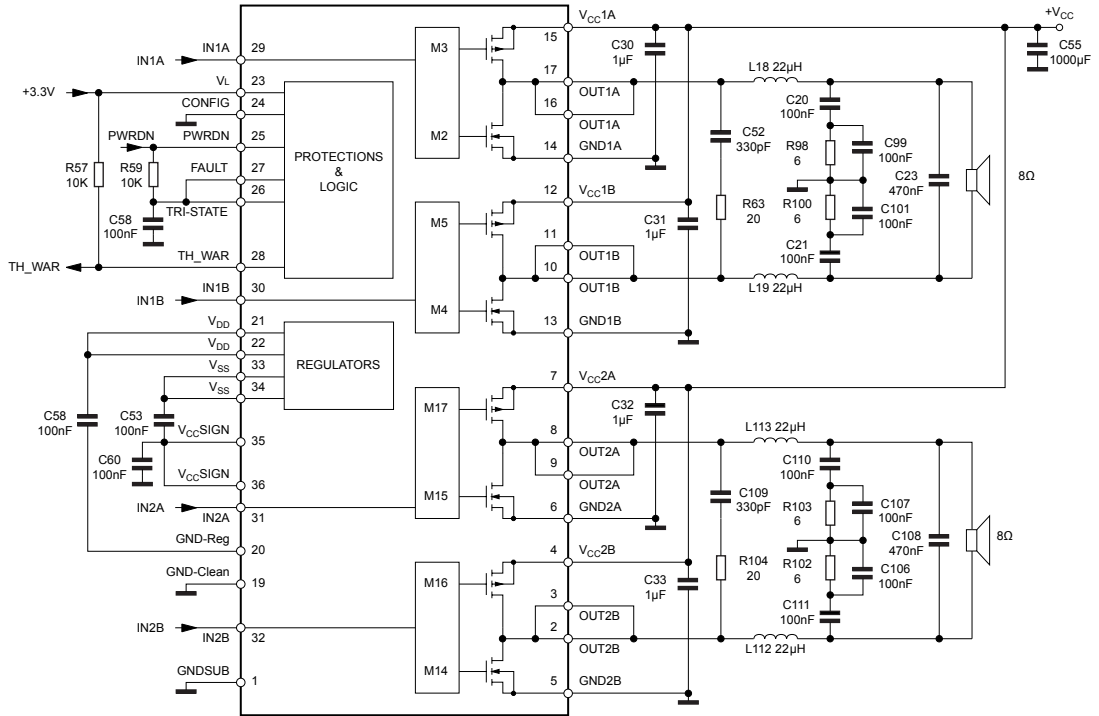
[STA508](#)

#### Device summary

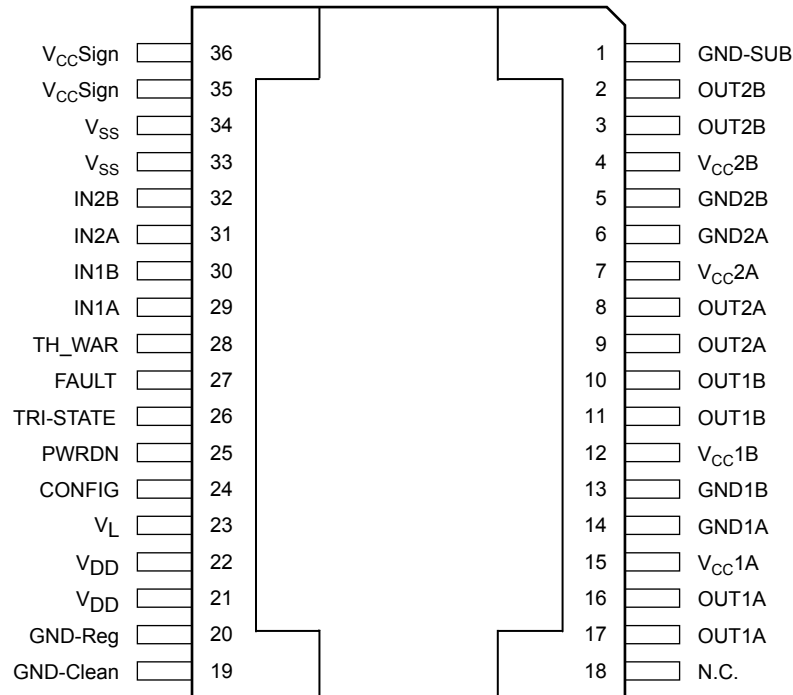
<b>Order code</b>	STA50813TR
<b>Package</b>	PowerSO-36 (EPU)

# 1 Diagram

Figure 1. Block diagram



## 2 Pin configuration

**Figure 2. Pin connection (top view)**

**Table 1. Pin description**

Pin N°	Name	Description
1	GND-SUB	Substrate ground
2, 3	OUT2B	Output half bridge 2B
4	V <sub>CC</sub> 2B	Positive supply
5	GND2B	Negative supply
6	GND2A	Negative supply
7	V <sub>CC</sub> 2A	Positive supply
8, 9	OUT2A	Output half bridge 2A
10, 11	OUT1B	Output half bridge 1B
12	V <sub>CC</sub> 1B	Positive supply
13	GND1B	Negative supply
14	GND1A	Negative supply
15	V <sub>CC</sub> 1A	Positive supply
16, 17	OUT1A	Output half bridge 1A
18	NC	Not connected
19	GND-clean	Logical ground
20	GND-Reg	Ground for regulator V <sub>dd</sub>

Pin N°	Name	Description
21, 22	V <sub>dd</sub>	5 V Regulator referred to Ground
23	V <sub>L</sub>	High logical state setting voltage
24	CONFIG	Configuration pin
25	PWRDN	Stand-by pin
26	TRI-STATE	Hi-Z pin
27	FAULT	Fault pin advisor
28	TH-WAR	Thermal warning advisor
29	IN1A	Input of half bridge 1A
30	IN1B	Input of half bridge 1B
31	IN2A	Input of half bridge 2A
32	IN2B	Input of half bridge 2B
33, 34	V <sub>ss</sub>	5 V regulator referred to + V <sub>CC</sub>
35, 36	V <sub>CC</sub> Sign	Signal positive supply

**Table 2. Functional pin status**

Pin name	Logical value	IC-STATUS
FAULT	0	Fault detected (Short circuit, or Thermal ..)
FAULT <sup>(1)</sup>	1	Normal operation
TRI-STATE	0	Allpowers in Hi-Z state
TRI-STATE	1	Normal operation
PWRDN	0	Low absorbion
PWRDN	1	Normal operation
THWAR	0	Temperature of the IC = 130 °C
THWAR <sup>(1)</sup>	1	Normal operation
CONFIG	0	Normal Operation
CONFIG <sup>(2)</sup>	1	OUT1A = OUT1B; OUT2A=OUT2B (If IN1A = IN1B; IN2A = IN2B)

1. The pin is open collector. To have the high logic value, it needs to be pulled up by a resistor.
2. To put CONFIG = 1 means connect Pin 24 (CONFIG) to Pins 21, 22 (V<sub>dd</sub>).

### 3 Maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage (Pin 4, 7, 12, 15)	40	V
$V_{max}$	Maximum voltage on pins 23 to 32	5.5	V
$P_{tot}$	Power dissipation ( $T_{case} = 70\text{ °C}$ )	50	W
$T_{op}$	Operating temperature range	- 40 to 90	°C
$T_{stg}$	Storage temperature	- 40 to 150	°C
$T_j$	Junction temperature		

**Table 4. Thermal data**

Symbol	Description	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	max 1.5	°C/W

## 4 Electrical characteristics

**Table 5. Electrical characteristics**  $V_L = 3.3\text{ V}$ ;  $V_{CC} = 30\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $f_{sw} = 384\text{ kHz}$  unless otherwise specified.

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{dsON}$	Power P-channel/N-channel MOSFET $R_{dsON}$	$I_d = 1\text{ A}$		200	270	mΩ
$I_{dss}$	Power P-channel/N-channel leakage $I_{dss}$	$V_{CC} = 35\text{ V}$			50	μA
$g_N$	Power P-channel $R_{dsON}$ matching	$I_d = 1\text{ A}$	95			%
$g_P$	Power N-channel $R_{dsON}$ matching	$I_d = 1\text{ A}$	95			%
$Dt_s$	Low current dead time (static)	See Figure 5		10	20	ns
$Dt_d$	High current dead time (dynamic)	$L = 22\text{ μH}$ ; $C = 470\text{ nF}$ ; $R_L = 8\text{ Ω}$ ; $I_d = 3.5\text{ A}$ ; see Figure 5			50	ns
$td_{ON}$	Turn-on delay time	Resistive load			100	ns
$td_{OFF}$	Turn-off delay time	Resistive load			100	ns
$t_r$	Rise time	Resistive load; as Figure 3			25	ns
$t_f$	Fall time	Resistive load; as Figure 3			25	ns
$V_{CC}$	Supply voltage operating voltage		10		36	V
$V_{IN-High}$	High level input voltage				$V_L/2 + 300\text{ mV}$	V
$V_{IN-Low}$	Low level input voltage		$V_L/2 - 300\text{ mV}$			V
$I_{IN-High}$	High level input current	Pin voltage = $V_L$		1		μA
$I_{IN-Low}$	Low level input current	Pin voltage = $0.3\text{ V}$		1		μA
$I_{PWRDN-H}$	High level PWRDN pin input current	$V_L = 3.3\text{ V}$		35		μA
$V_L$	Low logical state voltage $V_L$ (pin PWRDN, TRISTATE) <sup>(1)</sup>	$V_L = 3.3\text{ V}$	0.8			V
$V_H$	High logical state voltage $V_H$ (pin PWRDN, TRISTATE) <sup>(1)</sup>	$V_L = 3.3\text{ V}$			1.7	V
$I_{VCC-PWRDN}$	Supply CURRENT from $V_{CC}$ in Power Down	PWRDN = 0			3	mA
$I_{FAULT}$	Output current pins Fault -th-warn when Fault conditions	$V_{pin} = 3.3\text{ V}$		1		mA
$I_{VCC-hiz}$	Supply current from $V_{CC}$ in Tri-state	$V_{CC} = 30\text{ V}$ ; Tri-state = 0		22		mA
$I_{VCC}$	Supply current from $V_{CC}$ in operation both channel switching)	$V_{CC} = 30\text{ V}$ ; Input pulse width = 50% duty; Switching frequency = 384 kHz; No LC filters		50		mA
$I_{VCC-q}$	$I_{sc}$ (short circuit current limit) <sup>(2)</sup>		4.5	6	9	A
$V_{UV}$	Undervoltage protection threshold			7		V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{pw-min}$	Output minimum pulse width	No load	70		150	ns

1. See Table 6.  $V_{Low}$ ,  $V_{High}$  variation with  $V_L$ .
2. See relevant Application Note AN1994

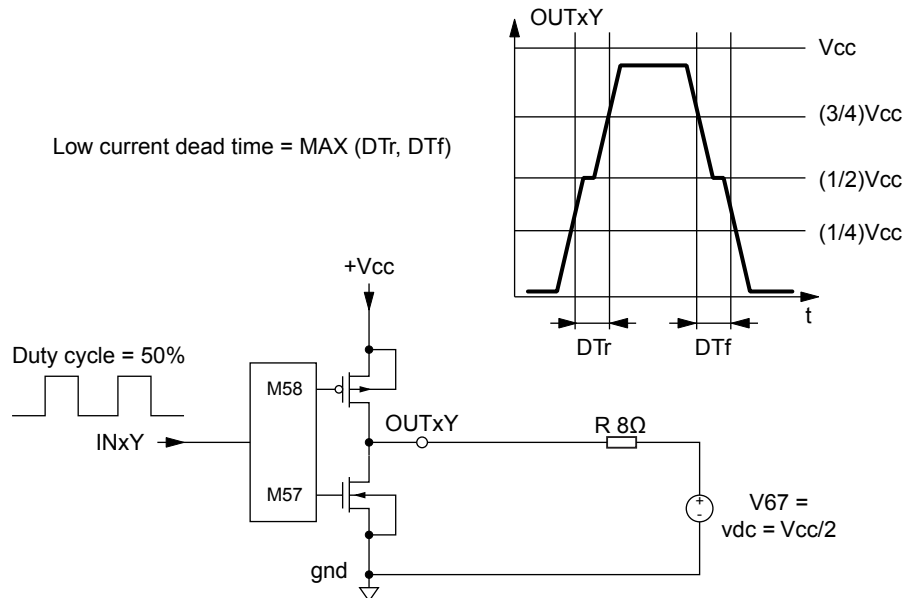
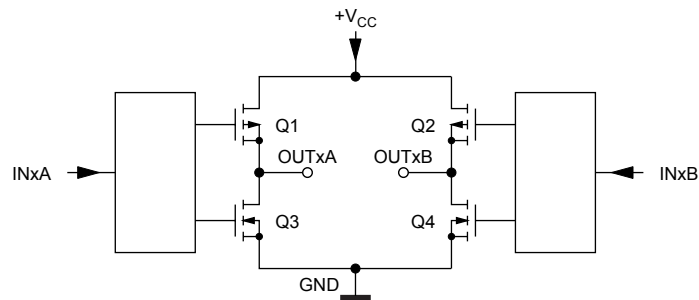
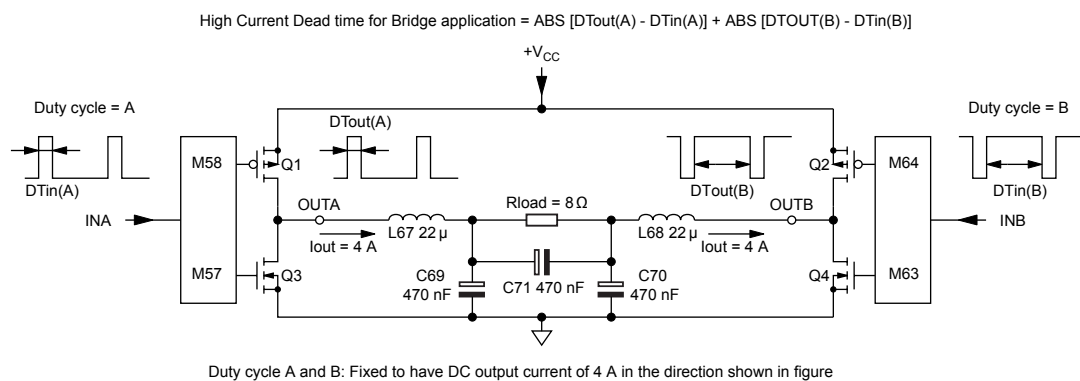
**Table 6.  $V_{Low}$ ,  $V_{High}$  variation with  $V_L$** 

$V_L$	$V_{Low}$ min	$V_{High}$ max	Unit
2.7	0.7	1.5	V
3.3	0.8	1.7	V
5	0.85	1.85	V

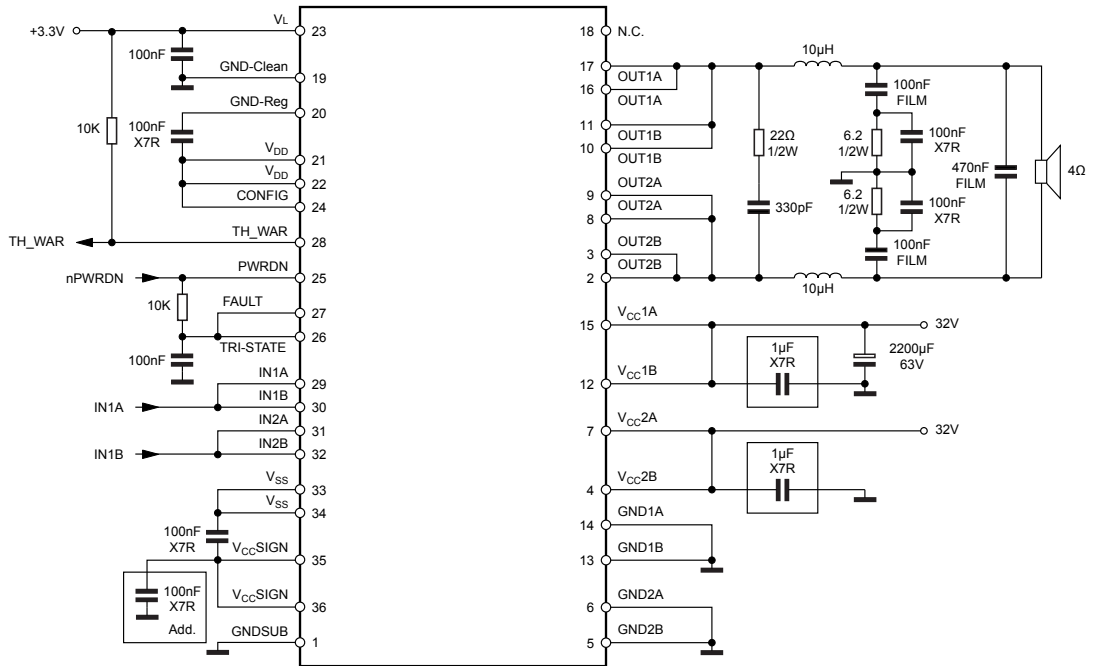
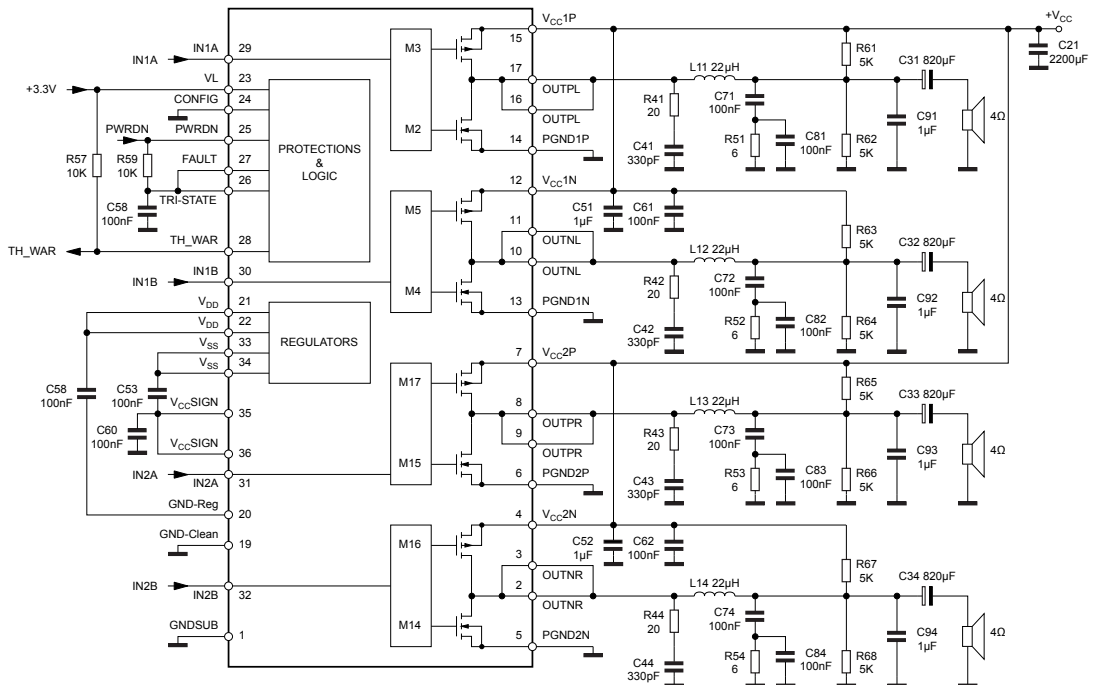
**Table 7. Logic truth table (see fig. 5)**

Tri-state	INxA	INxB	Q1	Q2	Q3	Q4	Output mode
0	x	x	OFF	OFF	OFF	OFF	Hi-Z
1	0	0	OFF	OFF	ON	ON	DUMP
1	0	1	OFF	ON	ON	OFF	NEGATIVE
1	1	0	ON	OFF	OFF	ON	POSITIVE
1	1	1	ON	ON	OFF	OFF	Not used

## 5 Test circuits and typical application diagrams

**Figure 3. Test circuit 1**

**Figure 4. Test circuit 2**

**Figure 5. Test circuit 3**




**Figure 6. Typical single BTL configuration**

**Figure 7. Typical quad half bridge configuration**


For more information refer to the application note AN1661.

## 6 Package information

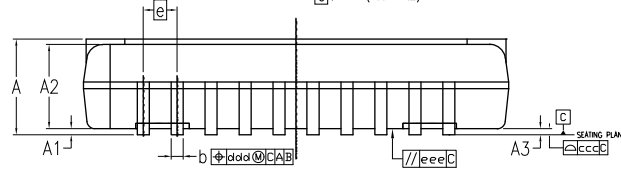
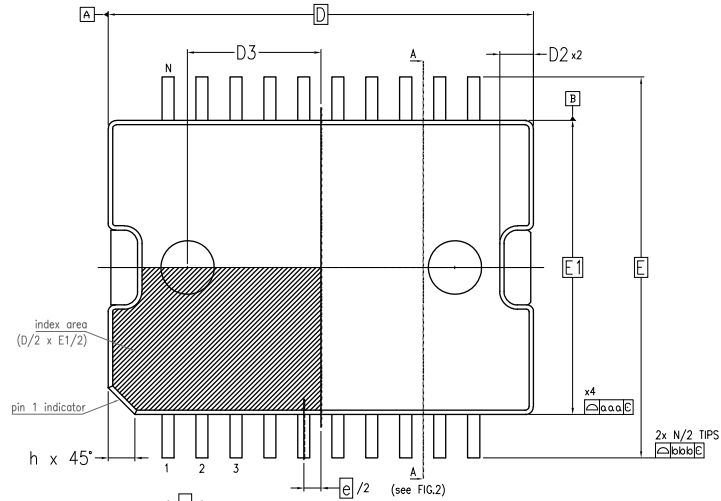
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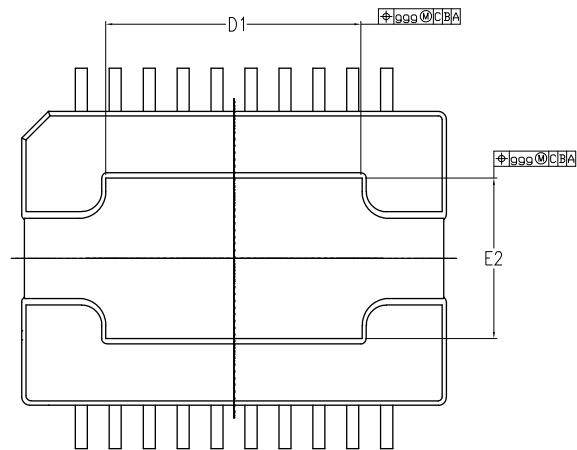
## 6.1 PowerSO-36 exposed pad up package information

Figure 8. PowerSO-36 exposed pad up package outline

BOTTOM VIEW

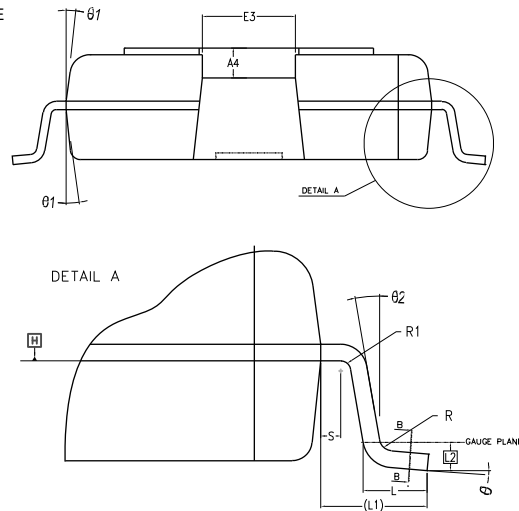


TOP VIEW

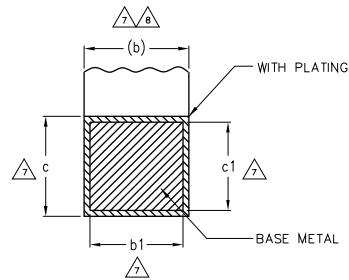


**Figure 9. PowerSO-36 section A-A and B-B package outline**
**SECTION A-A**

NOT TO SCALE


**SECTION B-B**

NOT TO SCALE



**Table 8. PowerSO-36 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
Θ	0°	-	8°
Θ1	5°	-	10°
Θ2	0°	-	-
A	-	-	3.41
A1	0.30	-	-0.40
A2	3.10	3.14	3.18
A3	-	0.2	-
A4	0.80	-	1.00
b	0.22	-	0.41
b1	0.22	-	0.38
c	0.23	-	0.32
c1	0.23	0.25	0.29
D	15.90 BSC		
D1	VARIATION		
D2		-	1.00
D3	-	5.00	-
e	0.65 BSC		
E	14.20 BSC		
E1	11.00 BSC		
E2	VARIATION		
E3	-	-	2.90
h	-	-	1.10
L	0.80	-	1.10
L1	1.60 REF		
L2	0.35 BSC		
N	36		
R	0.20	-	-
R1	0.20	-	-
s	0.25	-	-

**Table 9. Tolerance of form and position**

Symbol	Databook
aaa	0.10
bbb	0.30
ccc	0.075
ddd	0.25
eee	0.10
ggg	0.25
Note	1.2

**Table 10. Variations**

Symbol	Databook			Opt.
	Min.	Typ.	Max.	
D1	9.40	-	9.80	A
E2	5.80	-	6.20	

## Revision history

**Table 11. Document revision history**

Date	Revision	Changes
Sep 1994	1	Initial release.
Jun 2004	2	Note 2: See relevant Application Note AN1994
Nov 2004	3	Changed $V_{CC}$ from 9 min to 10 min
Feb 2006	4	Changed $T_{op}$ value on Table 5.
01-Sep-2020	5	Updated order code in device summary on the cover page.
19-Nov-2020	6	Updated package name, Figure 2 and Section 6.1 PowerSO-36 exposed pad up package information.

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## Contents

<b>1</b>	<b>Diagram .....</b>	<b>2</b>
<b>2</b>	<b>Pin configuration .....</b>	<b>3</b>
<b>3</b>	<b>Maximum ratings .....</b>	<b>5</b>
<b>4</b>	<b>Electrical characteristics .....</b>	<b>6</b>
<b>5</b>	<b>Test circuits and typical application diagrams .....</b>	<b>8</b>
<b>6</b>	<b>Package information .....</b>	<b>10</b>
<b>6.1</b>	<b>PowerSO36 package information .....</b>	<b>11</b>
	<b>Revision history .....</b>	<b>15</b>



## List of tables

<b>Table 1.</b>	Pin description . . . . .	3
<b>Table 2.</b>	Functional pin status . . . . .	4
<b>Table 3.</b>	Absolute maximum ratings . . . . .	5
<b>Table 4.</b>	Thermal data . . . . .	5
<b>Table 5.</b>	Electrical characteristics $V_L = 3.3\text{ V}$ ; $V_{CC} = 30\text{ V}$ ; $T_{amb} = 25\text{ }^\circ\text{C}$ ; $f_{sw} = 384\text{ kHz}$ unless otherwise specified. . . . .	6
<b>Table 6.</b>	VLow, VHigh variation with $V_L$ . . . . .	7
<b>Table 7.</b>	Logic truth table (see fig. 5) . . . . .	7
<b>Table 8.</b>	PowerSO-36 package mechanical data . . . . .	13
<b>Table 9.</b>	Tolerance of form and position . . . . .	14
<b>Table 10.</b>	Variations . . . . .	14
<b>Table 11.</b>	Document revision history . . . . .	15

## List of figures

<b>Figure 1.</b>	Block diagram . . . . .	2
<b>Figure 2.</b>	Pin connection (top view) . . . . .	3
<b>Figure 3.</b>	Test circuit 1 . . . . .	8
<b>Figure 4.</b>	Test circuit 2 . . . . .	8
<b>Figure 5.</b>	Test circuit 3 . . . . .	8
<b>Figure 6.</b>	Typical single BTL configuration . . . . .	9
<b>Figure 7.</b>	Typical quad half bridge configuration . . . . .	9
<b>Figure 8.</b>	PowerSO-36 exposed pad up package outline . . . . .	11
<b>Figure 9.</b>	PowerSO-36 section A-A and B-B package outline . . . . .	12

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