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# Translating Bus Exchange Switch

## 7WBD383

The 7WBD383 is an advanced high-speed low-power translating bus exchange switch in ultra-small footprints.

### Features

- High Speed:  $t_{PD} = 0.25 \text{ ns (Max) @ } V_{CC} = 4.5 \text{ V}$
- $3 \Omega$  Switch Connection Between 2 Ports
- Power Down Protection Provided on Inputs
- Zero Bounce
- TTL-Compatible Control Inputs
- Ultra-Small Pb-Free Packages
- These are Pb-Free Devices



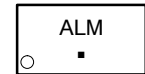
**ON Semiconductor®**

[www.onsemi.com](http://www.onsemi.com)

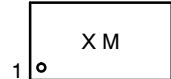
### MARKING DIAGRAMS



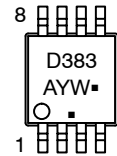
**UDFN8**  
MU SUFFIX  
CASE 517AJ



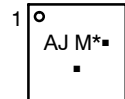
**UDFN8**  
1.95 x 1.0  
CASE 517CA



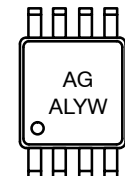
**Micro8**  
DM SUFFIX  
CASE 846A



**UQFN8**  
MU SUFFIX  
CASE 523AN



**US8**  
US SUFFIX  
CASE 493



Commercial

AL, X, D383, AJ, AG	= Specific Device Code
M	= Date Code
A	= Assembly Location
L	= Lot Code
Y	= Year Code
W	= Week Code
▪	= Pb-Free Package

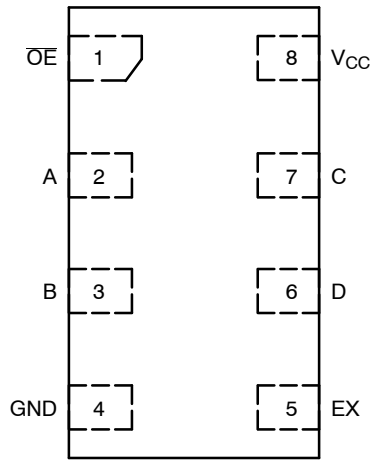
(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

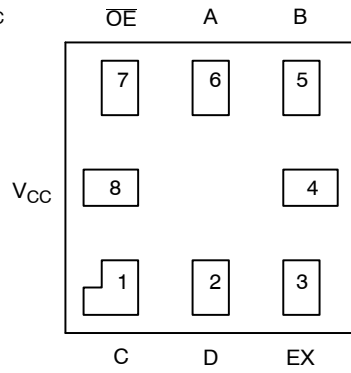
### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

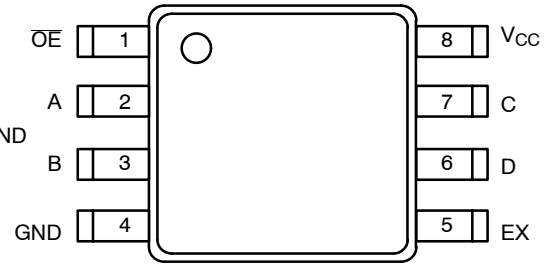
# 7WBD383



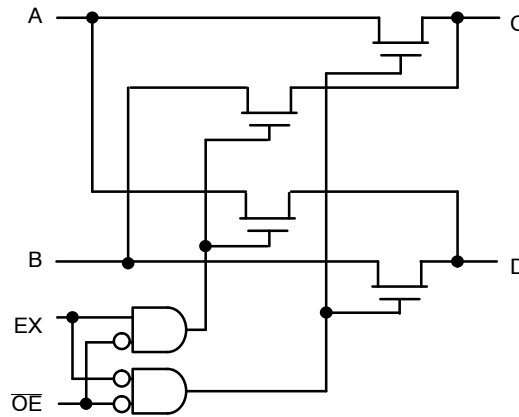
**Figure 1. UDFN8**  
(Top Thru-View)



**Figure 2. UQFN8**  
(Top Thru-View)



**Figure 3. US8/Micro8**  
(Top View)



**Figure 4. Logic Diagram**

## FUNCTION TABLE

Input $\overline{OE}$	Input EX	Function
L	L	A = C; B = D
L	H	A = D; B = C
H	X	Disconnect

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
$V_{CC}$	DC Supply Voltage	-0.5 to +7.0	V	
$V_{IN}$	Control Pin Input Voltage	-0.5 to +7.0	V	
$V_{I/O}$	Switch Input / Output Voltage	-0.5 to +7.0	V	
$I_{IK}$	Control Pin DC Input Diode Current $V_{IN} < GND$	-50	mA	
$I_{OK}$	Switch I/O Port DC Diode Current $V_{I/O} < GND$	-50	mA	
$I_O$	ON-State Switch Current	$\pm 128$	mA	
	Continuous Current Through $V_{CC}$ or GND	$\pm 150$	mA	
$I_{CC}$	DC Supply Current Per Supply Pin	$\pm 150$	mA	
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 150$	mA	
$T_{STG}$	Storage Temperature Range	-65 to +150	$^{\circ}C$	
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds	260	$^{\circ}C$	
$T_J$	Junction Temperature Under Bias	150	$^{\circ}C$	
$\theta_{JA}$	Thermal Resistance	US8 (Note 1)	251	$^{\circ}C/W$
		UDFN8	111	
		UQFN8	208	
		Micro8	392	
$P_D$	Power Dissipation in Still Air at 85 $^{\circ}C$	US8	498	mW
		UDFN8	1127	
		UQFN8	601	
		Micro8	319	
MSL	Moisture Sensitivity	Level 1		
$F_R$	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in		
$V_{ESD}$	ESD Withstand Voltage Human Body Mode (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000	V	
		> 200		
		N/A		
$I_{LATCHUP}$	Latchup Performance Above $V_{CC}$ and Below GND at 125 $^{\circ}C$ (Note 5)	$\pm 200$	mA	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA / JESD22-A114-A.
3. Tested to EIA / JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA / JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Positive DC Supply Voltage	4.0	5.5	V
$V_{IN}$	Control Pin Input Voltage	0	5.5	V
$V_{I/O}$	Switch Input / Output Voltage	0	5.5	V
$T_A$	Operating Free-Air Temperature	-55	+125	$^{\circ}C$
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate Control Input Switch I/O	0	5	nS/V
		0	DC	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# 7WBD383

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IK</sub>	Clamp Diode Voltage	I <sub>I/O</sub> = -18 mA	4.5			-1.2		-1.2	V
V <sub>IH</sub>	High-Level Input Voltage (Control)		4.0 to 5.5	2.0			2.0		V
V <sub>IL</sub>	Low-Level Input Voltage (Control)		4.0 to 5.5			0.8		0.8	V
V <sub>OH</sub>	Output Voltage High	See Figure 5							
I <sub>IN</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ 5.5 V	5.5			±0.1		±1.0	μA
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>I/O</sub> = 0 to 5.5 V	0			±0.1		±1.0	μA
I <sub>CC</sub>	Quiescent Supply Current	I <sub>O</sub> = 0, V <sub>IN</sub> = V <sub>CC</sub> or 0 V OE = GND OE = V <sub>CC</sub>	5.5			±1.0 ±0.1		±1.0 ±1.0	mA μA
ΔI <sub>CC</sub>	Increase in Supply Current (Control Pin)	One input at 3.4 V; Other inputs at V <sub>CC</sub> or GND	5.5					2.5	mA
R <sub>ON</sub>	Switch ON Resistance	V <sub>I/O</sub> = 0, I <sub>I/O</sub> = 64 mA I <sub>I/O</sub> = 30 mA	4.5		3 3	7 7		7 7	Ω
		V <sub>I/O</sub> = 2.4, I <sub>I/O</sub> = 15 mA			15	50		50	
		V <sub>I/O</sub> = 2.4, I <sub>I/O</sub> = 15 mA	4.0		50	70		70	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = 25 °C			T <sub>A</sub> = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
t <sub>PD</sub>	Propagation Delay, Bus to Bus	See Figure 6	4.0 to 5.5			0.25		0.25	ns
t <sub>PD-EX</sub>	Propagation Delay, EX to Bus	See Figure 6 and Figure 7	4.0 to 5.5			4.5		4.5	ns
t <sub>EN</sub>	Output Enable Time	See Figure 6	4.5 to 5.5	0.8	2.5	4.2	0.8	4.2	ns
			4.0	0.8	3.0	4.6	0.8	4.6	
t <sub>DIS</sub>	Output Disable Time		4.5 to 5.5	0.8	3.0	4.8	0.8	4.8	ns
			4.0	0.8	2.9	4.4	0.8	4.4	
C <sub>IN</sub>	Control Input Capacitance	V <sub>IN</sub> = 5 or 0 V	5.0		2.5				pF
C <sub>IO(ON)</sub>	Switch On Capacitance	Switch ON	5.0		10				pF
C <sub>IO(OFF)</sub>	Switch Off Capacitance	Switch OFF	5.0		5				pF

# 7WBD383

## TYPICAL DC CHARACTERISTICS

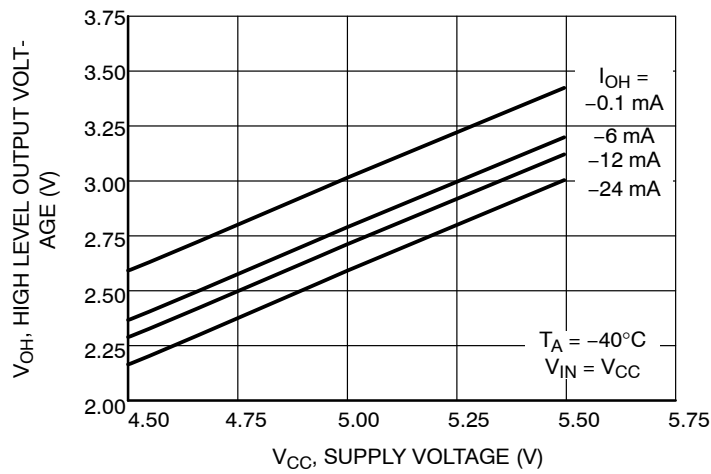
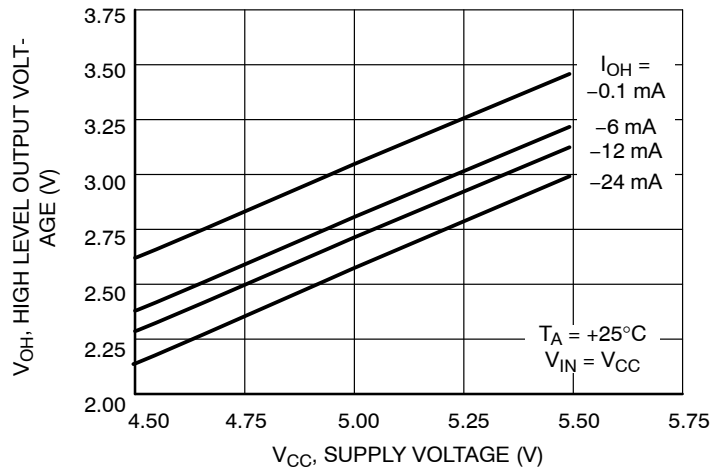
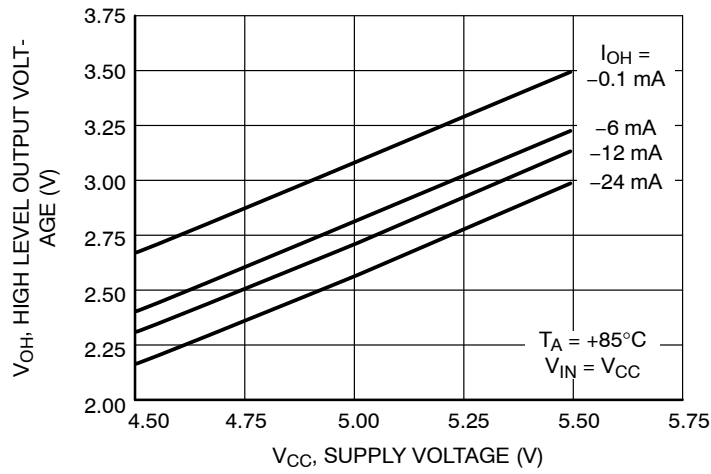
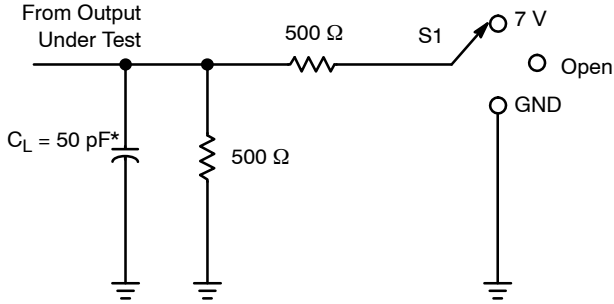


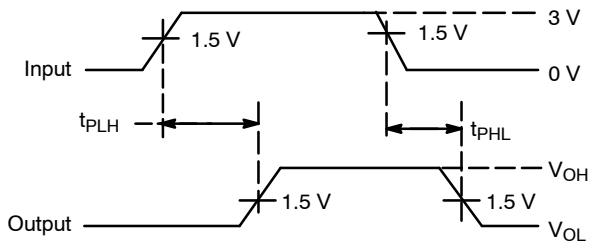
Figure 5. Output Voltage High vs Supply Voltage

AC LOADING AND WAVEFORMS

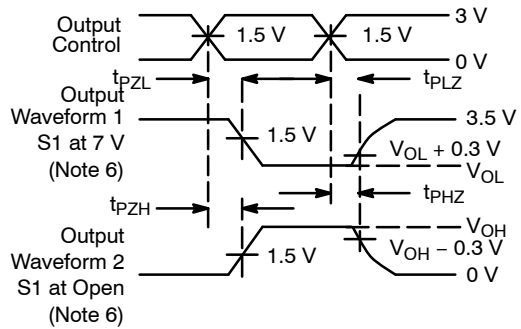


Test	S1
$t_{PD}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open

\* $C_L$  includes probes and jig capacitance.



Voltage Waveforms  
Propagation Delay Times



Voltage Waveforms  
Enable and Disable Times

6. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control
7. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
8. The outputs are measured one at a time, with one transition per measurement.
9.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{DIS}$ .
10.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{EN}$ .
11.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{PD}$ .

Figure 6.  $t_{PD}$ ,  $t_{EN}$ ,  $t_{DIS}$  Loading and Waveforms

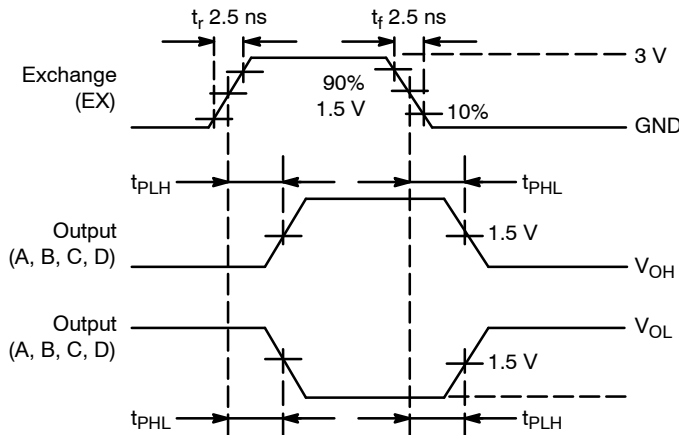


Figure 7.  $t_{PD-EX}$  Waveforms

## 7WBD383

### ORDERING INFORMATION

Device	Package	Shipping†
7WBD383USG	US8 (Pb-Free)	3000 / Tape & Reel
7WBD383MUTAG	UDFN8 (Pb-Free)	3000 / Tape & Reel
7WBD383AMUTCG	UQFN8 (Pb-Free)	3000 / Tape & Reel
7WBD383DMR2G	Micro8 (Pb-Free)	4000 / Tape & Reel
7WBD383DMUTCG	UDFN8, 1.95 x 1.0, 0.5 mm Pitch (Pb-Free)	3000 / Tape & Reel

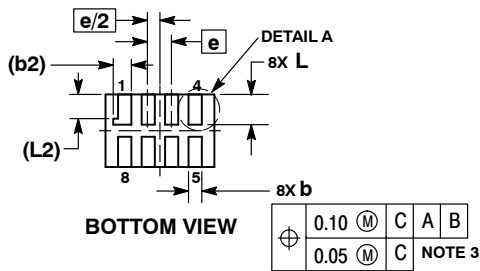
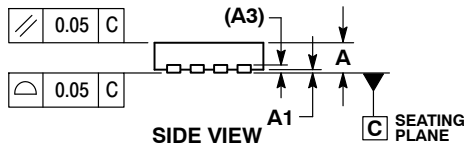
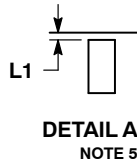
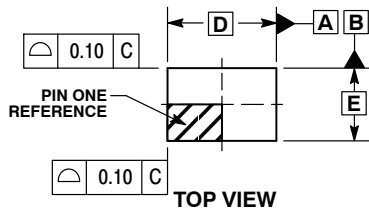
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



# 7WBD383

## PACKAGE DIMENSIONS

UDFN8 1.8 x 1.2, 0.4P  
CASE 517AJ  
ISSUE O

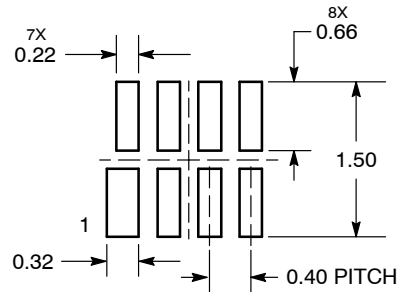


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127	REF
b	0.15	0.25
b2	0.30	REF
D	1.80	BSC
E	1.20	BSC
e	0.40	BSC
L	0.45	0.55
L1	0.00	0.03
L2	0.40	REF

**MOUNTING FOOTPRINT\*  
SOLDEMASK DEFINED**



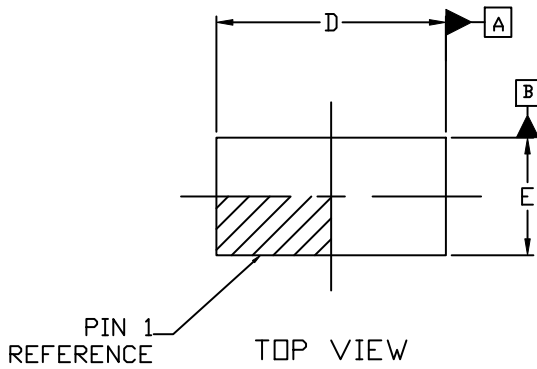
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# 7WBD383

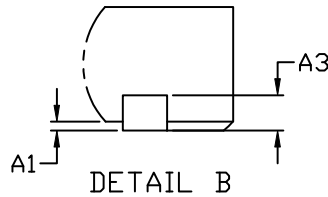
## PACKAGE DIMENSIONS

UDFN8 1.95x1.0, 0.5P  
CASE 517CA  
ISSUE A

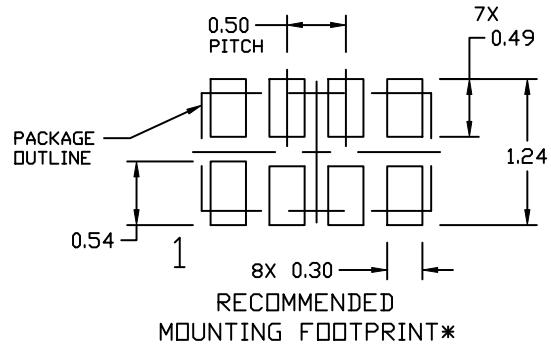
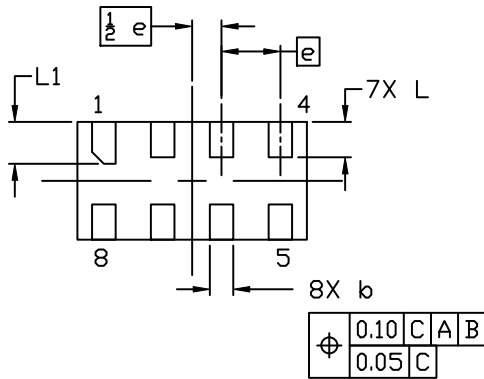
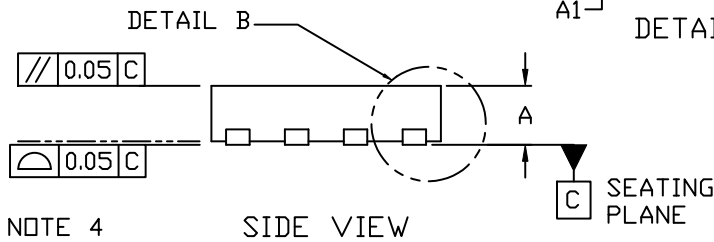


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO ALL THE TERMINALS.
5. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.45	0.50	0.55
A1	0.00	---	0.05
A3	0.13 REF		
b	0.15	0.20	0.25
D	1.85	1.95	2.05
E	0.90	1.00	1.10
e	0.50 BSC		
L	0.25	0.30	0.35
L1	0.30	0.35	0.40

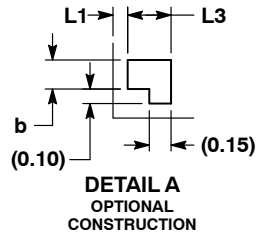
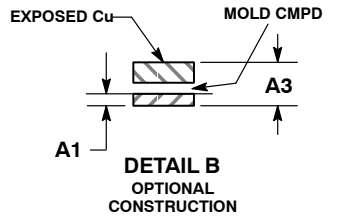
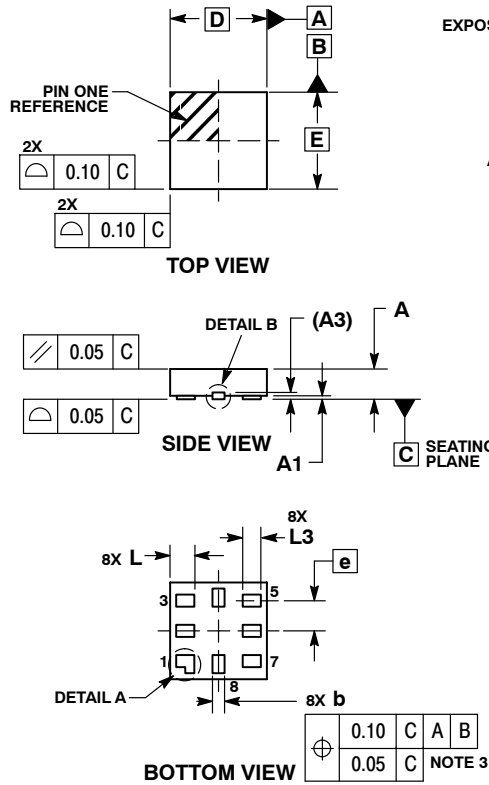


\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

# 7WBD383

## PACKAGE DIMENSIONS

UQFN8, 1.6x1.6, 0.5P  
CASE 523AN  
ISSUE O

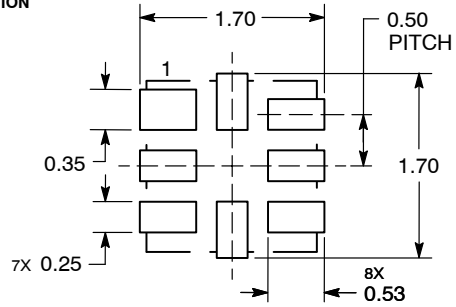


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	1.60	BSC
E	1.60	BSC
e	0.50	BSC
L	0.35	0.45
L1	---	0.15
L3	0.25	0.35

**SOLDERING FOOTPRINT\***



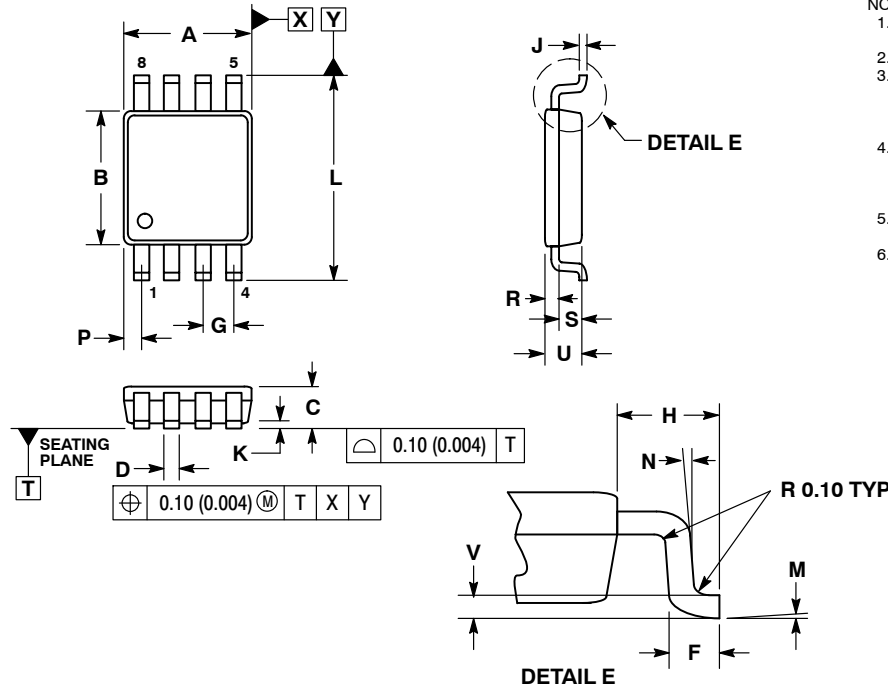
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# 7WBD383

## PACKAGE DIMENSIONS

US8  
CASE 493  
ISSUE D

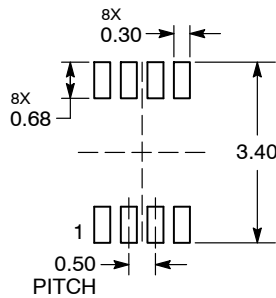


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.14MM (0.0055") PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.14MM (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203MM (0.003-0.008").
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508MM (0.0002").

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.128
M	0°	6°	0°	6°
N	0°	10°	0°	10°
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

### RECOMMENDED SOLDERING FOOTPRINT\*



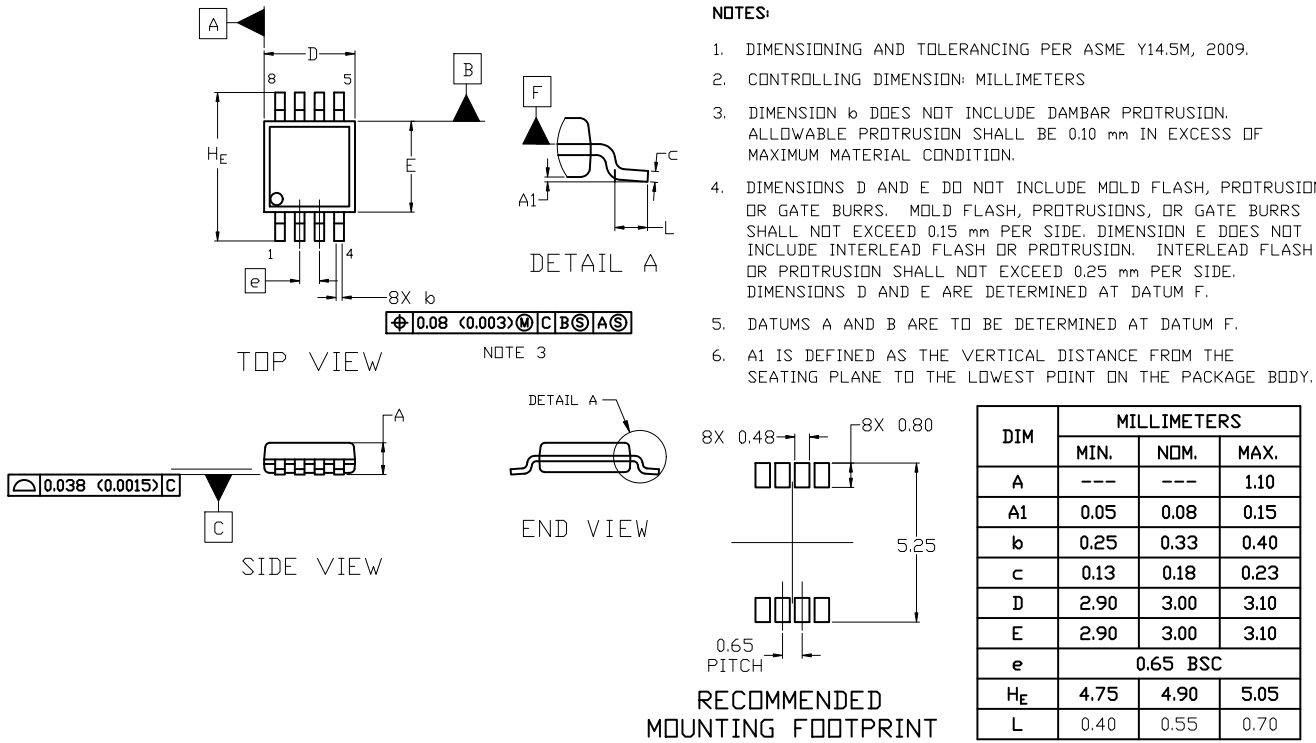
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# 7WBD383

## PACKAGE DIMENSIONS

### Micro8 CASE 846A ISSUE K



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

■ For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, [SOLDSM047A](#).

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