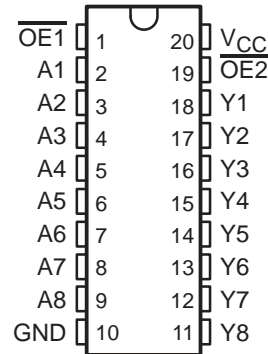


CD74FCT541 BiCMOS OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCBS741 – JULY 2000

- BiCMOS Technology With Low Quiescent Power
- Buffered Inputs
- Noninverted Outputs
- Input/Output Isolation From V_{CC}
- Controlled Output Edge Rates
- 64-mA Output Sink Current
- Output Voltage Swing Limited to 3.7 V
- SCR Latch-Up-Resistant BiCMOS Process and Circuit Design
- Package Options Include Plastic Small-Outline (M) and Shrink Small-Outline (SM) Packages and Standard Plastic (E) DIP

E, M, OR SM PACKAGE
(TOP VIEW)



description

The CD74FCT541 is an octal buffer/driver with 3-state outputs that is ideal for driving bus lines or buffer memory address registers and uses a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output high level to two diode drops below V_{CC} . This resultant lowering of output swing (0 V to 3.7 V) reduces power-bus ringing [a source of electromagnetic interference (EMI)] and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 mA.

The 3-state control gate is a two-input AND gate with active-low inputs, so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The CD74FCT541 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each buffer/driver)

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z



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**TEXAS
INSTRUMENTS**

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recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4.75	5.25	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current		-15	mA
I _{OL}	Low-level output current		64	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	0	70	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
V _{IK}	I _I = -18 mA	4.75 V		-1.2		-1.2	V
V _{OH}	I _{OH} = -15 mA	4.75 V	2.4		2.4		V
V _{OL}	I _{OL} = 64 mA	4.75 V		0.55		0.55	V
I _I	V _I = V _{CC} or GND	5.25 V		±0.1		±1	μA
I _{OZ}	V _O = V _{CC} or GND	5.25 V		±0.5		±10	μA
I _{OS} [†]	V _I = V _{CC} or GND, V _O = 0	5.25 V		-60		-60	mA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.25 V		8		80	μA
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at V _{CC} or GND	5.25 V		1.6		1.6	mA
C _i	V _I = V _{CC} or GND			10		10	pF
C _o	V _O = V _{CC} or GND			15		15	pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 100 ms.

[‡] This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating conditions, V_{CC} = 5 V ± 0.25 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C	MIN	MAX	UNIT
			TYP			
t _{pd}	A	Y	6	2	8	ns
t _{en}	\overline{OE}	Y	7.5	2	10	ns
t _{dis}	\overline{OE}	Y	7.1	2	9.5	ns

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C

PARAMETER	MIN	TYP	MAX	UNIT
V _{OL(P)} Quiet output, maximum dynamic V _{OL}		1		V
V _{OH(V)} Quiet output, minimum dynamic V _{OH}		0.5		V
V _{IH(D)} High-level dynamic input voltage	2			V
V _{IL(D)} Low-level dynamic input voltage			0.8	V

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BiCMOS OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS

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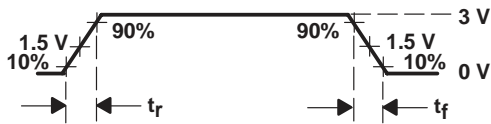
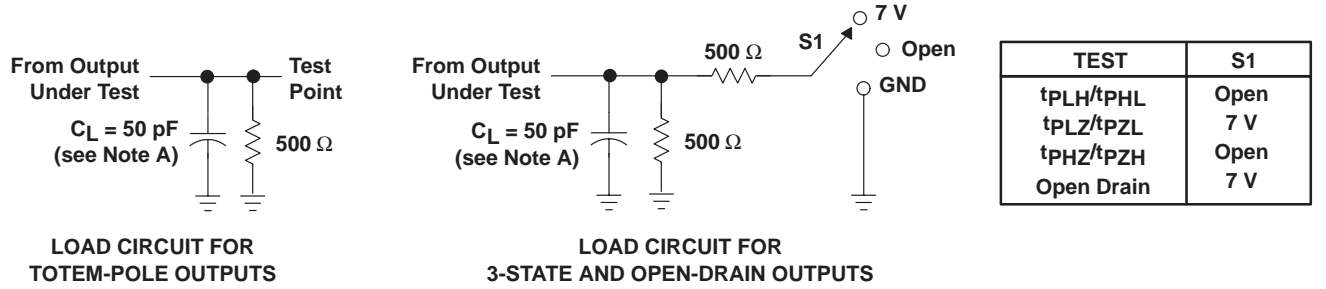
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	40	pF

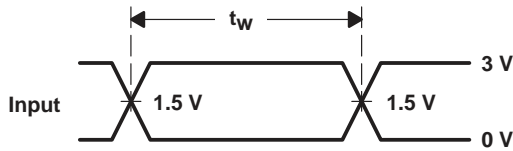


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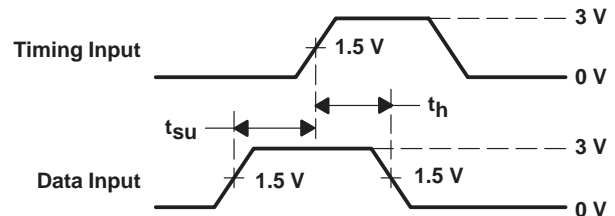
PARAMETER MEASUREMENT INFORMATION



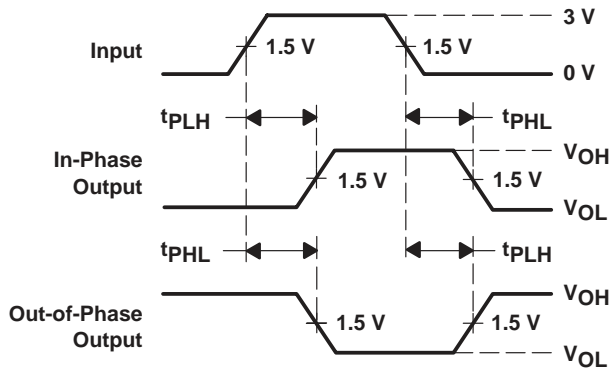
VOLTAGE WAVEFORM
 INPUT RISE AND FALL TIMES



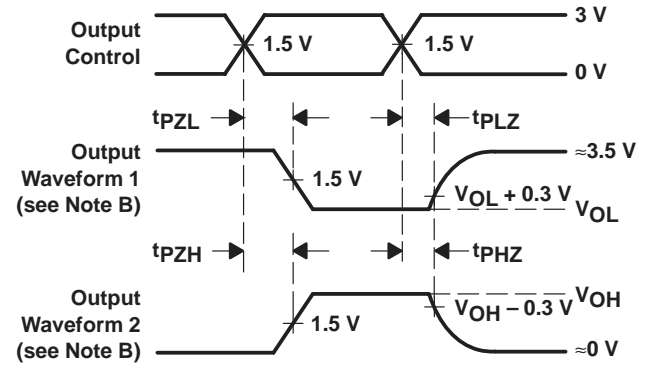
VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r and t_f = 2.5 ns.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. t_{PZL} and t_{PHZ} are the same as t_{dis}.
 F. t_{PZL} and t_{PZH} are the same as t_{en}.
 G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74FCT541E	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	CD74FCT541E	Samples
CD74FCT541M	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74FCT541M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74FCT541E	N	PDIP	20	20	506	13.97	11230	4.32
CD74FCT541M	DW	SOIC	20	25	507	12.83	5080	6.6

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



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NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

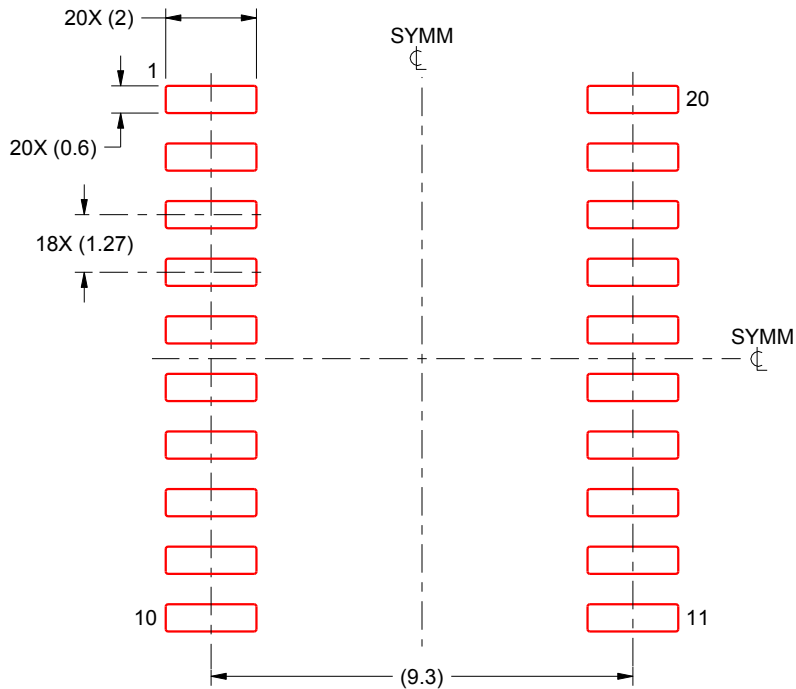
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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