FastEdge™ Series
CY2PP326

2 x 2 Clock and Data Switch Buffer

Features

- **Six ECL/PECL differential outputs**
- **Two ECL/PECL differential inputs**
- **Hot-swappable/-insertable**
- **50 ps output-to-output skew**
- **250 ps device-to-device skew**
- **950 ps propagation delay (typical)**
- **1.2 GHz Operation**
- **2.8 ps RMS period jitter (max.)**
- **PECL mode supply range: V_{EE} = –2.5V± 5% to –3.3V±5% with V_{EE} = 0V**
- **ECL mode supply range: V_{CC} = 2.5V± 5% to 3.3V±5% with V_{EE} = 0V**
- **Industrial temperature range: –40°C to 85°C**
- **32-pin 1.4mm TQFP package**
- **Temperature compensation like 100K ECL**
- **Pin Compatible with MC100ES6254**

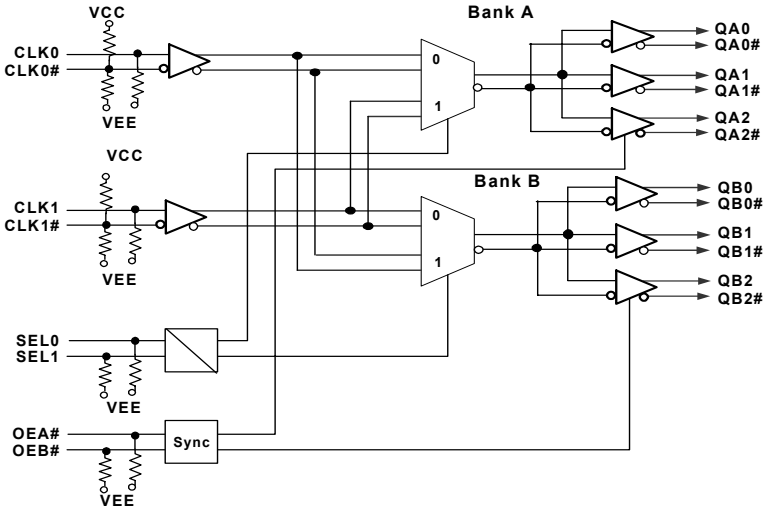
Functional Description

The CY2PP326 is a low-skew, low propagation delay 2 x 2 differential clock, data switch, and fanout buffer targeted to meet the requirements of high-performance clock and data distribution applications. The device is implemented on SiGe technology and has a fully differential internal architecture that is optimized to achieve low-signal skews at operating frequencies of up to 1.5 GHz.

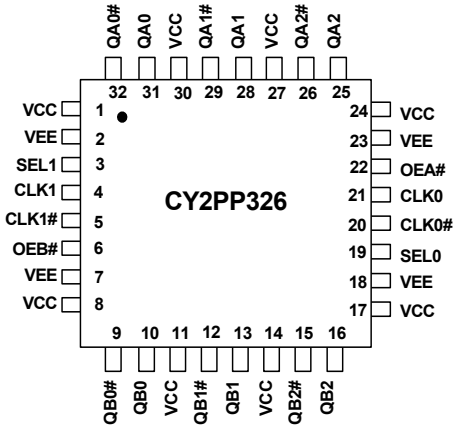
The device features two differential input paths which are multiplexed internally to six outputs grouped in two banks. The muxes are controlled by SEL(0:1) control inputs. The CY2PP326 may function as 1:6 or 2x 1:3 clock/data buffer and as a clock/data repeater or multiplexer.

Since the CY2PP326 introduces negligible jitter to the timing budget, it is the ideal choice for distributing high frequency, high precision clocks across back-planes and boards in communication systems and for switching data signals between different channels. Furthermore, advanced circuit design schemes, such as internal temperature compensation, ensure that the CY2PP326 delivers consistent, guaranteed performance over differing platforms.

Block Diagram



Pin Configuration



Pin Definitions

Pin	Name	I/O[1]	Type[2]	Description
19,3	SEL0,SEL1	I	LVCMOS	**Clock/Data Switch Select**.
22,6	OEA#,OEB#	I	LVCMOS	**Output Enable**.
21,4	CLK(0:1)	I,PD	ECL/PECL	**True Differential Inputs**.
20,5	CLK(0:1)#	I,PD/PU	ECL/PECL	**Complement Differential Inputs**.
31,28,25 32,29,26	QA(0:2) QA(0:2)#	O	ECL/PECL	**Differential Outputs – Bank A**.
10,13,16 9,12,15	QB(0:2) QB(0:2)#	O	ECL/PECL	**Differential Outputs – Bank B**.
2,7,18,23,	VEE	–PWR	GND	**Negative Power Supply**.
1,8,11,14,17,24,27,30	VCC	+PWR	POWER	**Positive Power Supply**.

Table 1. Function Table

Control	Default	0	1
OAE#	0	QA(0–2), QX(0–2)# are active. Deassertion of OE# can be asynchronous to the reference clock without generation of output runt pulses.	QA(0–2)= L, QX(0–2)# = H. Assertion of OE# can be asynchronous to the reference clock without generation of output runt pulses.
OEB#	0	QA(0–2), QX(0–2)are active. Deassertion of OE# can be asynchronous to the reference clock without generation of output runt pulses.	QA(0–2)= L, QX(0–2)# = H. Assertion of OE# can be asynchronous to the reference clock without generation of output runt pulses.
SEL0,SEL1	00	See *Table 2*	

Table 2. Clock Select Control

SEL0	SEL1	CLK0 Routed to	CLK1 Routed to	Application Mode
0	0	QA(0:2) and QB(0:2)	–	1:6 fanout of CLK0
0	1	–	QA(0:2) and QB(0:2)	1:6 fanout of CLK1
1	0	QA(0:2)	QB(0:2)	Dual 1:3 buffer
1	1	QB(0:2)	QA(0:2)	Dual 1:3 buffer crossed

Governing Agencies

The following agencies provide specifications that apply to the CY2PP326. The agency name and relevant specification is listed below in *Table 3*.

Table 3.

Agency Name	Specification
JEDEC	JESD 020B (MSL) JESD 51 (Theta JA) JESD 8–2 (ECL) JESD 65–B (skew,jitter)
Mil-Spec	883E Method 1012.1 (Thermal Theta JC)

Notes:
1. In the I/O column, the following notation is used: I for Input, O for Output, PD for Pull-Down, PU for Pull-Up, and PWR for Power
2. In ECL mode (negative power supply mode), V_{EE} is either –3.3V or –2.5V and V_{CC} is connected to GND (0V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0V) and V_{CC} is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply (V_{CC}) and are between V_{CC} and V_{EE}.

Absolute Maximum Ratings

Parameter	Description	Condition	Min.	Max.	Unit
V_{CC}	Positive Supply Voltage	Non-Functional	–0.3	4.6	V
V_{EE}	Negative Supply Voltage	Non-Functional	-4.6	0.3	V
T_S	Temperature, Storage	Non-Functional	–65	+150	°C
T_J	Temperature, Junction	Non-Functional		150	°C
ESD_h	ESD Protection	Human Body Model	2000		V
M_{SL}	Moisture Sensitivity Level		3		N.A.
Gate Count	Total Number of Used Gates	Assembled Die	50		gates

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Operating Conditions

Parameter	Description	Condition	Min.	Max.	Unit
LU_I	Latch Up Immunity	Functional, typical	100		mA
T_A	Temperature, Operating Ambient	Functional	–40	+85	°C
$Ø_{Jc}$	Dissipation, Junction to Case	Functional	29[3]		°C/W
$Ø_{Ja}$	Dissipation, Junction to Ambient	Functional	75[3]		°C/W
I_{EE}	Maximum Quiescent Supply Current	V_{EE} pin		130 [4]	mA
C_{IN}	Input pin capacitance			3	pF
L_{IN}	Pin Inductance			1	nH
V_{IN}	Input Voltage	Relative to V_{CC}[5]	–0.3	V_{CC} + 0.3	V
V_{TT}	Output Termination Voltage	Relative to V_{CC}[5]	V_{CC} – 2		V
V_{OUT}	Output Voltage	Relative to V_{CC}[5]	–0.3	V_{CC} + 0.3	V
I_{IN}	Input Current[6]	$V_{IN} = V_{IL}$, or $V_{IN} = V_{IH}$		I150I	uA

PECL DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V_{CC}	Operating Voltage	2.5V ± 5%, V_{EE} = 0.0V 3.3V ± 5%, V_{EE} = 0.0V	2.375 3.135	2.625 3.465	V V
V_{CMR}	Differential Cross Point Voltage[7]	Differential operation	1.2	V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = –30 mA[8]	V_{CC} – 1.25	V_{CC} – 0.7	V
V_{OL}	Output Low Voltage V_{CC} = 3.3V ± 5% V_{CC} = 2.5V ± 5%	I_{OL} = –5 mA[8]	 V_{CC} – 1.995 V_{CC} –1.995	 V_{CC} – 1.5 V_{CC} – 1.3	 V V
V_{IH}	Input Voltage, High	Single-ended operation	V_{CC} – 1.165	V_{CC} – 0.880 [9]	V
V_{IL}	Input Voltage, Low	Single-ended operation	V_{CC} – 1.945 [9]	V_{CC} – 1.625	V

Notes:
3. Theta JA EIA JEDEC 51 test board conditions (typical value); Theta JC 883E Method 1012.1
4. Power Calculation: $V_{CC} * I_{EE} + 0.5 (I_{OH} + I_{OL}) (V_{OH} – V_{OL})$ (number of differential outputs used); I_{EE} does not include current going off chip.
5. where V_{CC} is 3.3V±5% or 2.5V±5%
6. Inputs have internal pull-up/pull-down or biasing resistors which affect the input current.
7. Refer to Figure 1
8. Equivalent to a termination of 50Ω to VTT. $I_{OHMIN}=(V_{OHMIN}-V_{TT})/50$; $I_{OHMAX}=(V_{OHMAX}-V_{TT})/50$; $I_{OLMIN}=(V_{OLMIN}-V_{TT})/50$; $I_{OLMAX}=(V_{OLMAX}-V_{TT})/50$;
9. V_{IL} will operate down to V_{EE}; V_{IH} will operate up to V_{CC}

ECL DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V_{EE}	Negative Power Supply	–2.5V ± 5%, V_{CC} = 0.0V –3.3V ± 5%, V_{CC} = 0.0V	–2.625 –3.465	–2.375 –3.135	V
V_{CMR}	Differential cross point voltage[7]	Differential operation	V_{EE} + 1.2	0V	V
V_{OH}	Output High Voltage	I_{OH} = –30 mA[8]	–1.25	–0.7	V
V_{OL}	Output Low Voltage V_{EE} = –3.3V ± 5% V_{EE} = –2.5V ± 5%	I_{OL} = –5 mA[8]	 –1.995 –1.995	 –1.5 –1.3	V
V_{IH}	Input Voltage, High	Single-ended operation	–1.165	–0.880 [9]	V
V_{IL}	Input Voltage, Low	Single-ended operation	–1.945 [9]	–1.625	V

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V_{PP}	Differential Input Voltage[7]	Differential operation	0.1	1.3	V
F_{CLK}	Input Frequency	50% duty cycle Standard load	–	1.5	GHz
T_{PD}	Propagation Delay CLKA or CLKB to Output pair	< 1 GHz [10]	–	1200	ps
Vo	Output Voltage (peak-to-peak; see Figure 2)	< 1 GHz	0.375	–	V
V_{CMRO}	Output Common Voltage Range (typ.)		V_{CC} – 1.425		V
$tsk_{(0)}$	Output-to-output Skew	660 MHz [10], See Figure 3	–	50	ps
$tsk_{(PP)}$	Part-to-Part Output Skew	660 MHz [10]	–	250	ps
T_{PER}	Output Period Jitter (rms)[11]	660 MHz [10]	–	2.8	ps
$tsk_{(P)}$	Output Pulse Skew[12]	660 MHz [10], See Figure 3	–	75	ps
T_R,T_F	Output Rise/Fall Time (see Figure 2)	660 MHz 50% duty cycle Differential 20% to 80%	0.08	0.3	ns
t_{PDL}	Output disable time	T = CLK period	2.5T + T_{PD}	3.5T + T_{PD}	ns
t_{PLD}	Output enable time	T = CLK period	3.0T + T_{PD}	4.0T + T_{PD}	ns

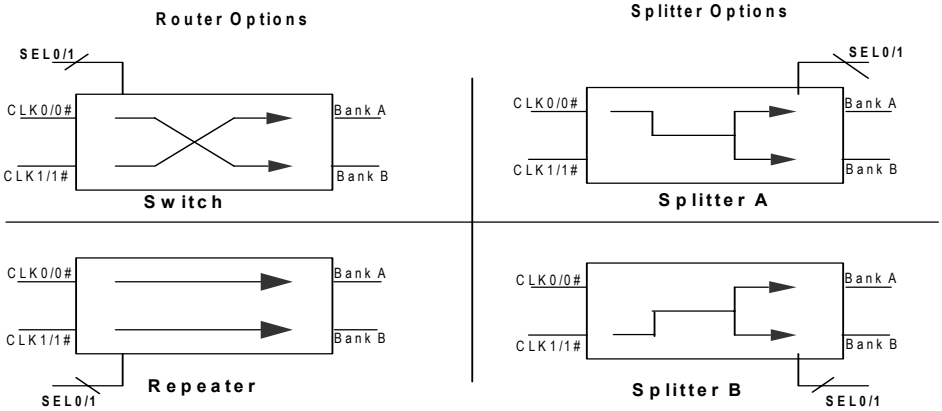


Figure 1. Channel Cross Point Switch/Mux Configurations

Notes:
10. 50% duty cycle; standard load; differential operation
11. For 3.3V supplies. Jitter measured differentially using an Agilent 8133A Pulse Generator with an 8500A LeCroy Wavemaster Oscilloscope using at least 10,000 data points
12. Output pulse skew is the absolute difference of the propagation delay times: $| t_{PLH} – t_{PHL} |$.

Timing Definitions

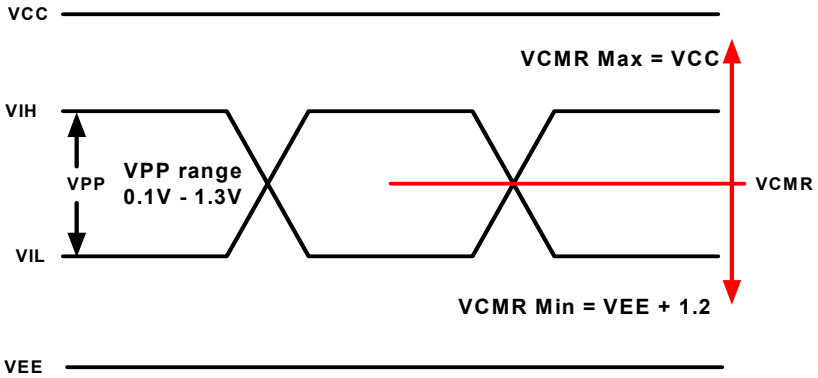


Figure 2. PECL/ECL Input Waveform Definitions

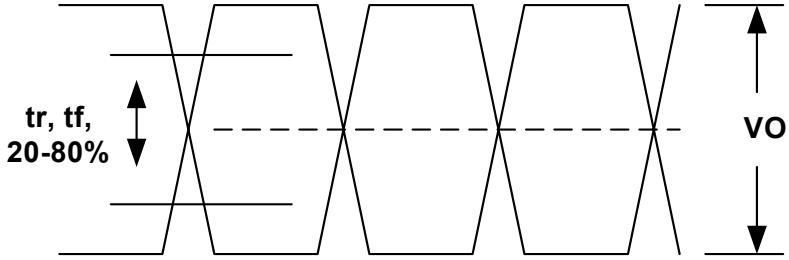


Figure 3. ECL/LVPECL Output

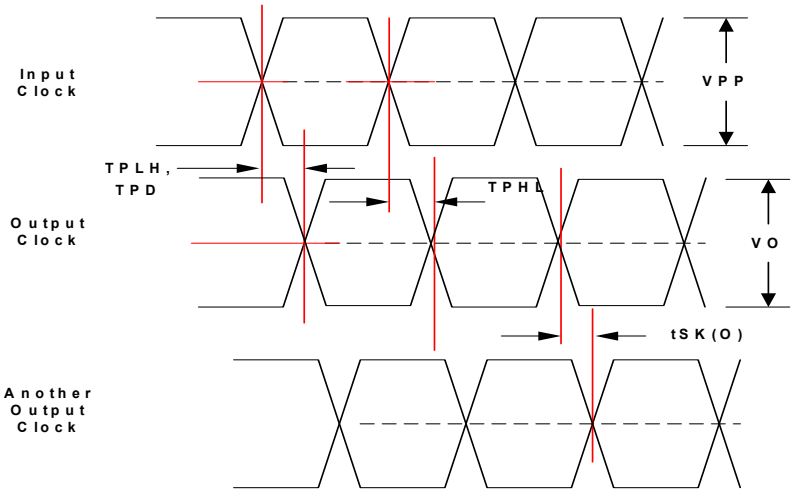


Figure 4. Propagation Delay (T_{PD}), output pulse skew ($|t_{PLH}-t_{PHL}|$), and output-to-output skew ($t_{SK(O)}$) for both CLKA or CLKB to Output Pair, PECL/ECL to PECL/ECL

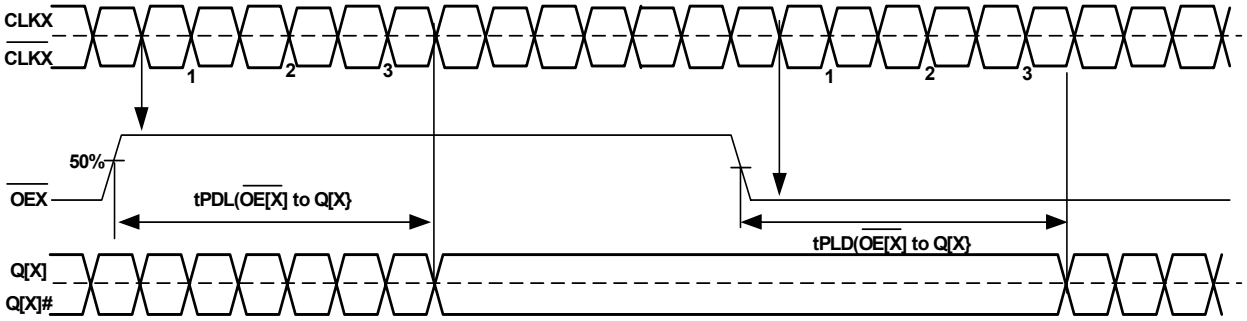


Figure 5. Output Disable/Enable Timing

Test Configuration

Standard test load using a differential pulse generator and differential measurement instrument.

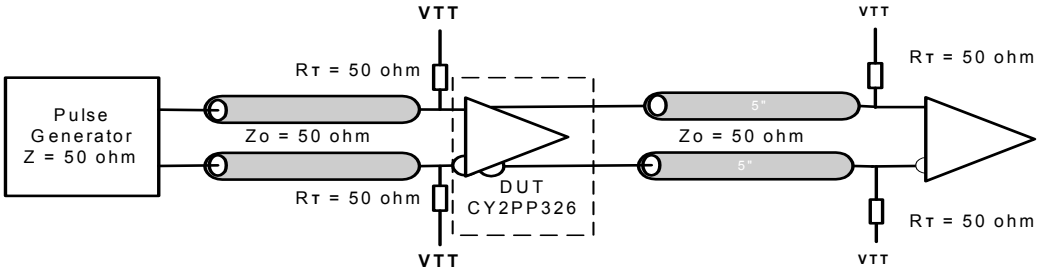


Figure 6. CY2PP326 AC Test Reference

Applications Information

Termination Examples

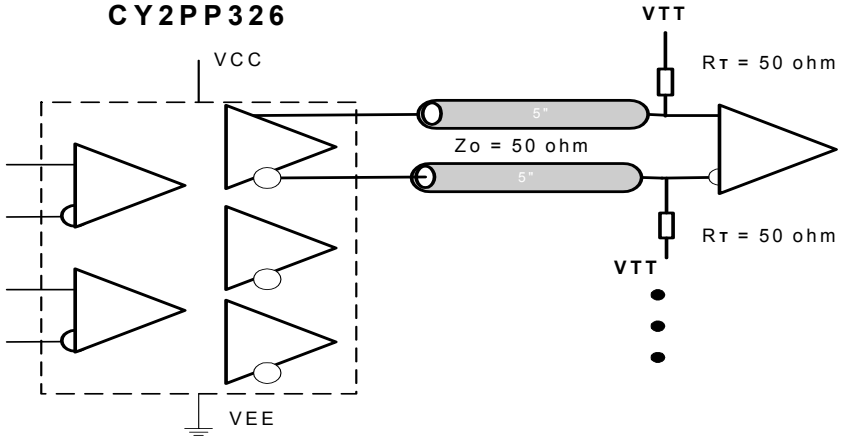


Figure 7. Standard LVPECL – PECL Output Termination

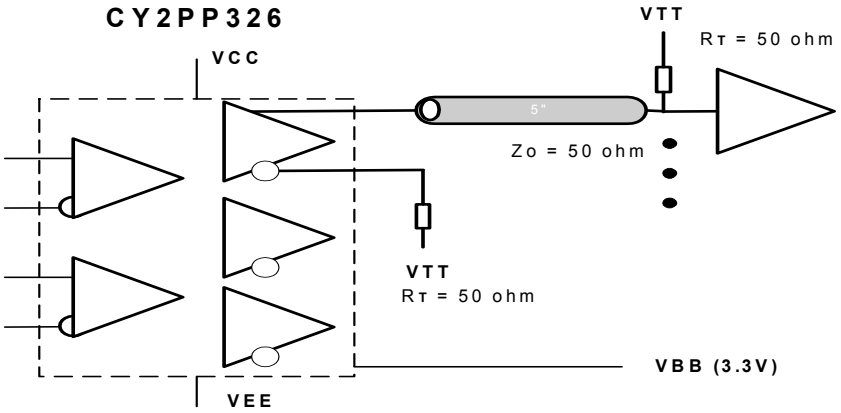


Figure 8. Driving a PECL/ECL Single-ended Input

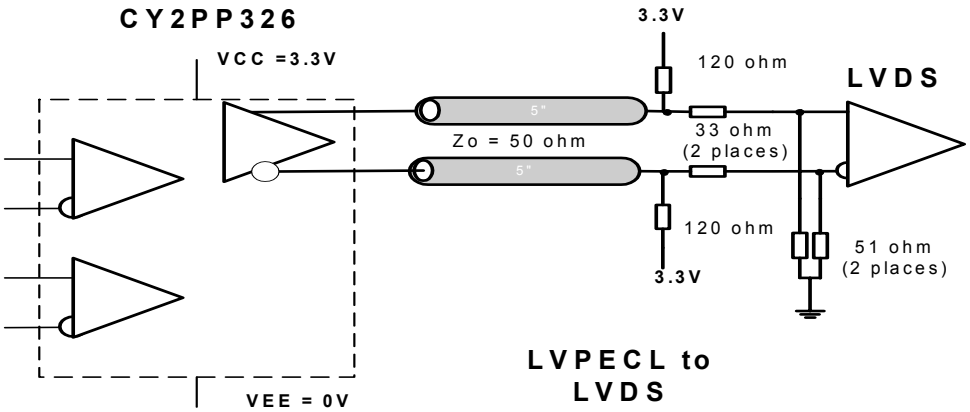
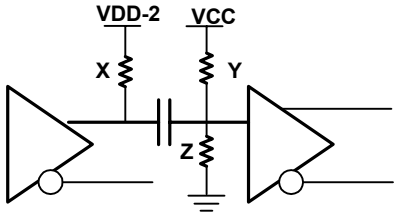


Figure 9. Low-voltage Positive Emitter-coupled Logic (LVPECL) to a Low-voltage Differential Signaling (LVDS) Interface



One output is shown for clarity

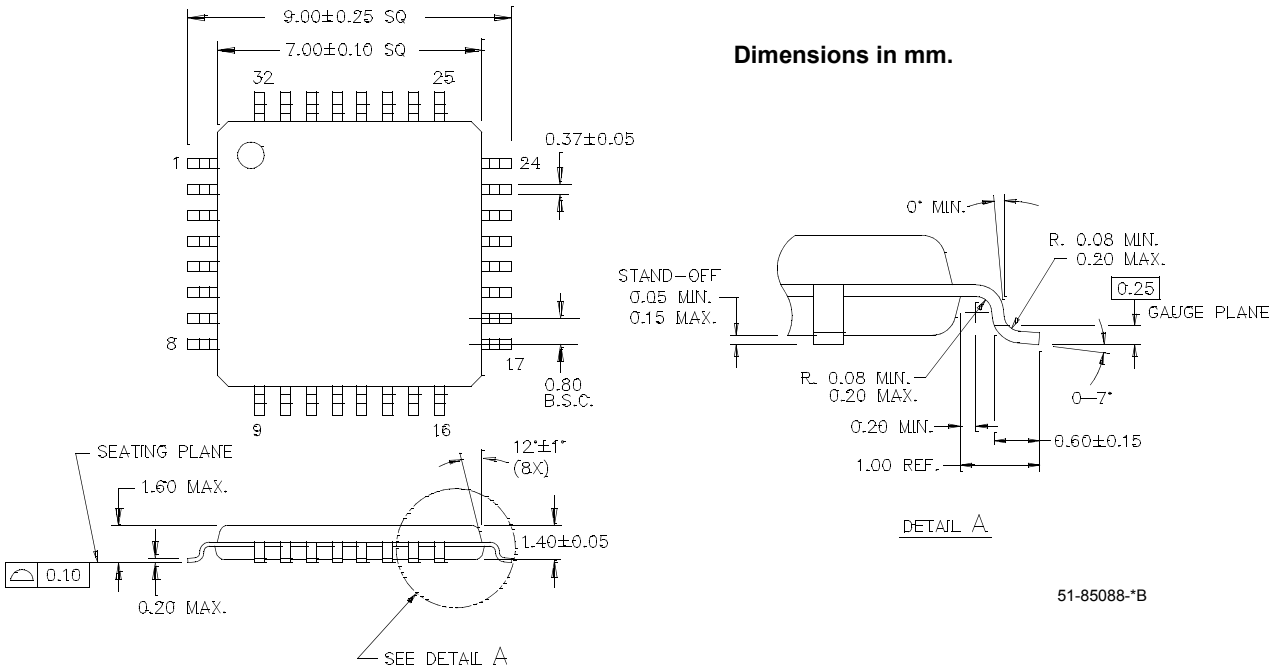
Figure 10. Termination for LVPECL to HTSL interface for VCC=2.5V would use X=50 Ohms, Y=2300 Ohms, and Z=1000 Ohms. See application note titled, "PECL Translation, SAW Oscillators, and Specs" for other signalling standards and supplies.

Ordering Information

Part Number	Package Type	Product Flow
CY2PP326AI	32-pin TQFP	Industrial, –40° to 85°C
CY2PP326AIT	32-pin TQFP – Tape and Reel	Industrial, –40° to 85°C

Package Drawing and Dimensions

32-lead Thin Plastic Quad Flatpack 7 x 7 x 1.4 mm A32.14



Dimensions in mm.

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Document History Page

Document Title: CY2PP326 FastEdge™ Series 2 x 2 Clock and Data Switch Buffer Document Number: 38-07506				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	122361	02/12/03	RGL	New Data Sheet
*A	129269	09/09/03	RGL	Changed ComLink™ to FastEdge™ Added t_{PLDg} and t_{PDLf} specs in the AC specs table Added the Output disable/enabling timing diagram Deleted the output reference voltage in the absolute max. conditions Fixed the AC/DC Electrical specs to match the EROS
*B	131346	11/20/03	RGL	Posted to external web
*C	237751	See ECN	RGL	Supplied data to all TBD's to match the device.
*D	247620	See ECN	RGL/GGK	Changed V_{OH} and V_{OL} to match the Char Data