

Automotive PSoC™ 4 MCU: PSoC™ 4700S Plus

General description

Automotive PSoC™ 4 MCU is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an Arm® Cortex®-M0+ CPU while being AEC-Q100 compliant. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The PSoC™ 4700S Plus product family, based on this platform, is the industry's first microcontroller with oscillator based inductive sensing and capacitive sensing technology in a single chip. The inductive sensing technology enables sensing of metal objects and industry's leading capacitive sensing (CAPSENSE™) technology enables sensing of non-metallic objects.

Features

- Automotive Electronics Council (AEC) AEC-Q100 qualified
- 32-bit MCU subsystem
 - 48-MHz Arm® Cortex®-M0+ CPU
 - Up to 128 KB of flash with read accelerator
 - Up to 8 KB of SRAM
 - 8-channel DMA engine
- Programmable analog
 - Two opamps with reconfigurable high-drive external and high-bandwidth internal drive and comparator modes and ADC input buffering capability. Opamps can operate in deep sleep low-power mode.
 - 12-bit 1-Msps SAR ADC with differential and single-ended modes, and channel sequencer with signal averaging
 - Single-slope 10-bit ADC function provided by a capacitance sensing block
 - Two current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
 - Two low-power comparators that operate in deep sleep low-power mode
- Programmable digital
 - Three smart IO ports (19 smart IO pins) allowing boolean operations to be performed on port inputs and outputs
- Low-power 1.71 V to 5.5 V operation
 - Deep sleep mode with operational analog and 2.5 µA digital system current
- Oscillator based inductive sensing
 - Infineon inductive sensing provides superior noise immunity
 - Can reliably detect metal deflection under 190 nm
 - Inductive sense software component automatically calibrates the solution to compensate for the manufacturing variations
 - Supports up to four sensors
- Capacitive sensing
 - Infineon CAPSENSE™ sigma-delta (CSD) provides best-in-class signal-to-noise ratio (SNR) (> 5:1) and water tolerance
 - Infineon-supplied software component makes capacitive sensing design easy
 - Automatic hardware tuning (SmartSense)
- LCD drive capability
 - LCD segment drive capability on GPIOs
- Serial communication
 - Five independent run-time reconfigurable Serial Communication Blocks (SCBs) with re-configurable I²C, SPI, UART functionality, or LIN slave functionality

Features

- Timing and Pulse-Width Modulation
 - Eight 16-bit Timer/Counter/Pulse-Width Modulator (TCPWM) blocks
 - Center-aligned, edge, and pseudo-random modes
 - Comparator-based triggering of kill signals for motor drive and other high-reliability digital logic applications
 - Quadrature decoder
- Clock sources
 - 4 to 33 MHz External Crystal Oscillator (ECO)
 - PLL to generate 48-MHz frequency
 - 32-kHz Watch Crystal Oscillator (WCO)
 - $\pm 2\%$ Internal Main Oscillator (IMO)
 - 32-kHz Internal Low-Power Oscillator (ILO)
- True random number generator (TRNG)
 - TRNG generates truly random number for secure key generation for cryptography applications
- Temperature range
 - Grade-S: -40°C to $+105^{\circ}\text{C}$
- Up to 34 programmable GPIO pins (19 of these can be configured as smart IO)
 - 40-pin QFN package
 - Any GPIO pin can be CAPSENSE™, analog, or digital
 - Drive modes, strengths, and slew rates are programmable
- ModusToolbox™ software enables cross platform code development with a robust suite of tools and software libraries
- Industry-standard tool compatibility
 - After schematic entry, development can be done with Arm®-based industry-standard development tools

More information

More information

Infineon provides a wealth of data at www.infineon.com to help you to select the right PSoC™ MCU device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [How to design with PSoC™ 3, PSoC™ 4, and PSoC™ 5LP - KBA86521](#). Following is an abbreviated list for PSoC™ 4 MCU:

- Application notes: Infineon offers a large number of PSoC™ device application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC™ 4 MCU are:
 - [AN79953](#): Getting started with PSoC™ 4
 - [AN86439](#): Using PSoC™ 4 GPIO pins
 - [AN57821](#): Mixed signal circuit board layout
 - [AN81623](#): Digital design best practices
 - [AN73854](#): Introduction to bootloaders
 - [AN89610](#): Arm® Cortex® code optimization
 - [AN85951](#): PSoC™ 4 and PSoC™ 6 MCU CAPSENSE™ design guide
- Online:
 - In addition to print documentation, the [PSoC™ forums](#) connect you with fellow PSoC™ MCU users and experts in PSoC™ MCU from around the world, 24 hours a day, 7 days a week.

ModusToolbox™ software

ModusToolbox™ software

ModusToolbox™ software is Infineon comprehensive collection of multi-platform tools and software libraries that enable an immersive development experience for creating converged MCU and wireless systems. It is:

- Comprehensive - it has the resources you need
- Flexible - you can use the resources in your own workflow
- Atomic - you can get just the resources you want

Infineon provides a large collection of code [repositories on GitHub](#). This includes:

- Board support packages (BSPs) aligned with Infineon kits
- Low-level resources, including a hardware abstraction layer (HAL) and peripheral driver library (PDL)
- Middleware enabling industry-leading features such as CAPSENSE™, Bluetooth® Low Energy, and mesh networks
- An extensive set of thoroughly tested [code example applications](#)

Note: The HAL provides a high-level, simplified interface to configure and use the hardware blocks on Infineon MCUs. It is a generic interface that can be used across multiple product families. For example, it wraps the PSoC™ 4 MCU PDL with a simplified API, but the PDL exposes all low-level peripheral functionality. You can leverage the HAL's simpler and more generic interface for most of an application, even if one portion requires finer-grained control.

ModusToolbox™ software is IDE-neutral and easily adaptable to your workflow and preferred development environment. It includes a project creator, peripheral and library configurators, a library manager, as well as the optional eclipse IDE for ModusToolbox™ software, as [Figure 1](#) shows.

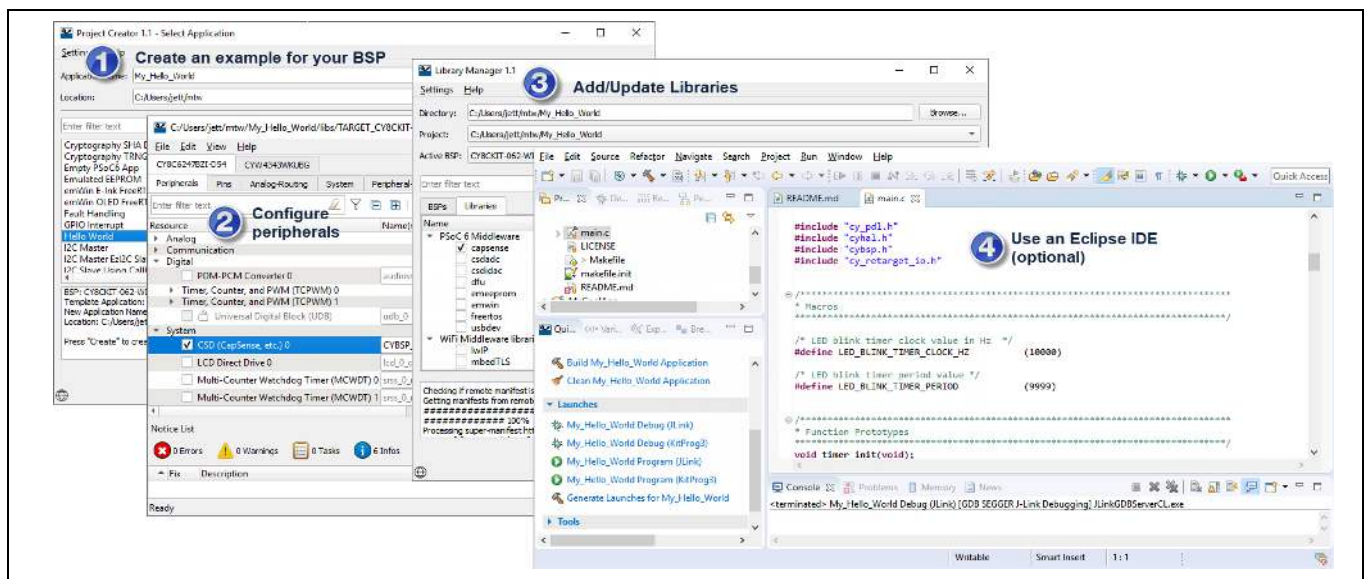


Figure 1 ModusToolbox™ software tools

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Block diagram

Block diagram

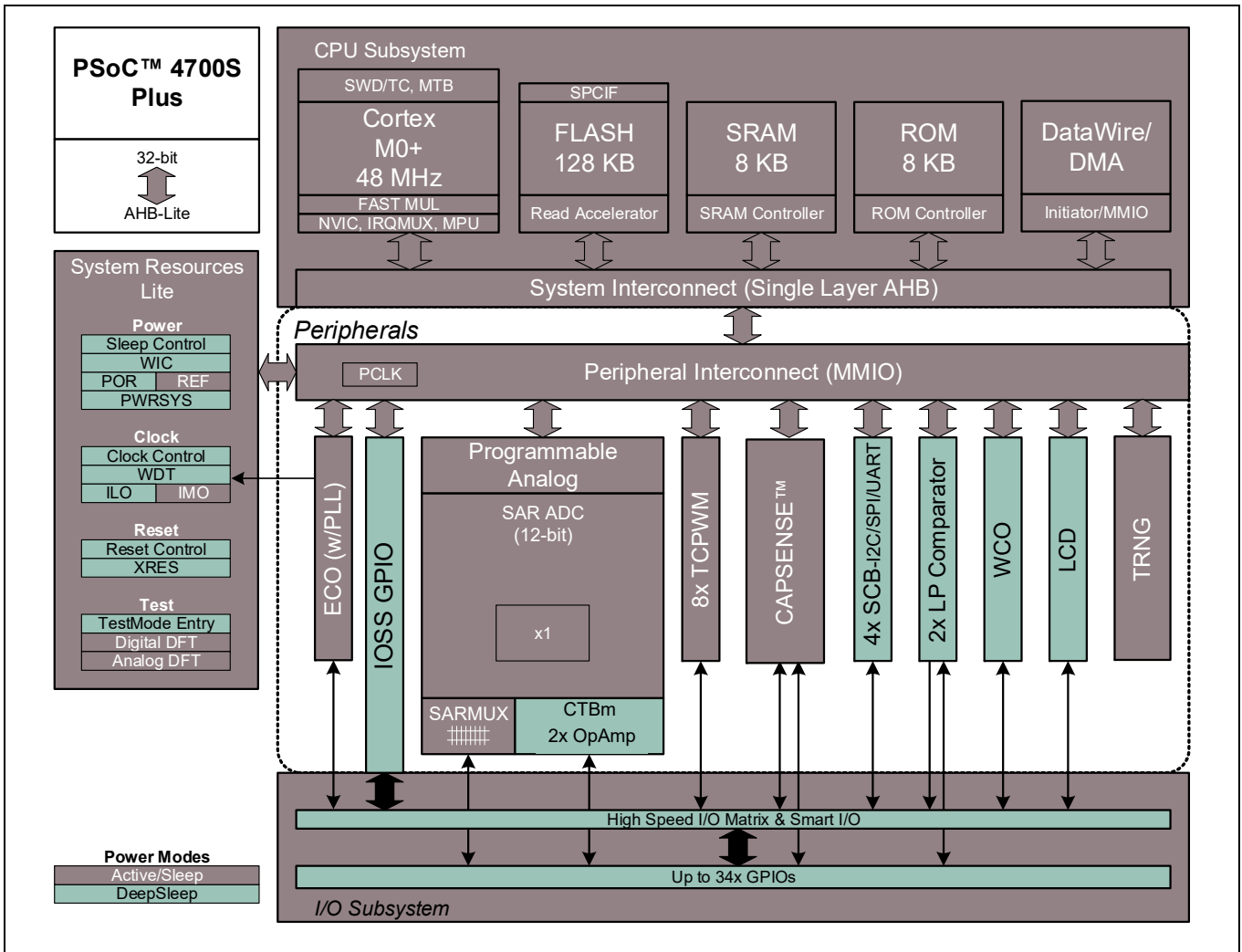


Figure 2 Block diagram

1 Functional description

PSoC™ 4700S Plus devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm® serial-wire debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The SWD interface is fully compatible with industry-standard third-party tools. PSoC™ 4700S Plus provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC™ 4700S Plus, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC™ 4700S Plus allows the customer to make.

2 Functional definition

2.1 CPU and memory subsystem

2.1.1 CPU

The Cortex®-M0+ CPU in the PSoC™ 4700S Plus is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a wakeup interrupt controller (WIC). The WIC can wake the processor from deep sleep mode, allowing power to be switched off to the main processor when the chip is in deep sleep mode. The CPU subsystem includes an 8-channel DMA engine and also includes a debug interface, the SWD interface, which is a 2-wire form of JTAG. The debug configuration used for PSoC™ 4700S Plus has four breakpoint (address) comparators and two watchpoint (data) comparators.

2.1.2 Flash

The PSoC™ 4700S Plus device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

2.1.3 SRAM

8 KB of SRAM are provided with zero wait-state access at 48 MHz.

2.1.4 SRAM

An 8-KB supervisory ROM that contains boot and configuration routines is provided.

2.2 System resources

2.2.1 Power system

The power system is described in detail in the section **“Power”** on page 26. It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brownout detection). PSoC™ 4700S Plus operates with a single external supply over the range of either 1.8 V ± 5% (externally regulated) or 1.8 V to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. PSoC™ 4700S Plus provides active, sleep, and deep sleep low-power modes.

All subsystems are operational in active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 μs. The opamps can remain operational in deep sleep mode.

2.2.2 Clock system

The PSoC™ 4700S Plus clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC™ 4700S Plus consists of the IMO, ILO, a 32-kHz watch crystal oscillator (WCO), 4 to 33 MHz ECO and PLL, and provision for an external clock. The WCO block allows locking the IMO to the 32-kHz oscillator.

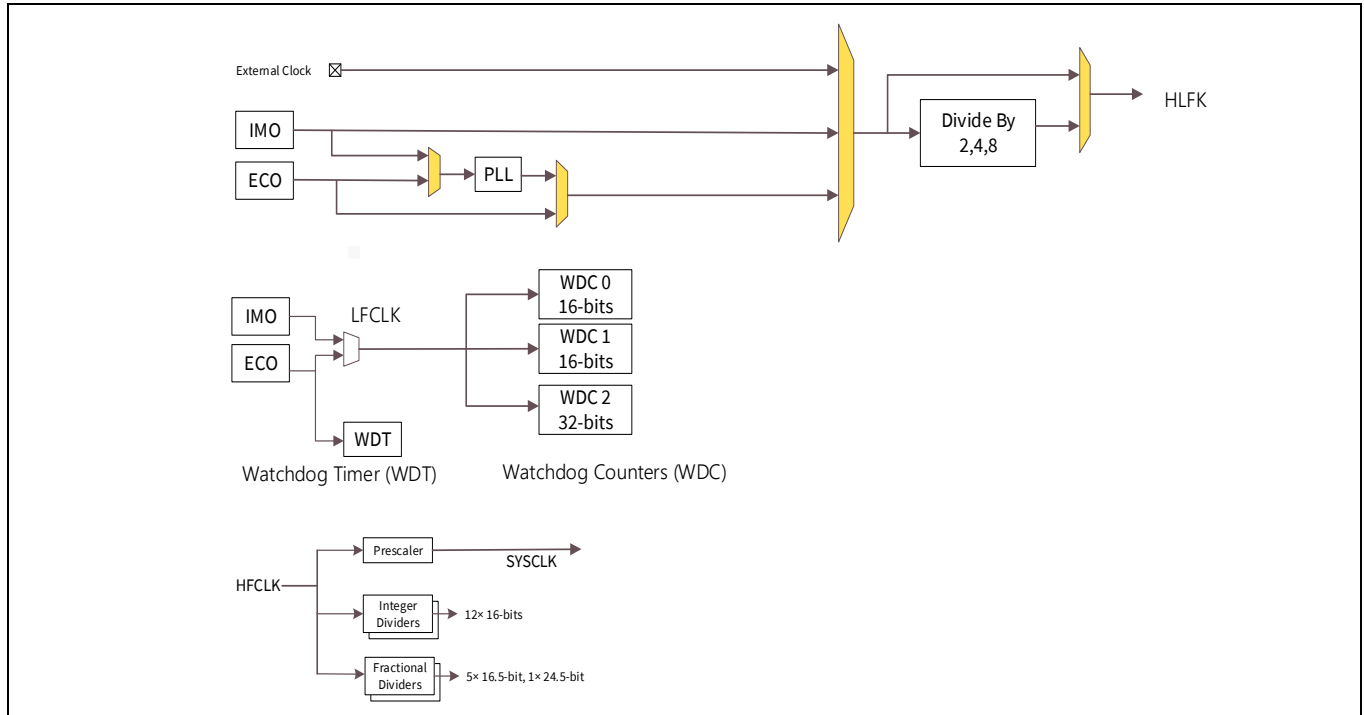


Figure 3 PSoC™ 4700S Plus MCU clocking architecture

The HFCLK signal can be divided down as shown to generate synchronous clocks for the analog and digital peripherals. There are 18 clock dividers for the PSoC™ 4700S Plus (six with fractional divide capability, twelve with integer divide only). The twelve 16-bit integer divide capability allows a lot of flexibility in generating fine-grained frequency. In addition, there are five 16-bit fractional dividers and one 24-bit fractional divider.

2.2.3 IMO clock source

The IMO is the primary source of internal clocking in the PSoC™ 4700S Plus. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Infineon-provided calibration settings is $\pm 2\%$ over the entire voltage and temperature range.

2.2.4 ILO clock source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in deep sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Infineon provides a software component, which does the calibration.

2.2.5 WCO

The PSoC™ 4700S Plus clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

Functional definition

2.2.6 ECO

The PSoC™ 4700S Plus also implements a 4 to 33 MHz crystal oscillator.

2.2.7 WDT

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during deep sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a reset cause register, which is firmware readable.

2.2.8 Reset

PSoC™ 4700S Plus can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

2.3 Analog blocks

2.3.1 12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The sample-and-hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is not available in deep sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

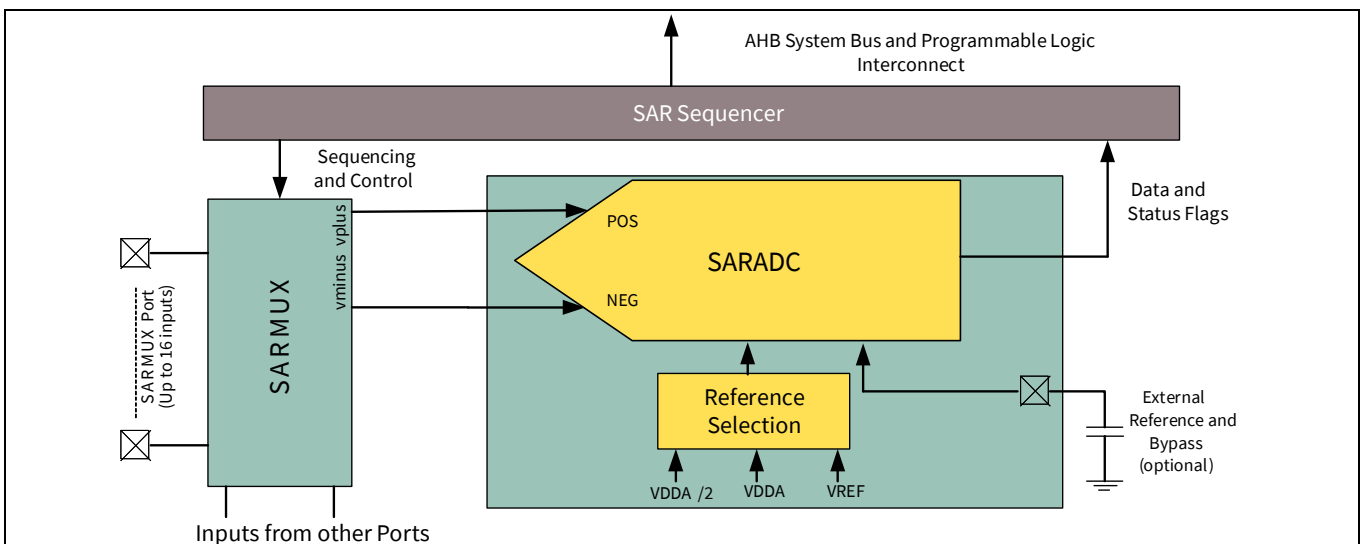


Figure 4 SAR ADC

2.3.2 Two opamps (continuous-time block; CTB)

PSoC™ 4700S Plus has two opamps with comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, voltage buffers, filters, trans-impedance amplifiers, and other functions can be realized, in some cases with external passives. saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the sample-and-hold circuit of the ADC without requiring external buffering.

2.3.3 Low-power comparators (LPC)

PSoC™ 4700S Plus has a pair of low-power comparators, which can also operate in deep sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

2.3.4 Current DACs

PSoC™ 4700S Plus has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

2.3.5 Analog multiplexed buses

PSoC™ 4700S Plus has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O ports.

2.4 Programmable digital blocks

2.4.1 Smart I/O block

The smart I/O block is a fabric of switches and LUTs that allows boolean functions to be performed in signals being routed to the pins of a GPIO port. The smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

2.5 Fixed function digital blocks

2.5.1 Timer/counter/PWM (TCPWM) block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. Each block also incorporates a quadrature decoder. There are eight TCPWM blocks in PSoC™ 4700S Plus.

2.5.2 Serial communication block (SCB)

PSoC™ 4700S Plus has five serial communication blocks (SCBs), which can be programmed to have SPI, I²C, UART, or LIN slave functionality.

I²C mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 1 Mbps (fast mode plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI²C that creates a mailbox address range in the memory of PSoC™ 4700S Plus and effectively reduces I²C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I²C peripheral is compatible with the I²C standard-mode and fast-mode plus devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

PSoC™ 4700S Plus is not completely compliant with the I²C spec in the following respect:

- GPIO cells are not over-voltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I²C system.

UART mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI mode: The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

LIN slave mode: The LIN slave mode uses the SCB hardware block and implements a full LIN slave interface. This LIN slave is compliant with LIN v1.3, v2.1/2.2, ISO 17987-6, and SAE J2602-2 specification standards. It is certified by C&S GmbH based on the standard protocol and data link layer conformance tests. LIN slave can be operated at baud rates of up to ~20 Kbps with a maximum of 40-meter cable length.

2.6 GPIO

PSoC™ 4700S Plus has up to 33 GPIOs. The GPIO block implements the following:

- Eight drive modes:
 - Analog input mode (input and output buffers disabled)
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disabled state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

2.7 Special function peripherals

2.7.1 CAPSENSE™

CAPSENSE™ is supported in the PSoC™ 4700S Plus through a CAPSENSE™ sigma-delta (CSD) block that can be connected to any pins through an analog multiplex bus via analog switches. CAPSENSE™ function can thus be provided on any available pin or group of pins in a system under software control. A PSoC™ Creator IDE component is provided for the CAPSENSE™ block to make it easy for the user.

Shield voltage can be driven on another analog multiplex bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CAPSENSE™ block has two IDACs, which can be used for general purposes if CAPSENSE™ is not being used (both IDACs are available in that case) or if CAPSENSE™ is used without water tolerance (one IDAC is available).

The CAPSENSE™ block also provides a 10-bit Slope ADC function which can be used in conjunction with the CAPSENSE™ function.

The CAPSENSE™ block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and ground to null out power-supply related noise.

2.7.2 LCD segment drive

PSoC™ 4700S Plus has an LCD controller, which can drive up to 4 commons and up to 50 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM. Digital correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during deep sleep refreshing a small display buffer (4 bits; one 32-bit register per port).

2.8 Inductive sensing

The PSoC™ 4700S Plus devices support a low-cost and robust Oscillator based inductive sensing, which integrates seamlessly with existing user interfaces and is used to detect the presence of metallic or conductive objects. The Oscillator based inductive sensing provides best-in-class signal-to-noise ratio (SNR), Higher operating frequency, better sensitivity and Parallel scanning.

The inductive sensing can be used for applications such as buttons (touch-over-metal), metal proximity detection and measurement, rotary and linear encoders, spring-based position detection, and other applications for detecting position or distance of the metal objects.

Oscillator based inductive sense block:

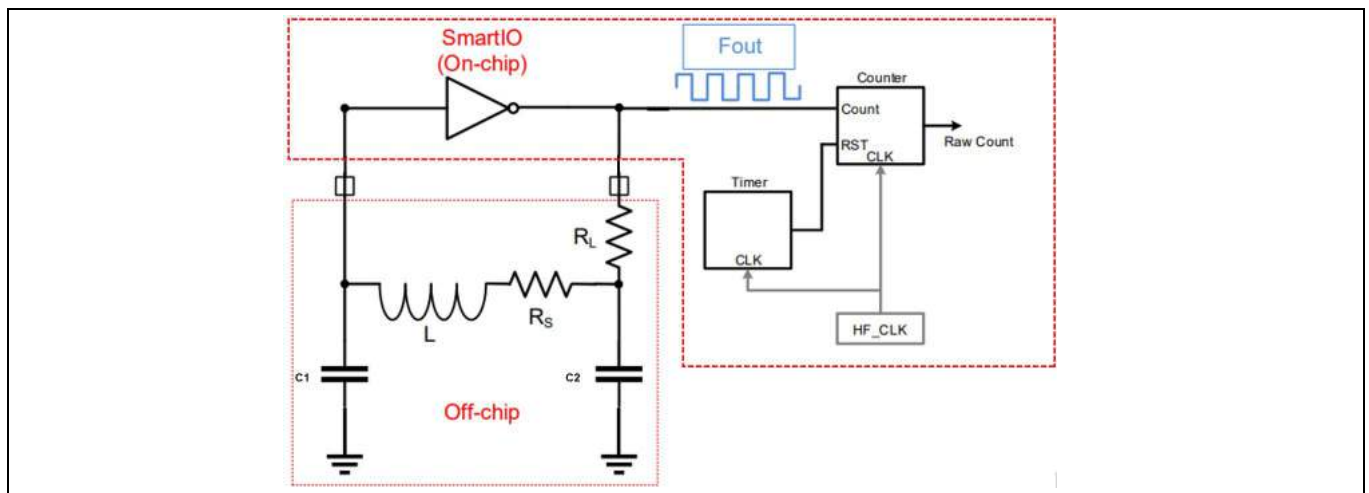


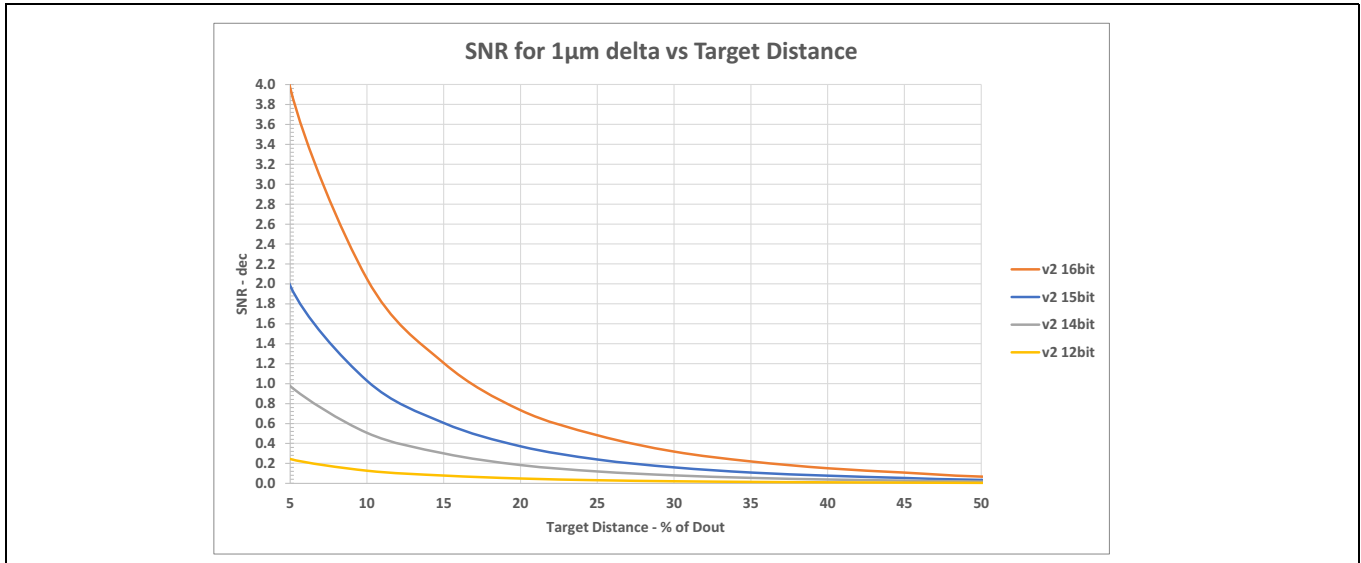
Figure 5 Oscillator based Inductive Sensing Architecture

As shown in the above **Figure 5**, off-chip components such as L_1 (PCB coil), C_1 , C_2 , R_S and R_L needs to be connected to GPIO pins and configure SmartIO block with inverter logic. This combination forms an oscillator whose output frequency (F_{OUT}) is modulated by the inductance changes of the PCB coil, caused by a metal target. Internal timer and counter blocks convert the variations of F_{OUT} into the digital domain.

Oscillator based inductive sense has the following features:

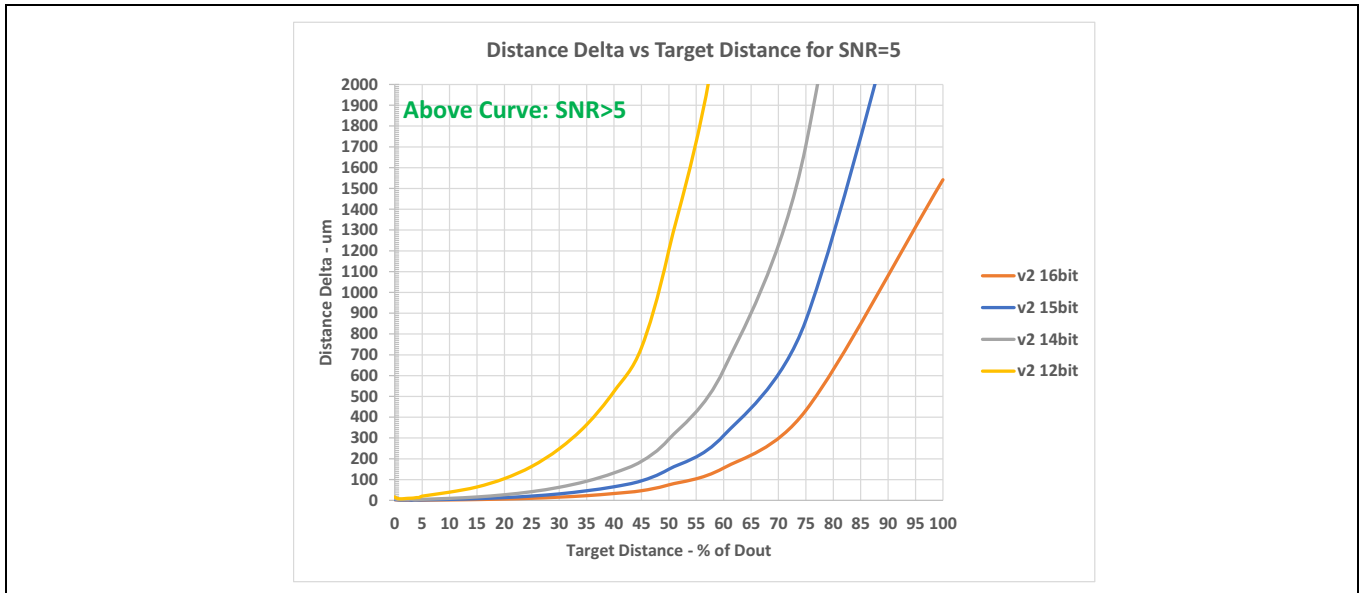
- Supports Inductive sensing for frequencies from 1 MHz to 12 MHz.
- Oscillator runs at high frequency reducing coil dimensions, current and scan.
- Lower temperature drift than other sensing methods
- High sensitivity, low noise, resulting in greater SNR
- Sensing distance up to 1.5 times the diameter of the coil (SNR = 5, 2 layers coil)
- Parallel scanning

2.8.1 SNR vs target distance



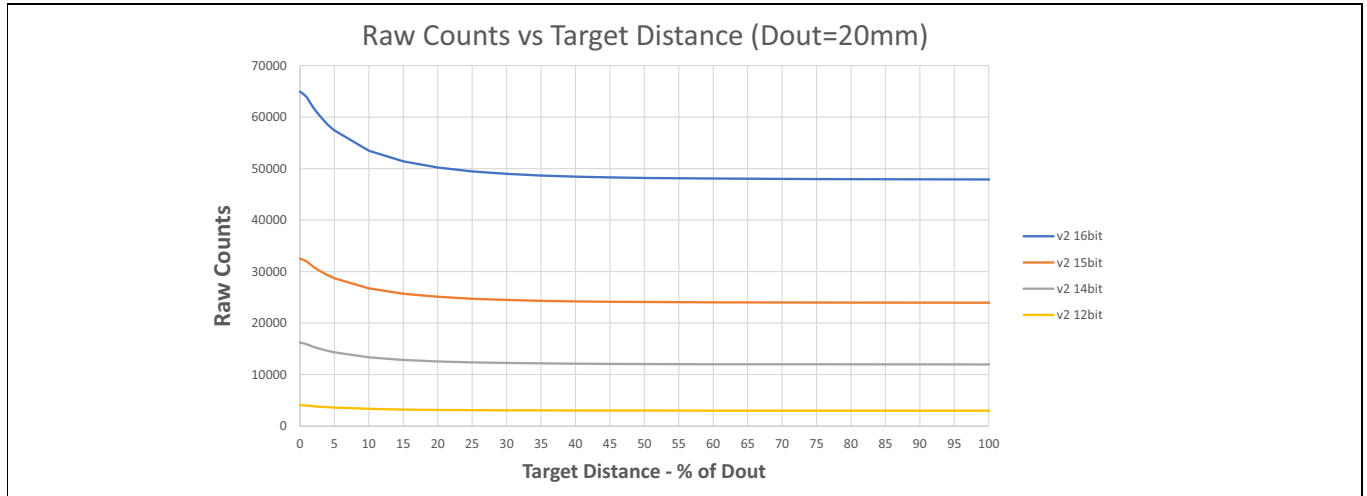
This graph shows the signal-to-noise ratio versus metal target position. In this case, the signal corresponds to the raw counts delta provoked by a metal target displacement of 1 µm. The y-axis of the graph is scalable for displacements different than 1 µm. For example, to obtain the SNR for a 10-µm displacement, the corresponding y-axis SNR value must be multiplied by 10.

2.8.2 Distance delta (metal target displacement) when SNR = 5



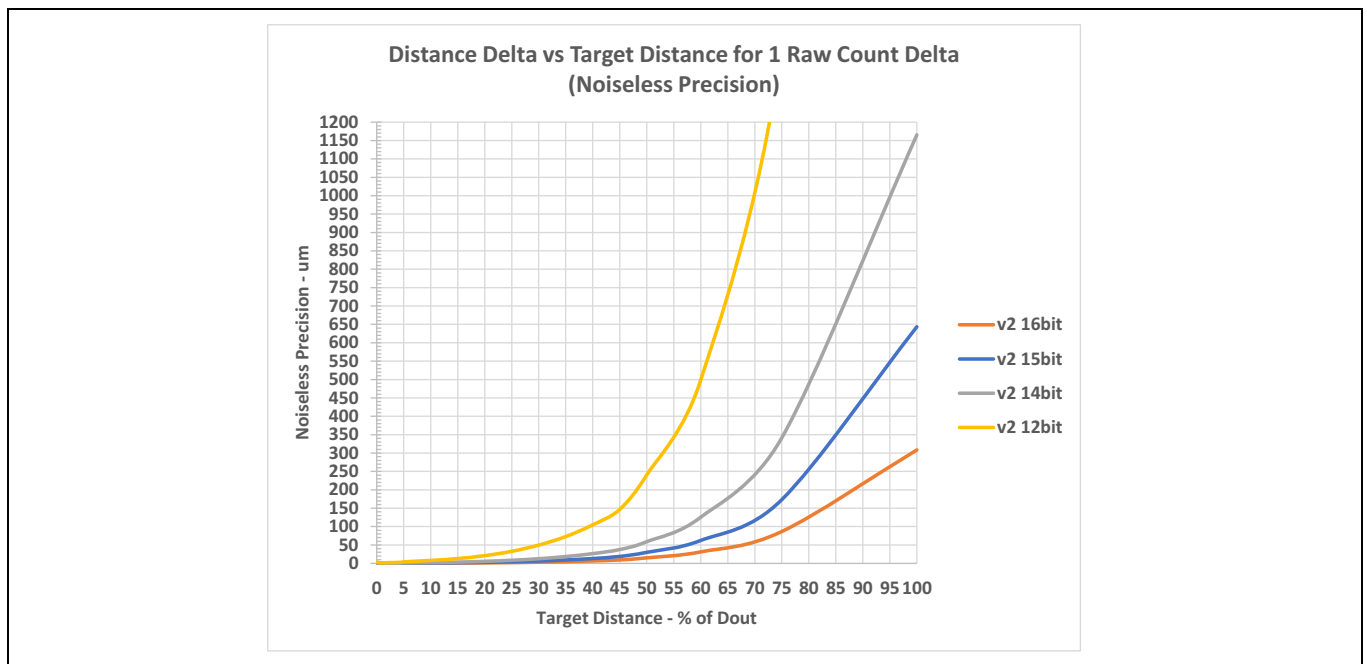
Each curve in this graph determines the metal target displacement needed to achieve a SNR value of 5. Therefore, above the curve, SNR > 5, and below the curve SNR < 5. For example, if we have a metal target positioned at a distance equivalent to 50% of the coil’s diameter (Dout), we need a minimum target displacement of approximately 75 µm @ 16 bits, 150 µm @ 15 bits, and 300 µm @ 14 bits to obtain an SNR ≥ 5.

2.8.3 Raw counts vs target distance



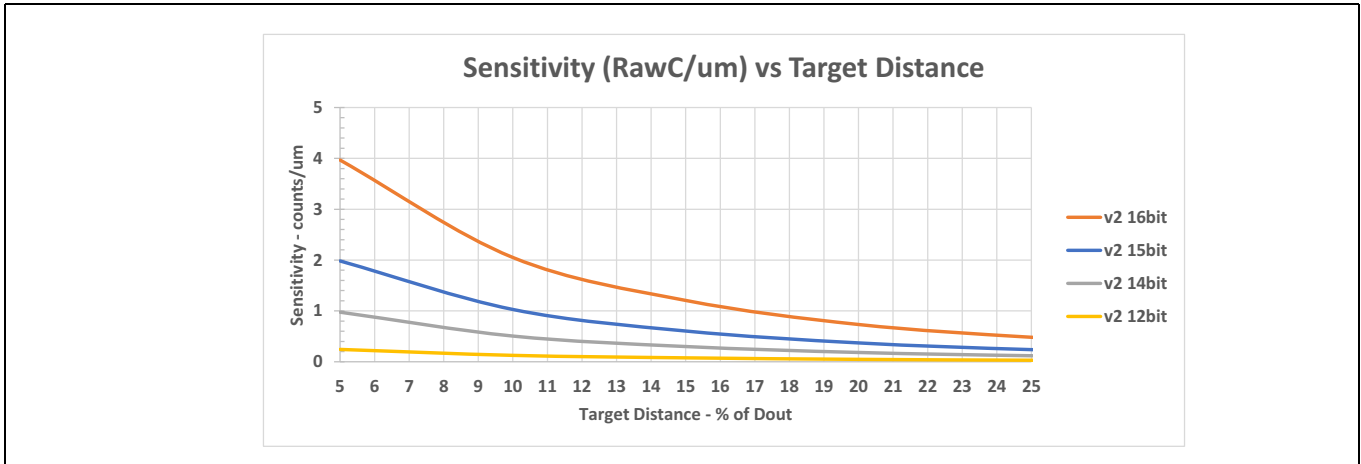
This graph plots the unfiltered converted data (raw counts) versus the metal target distance for different scan resolutions (bits).

2.8.4 Noiseless precision



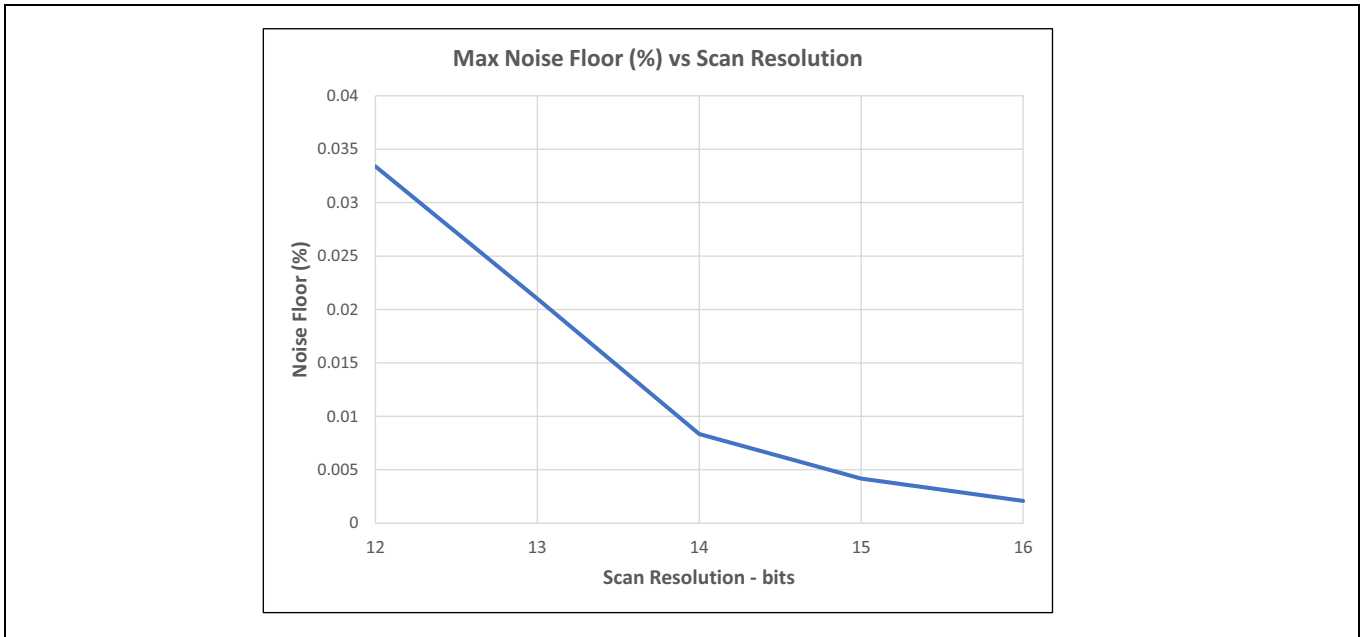
This graph shows the metal target displacement that can be detected in the absence of noise. In this ideal scenario, the plotted target displacement results in one raw count delta.

2.8.5 Sensitivity



This graph shows the sensitivity of the system in raw counts per μm versus the target distance.

2.8.6 Noise floor (%)



Noise floor is the ratio between the peak-to-peak raw counts noise and the averaged (or DC) raw counts (1000 samples).

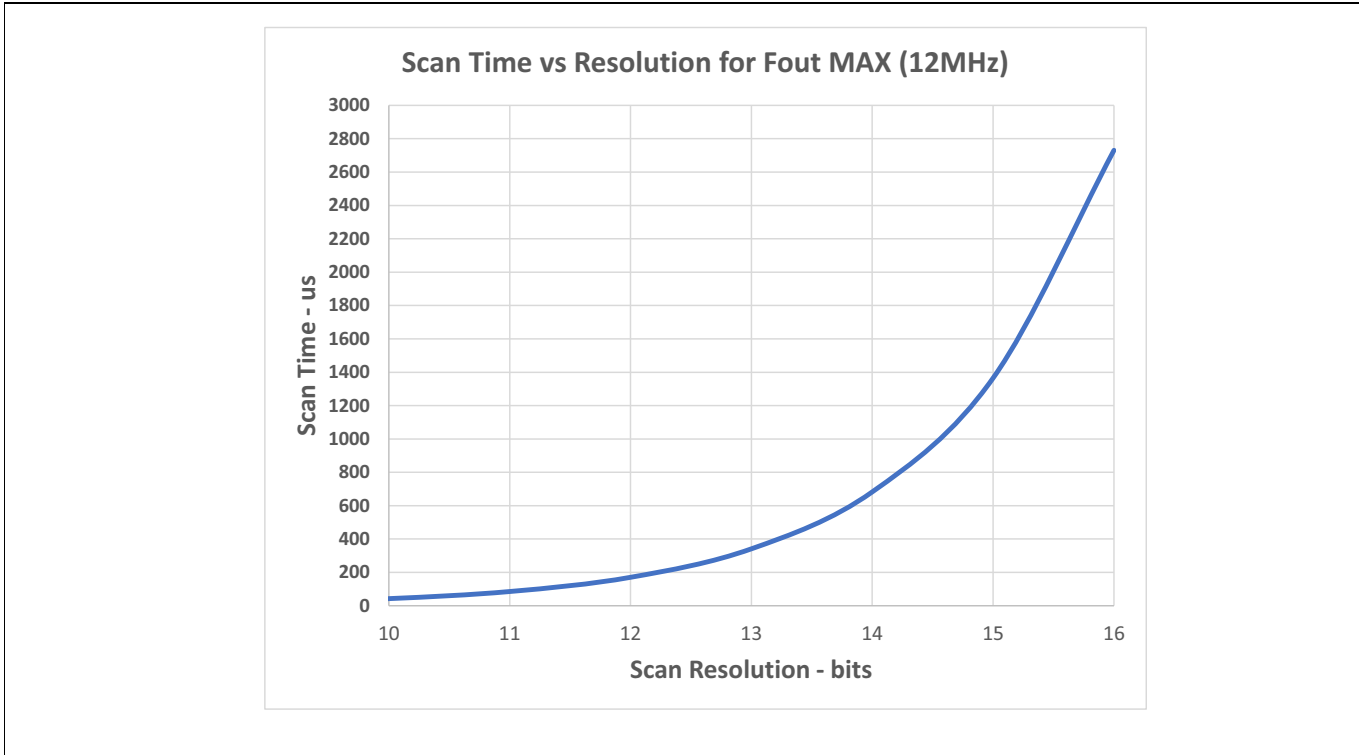
Functional definition

2.8.7 Effective number of bits (ENOB)

ENOB is the actual resolution of the system when intrinsic noise is considered. For example, a 16-bit scan has an ENOB = 15 bits, and therefore has the same resolution of a noiseless 15-bit scan.

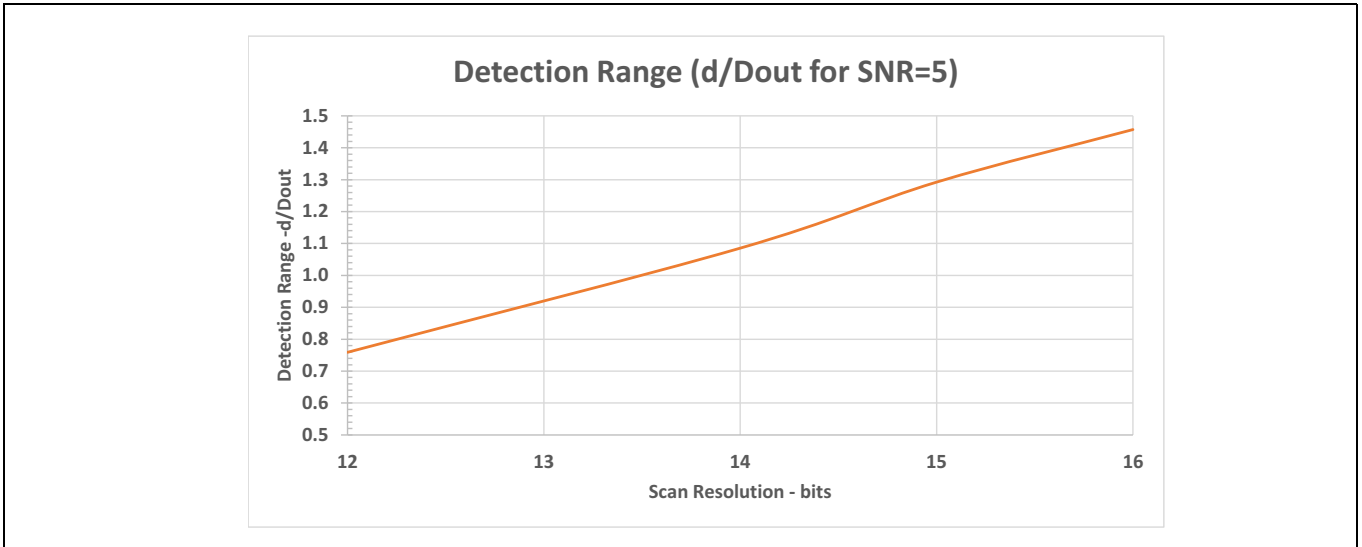
Resolution (% of Dout)	Target distance (mm)	ENOB (bits)
5	1	12.997
10	2	12.858
20	4	12.786
40	8	12.738
60	12	12.525
100	20	11.057

2.8.8 Scan time



The plot in this graph shows an example of Fmax = 12 MHz; hence it shows the minimum scan time per sensor at different scan resolutions.

2.8.9 Detection range



This graph shows the maximum distance until which a metal target can be detected with a SNR value of 5. When a metal target that was initially far away (i.e. > 2x D_{out}) is moved in closer, the raw counts begin to increase. The point at which these raw counts increase is 5 times the peak-to-peak noise (SNR = 5) and that marks the detection range. The measured peak-to-peak noise is the noise at the initial distance, $d > 2x D_{out}$.

3 Pinouts

Table 1 Pin list for PSoC™ 4700S Plus for the 40-pin QFN package

Pin	Name
22	P0.0
23	P0.1
24	P0.2
25	P0.3
26	P0.4
27	P0.5
28	P0.6
29	P0.7
30	XRES
31	VCCD
32	VSSD
33	VDD
34	VSSA
35	P1.0
36	P1.1
37	P1.2
38	P1.3
39	P1.4
40	P1.7/VREF
1	P2.3
2	P2.4
3	P2.5
4	P2.6
5	P2.7
6	P6.0
7	P6.1
8	P6.2
9	VSSD
10	P3.0
11	P3.1
12	P3.2
13	P3.3
14	P3.4
15	P3.5
16	P3.6
17	P3.7
18	P4.0

Pinouts

Table 1 Pin list for PSoC™ 4700S Plus for the 40-pin QFN package (continued)

Pin	Name
19	P4.1
20	P4.2
21	P4.3

Descriptions of the power pins are as follows:

VDDD: Power supply for the digital section.

VDDA: Power supply for the analog section.

VSSD, VSSA: Ground pins for the digital and analog sections respectively.

VCCD: Regulated digital supply (1.8 V ± 5%)

VDD: On some packages, VDDA and VDDD are shorted inside and brought out as a single power supply

GPIOs: 34

3.1 Alternate pin functions

Each port pin has can be assigned to one of multiple functions; it can, for example, be an analog I/O, a digital peripheral function, an LCD pin, or a Smart IO pin. The pin assignments are shown in the following table.

Table 2 Pin assignments

Pin	Name	Analog	Smart I/O	Alternate function 1	Alternate function 2	Alternate function 3	Alternate function 4	Deep Sleep 1	Deep Sleep 2	Deep Sleep 3	Deep Sleep 4
22	P0.0	lpcomp.in_p[0]	-	-	tcpwm.tr_in[0]	pass.dsi_sar_data_valid	scb[2].uart_cts:0	lcd.com[0]	lcd.seg[0]	scb[2].i2c_scl:0	scb[0].spi_select1:0
23	P0.1	lpcomp.in_n[0]	-	-	tcpwm.tr_in[1]	pass.tr_sar_out	scb[2].uart_rts:0	lcd.com[1]	lcd.seg[1]	scb[2].i2c_sda:0	scb[0].spi_select2:0
24	P0.2	lpcomp.in_p[1]	-	-	-	pass.dsi_sar_sample_done	-	lcd.com[2]	lcd.seg[2]	-	scb[0].spi_select3:0
25	P0.3	lpcomp.in_n[1]	-	-	-	pass.dsi_sar_data[2]	-	lcd.com[3]:0	lcd.seg[3]	-	scb[2].spi_select0:1
26	P0.4	wco.wco_in	-	-	scb[1].uart_rx:0	pass.dsi_sar_data[0]	scb[2].uart_rx:0	lcd.com[4]	lcd.seg[4]	scb[1].i2c_scl:0	scb[1].spi_mosi:1
27	P0.5	wco.wco_out	-	-	scb[1].uart_tx:0	pass.dsi_sar_data[1]	scb[2].uart_tx:0	lcd.com[5]	lcd.seg[5]	scb[1].i2c_sda:0	scb[1].spi_miso:1
28	P0.6	srss.adft_por_pad_hv_exco.eco_in	-	srss.ext_clk	scb[1].uart_cts:0	-	scb[2].uart_tx:1	lcd.com[6]	lcd.seg[6]	-	scb[1].spi_clk:1
29	P0.7	exco.eco_out	-	tcpwm.line[0]:3	scb[1].uart_rts:0	-	-	lcd.com[7]	lcd.seg[7]	-	scb[1].spi_select0:1
35	P1.0	pass.ctb0_pads[0]	SmartIo[2].io[0]	tcpwm.line[2]:1	scb[0].uart_rx:1	-	-	lcd.com[8]	lcd.seg[8]	scb[0].i2c_scl:0	scb[0].spi_mosi:1
36	P1.1	pass.ctb0_pads[1]	SmartIo[2].io[1]	tcpwm.line_compl[2]:1	scb[0].uart_tx:1	-	-	lcd.com[9]	lcd.seg[9]	scb[0].i2c_sda:0	scb[0].spi_miso:1
37	P1.2	pass.ctb0_pads[2] pass.ctb0_oa0_out_10x	SmartIo[2].io[2]	tcpwm.line[3]:1	scb[0].uart_cts:1	pass.dsi_sar_data[3]:0	tcpwm.tr_in[2]	lcd.com[10]	lcd.seg[10]	scb[2].i2c_scl:2	scb[0].spi_clk:1
38	P1.3	pass.ctb0_pads[3] pass.ctb0_oa1_out_10x	SmartIo[2].io[3]	tcpwm.line_compl[3]:1	scb[0].uart_rts:1	pass.dsi_sar_data[4]:0	tcpwm.tr_in[3]	lcd.com[11]	lcd.seg[11]	scb[2].i2c_sda:2	scb[0].spi_select0:1
39	P1.4	pass.ctb0_pads[4]	SmartIo[2].io[4]	tcpwm.line[6]:1	-	-	-	lcd.com[12]	lcd.seg[12]	scb[3].i2c_scl:0	scb[0].spi_select1:1

Table 2 Pin assignments (continued)

Pin	Name	Analog	Smart I/O	Alternate function 1	Alternate function 2	Alternate function 3	Alternate function 4	Deep Sleep 1	Deep Sleep 2	Deep Sleep 3	Deep Sleep 4
40	P1.7	pass.ctb0_pads[7] pass.sar_ext_vref0 pass.sar_ext_vref1	SmartIo[2].io[7]	tcpwm.line_compl[7]:1	-	-	-	lcd.com[15]	lcd.seg[15]	-	scb[2].spi_clk:1
		pass.sarmux_pads[0]	-	tcpwm.line[4]:0	csd.comp	-	tcpwm.tr_in[4]	lcd.com[16]	lcd.seg[16]	scb[1].i2c_scl:1	scb[1].spi_mosi:2
		pass.sarmux_pads[1]	-	tcpwm.line_compl[4]:0	-	-	tcpwm.tr_in[5]	lcd.com[17]	lcd.seg[17]	scb[1].i2c_sda:1	scb[1].spi_miso:2
		pass.sarmux_pads[2]	-	tcpwm.line[5]:1	-	-	-	lcd.com[18]	lcd.seg[18]	-	scb[1].spi_clk:2
1	P2.3	pass.sarmux_pads[3]	SmartIo[0].io[3]	tcpwm.line_compl[5]:1	-	-	-	lcd.com[19]	lcd.seg[19]	-	scb[1].spi_select0:2
2	P2.4	pass.sarmux_pads[4]	SmartIo[0].io[4]	tcpwm.line[0]:1	scb[3].uart_rx:1	-	-	lcd.com[20]	lcd.seg[20]	-	scb[1].spi_select1:1
3	P2.5	pass.sarmux_pads[5]	SmartIo[0].io[5]	tcpwm.line_compl[0]:1	scb[3].uart_tx:1	-	-	lcd.com[21]	lcd.seg[21]	-	scb[1].spi_select2:1
4	P2.6	pass.sarmux_pads[6]	SmartIo[0].io[6]	tcpwm.line[1]:1	scb[3].uart_cts:1	pass.dsi_sar_data[5]:0	-	lcd.com[22]	lcd.seg[22]	-	scb[1].spi_select3:1
5	P2.7	pass.sarmux_pads[7]	SmartIo[0].io[7]	tcpwm.line_compl[1]:1	scb[3].uart_rts:1	pass.dsi_sar_data[6]:0	-	lcd.com[23]	lcd.seg[23]	lpcomp.comp[0]:0	scb[2].spi_mosi:1
6	P6.0	-	-	tcpwm.line[4]:1	scb[3].uart_rx:0	-	can.can_tx_enb_n:0	lcd.com[48]	lcd.seg[48]	scb[3].i2c_scl:1	scb[3].spi_mosi:0
7	P6.1	-	-	tcpwm.line_compl[4]:1	scb[3].uart_tx:0	-	can.can_rx:0	lcd.com[49]	lcd.seg[49]	scb[3].i2c_sda:1	scb[3].spi_miso:0
8	P6.2	-	-	tcpwm.line[5]:0	scb[3].uart_cts:0	-	can.can_tx:0	lcd.com[50]	lcd.seg[50]	-	scb[3].spi_clk:0
10	P3.0	-	SmartIo[1].io[0]	tcpwm.line[0]:0	scb[1].uart_rx:1	pass.dsi_sar_data[7]:0	-	lcd.com[24]	lcd.seg[24]	scb[1].i2c_scl:2	scb[1].spi_mosi:0
11	P3.1	-	SmartIo[1].io[1]	tcpwm.line_compl[0]:0	scb[1].uart_tx:1	pass.dsi_sar_data[8]:0	-	lcd.com[25]	lcd.seg[25]	scb[1].i2c_sda:2	scb[1].spi_miso:0

Table 2 Pin assignments (continued)

Pin	Name	Analog	Smart I/O	Alternate function 1	Alternate function 2	Alternate function 3	Alternate function 4	Deep Sleep 1	Deep Sleep 2	Deep Sleep 3	Deep Sleep 4
12	P3.2	–	SmartIo[1].io[2]	tcpwm.line[1]:0	scb[1].uart_cts:1	–	–	lcd.com[26]	lcd.seg[26]	cpuss.swd_data	scb[1].spi_clk:0
13	P3.3	–	SmartIo[1].io[3]	tcpwm.line_compl[1]:0	scb[1].uart_rts:1	–	–	lcd.com[27]	lcd.seg[27]	cpuss.swd_clk	scb[1].spi_select0:0
14	P3.4	–	SmartIo[1].io[4]	tcpwm.line[2]:0	–	–	tcpwm.tr_in[6]	lcd.com[28]	lcd.seg[28]	–	scb[1].spi_select1:0
15	P3.5	–	SmartIo[1].io[5]	tcpwm.line_compl[2]:0	–	–	–	lcd.com[29]	lcd.seg[29]	–	scb[1].spi_select2:0
16	P3.6	–	SmartIo[1].io[6]	tcpwm.line[3]:0	–	pass.dsi_ctb_cmp0	–	lcd.com[30]	lcd.seg[30]	scb[4].spi_select3	scb[1].spi_select3:0
17	P3.7	–	SmartIo[1].io[7]	tcpwm.line_compl[3]:0	–	pass.dsi_ctb_cmp1	–	lcd.com[31]	lcd.seg[31]	lpcomp.comp[1]:1	scb[2].spi_miso:1
18	P4.0	csd.vref_ext csd.vref_ext_h_scomp	–	–	scb[0].uart_rx:0	pass.dsi_sar_data[9]:0	can.can_rx:1	lcd.com[32]	lcd.seg[32]	scb[0].i2c_scl:1	scb[0].spi_mosi:0
19	P4.1	csd.cshieldpads	–	–	scb[0].uart_tx:0	–	can.can_tx:1	lcd.com[33]	lcd.seg[33]	scb[0].i2c_sda:1	scb[0].spi_miso:0
20	P4.2	csd.cmodpads csd.cmodpadd	–	–	scb[0].uart_cts:0	pass.dsi_sar_data[10]:0	can.can_tx_enb_n:1	lcd.com[34]	lcd.seg[34]	lpcomp.comp[0]:1	scb[0].spi_clk:0
21	P4.3	csd.csh_tankpads csd.csh_tankpadd	–	–	scb[0].uart_rts:0	pass.dsi_sar_data[11]:0	–	lcd.com[35]	lcd.seg[35]	lpcomp.comp[1]:2	scb[0].spi_select0:0
–	–	–	–	tcpwm.line_compl[0]:2	scb[3].uart_tx:2	–	–	lcd.com[55]:0	lcd.seg[55]	scb[3].i2c_sda:2	scb[3].spi_miso:1

4 Power

The following power system diagram shows the set of power supply pins as implemented for the PSoC™ 4700S Plus. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the VDDA input.

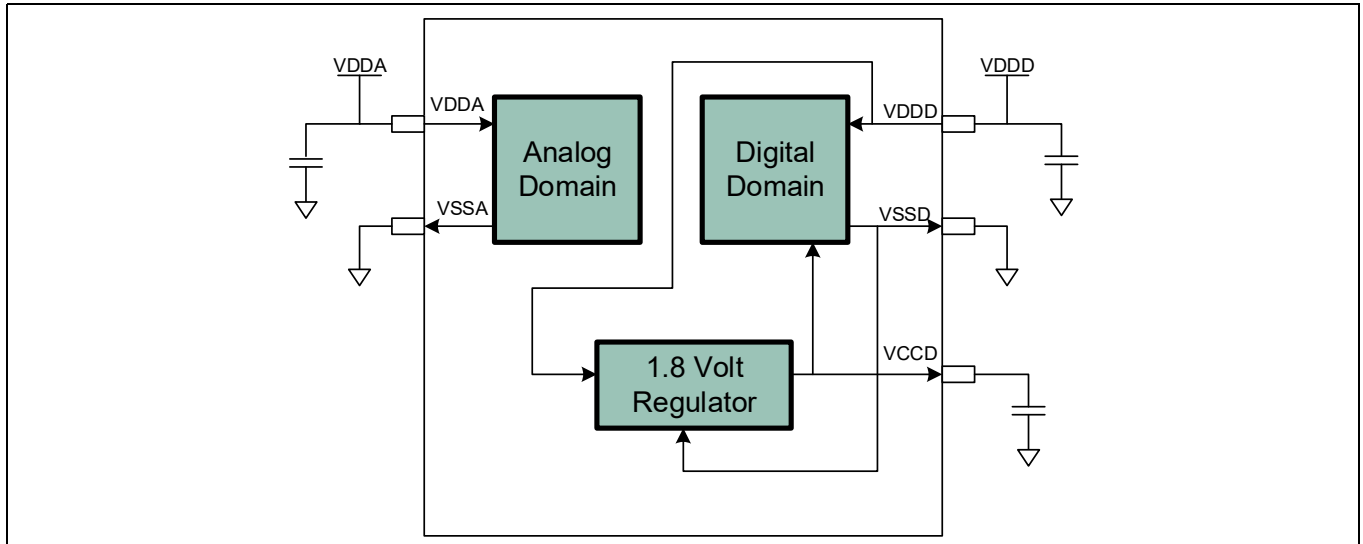


Figure 6 Power supply connections

There are two distinct modes of operation. In mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In mode 2, the supply range is 1.8 V \pm 5% (externally regulated; 1.71 to 1.89 V, internal regulator bypassed).

4.1 Mode 1: 1.8 V to 5.5 V external supply

In this mode, PSoC™ 4700S Plus is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of PSoC™ 4700S Plus supplies the internal logic and its output is connected to the VCCD pin. The VCCD pin must be bypassed to ground via an external capacitor (0.1 μ F; X5R ceramic or better) and must not be connected to anything else.

4.2 Mode 2: 1.8 V \pm 5% external supply

In this mode, PSoC™ 4700S Plus is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the VDD and VCCD pins are shorted together and bypassed.

Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1- μ F range, in parallel with a smaller capacitor (0.1 μ F, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing. On some packages, VDDD and VDDA pins are shorted inside the package and brought out as a generic VDD pin. In that case, only 0.1- μ F and 1- μ F decoupling capacitors are required on the VDD pin.

An example of a bypass scheme is shown in the following diagram.

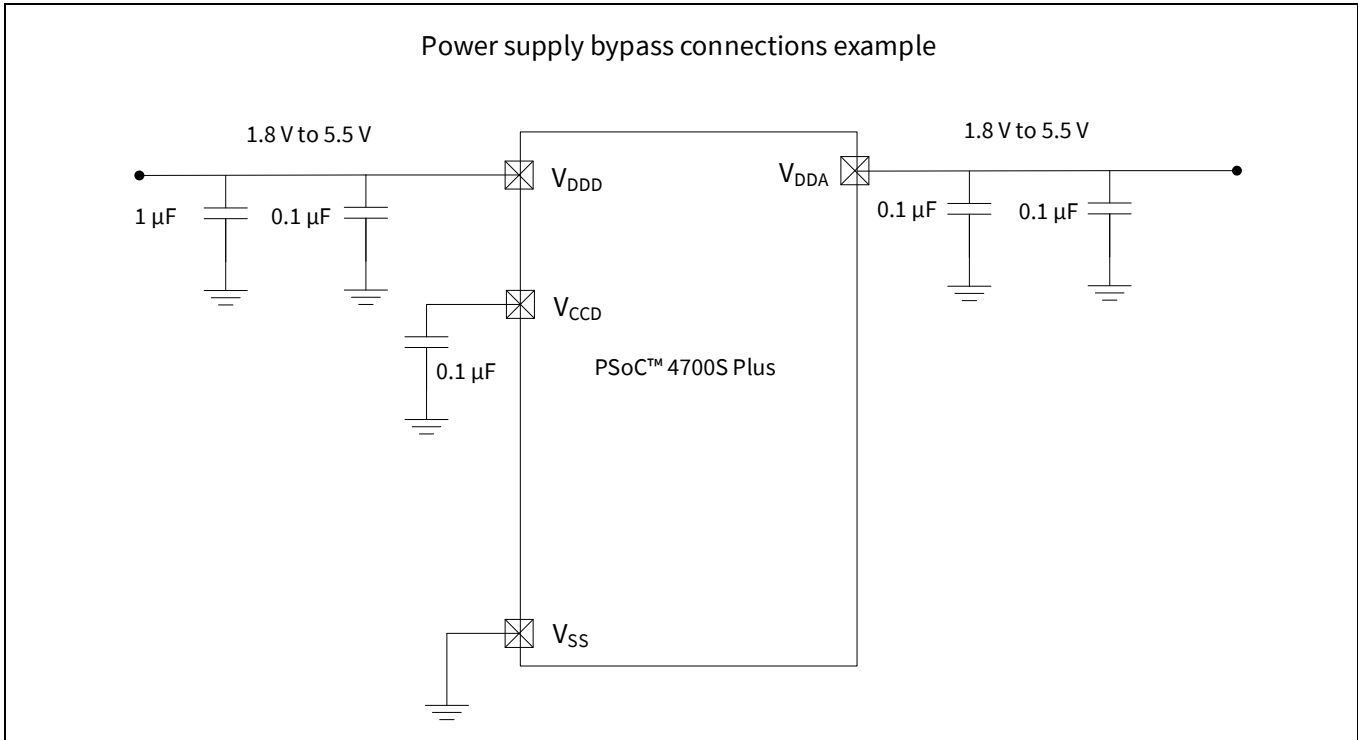


Figure 7 External supply range from 1.8 V to 5.5 V with internal regulator active

Electrical specifications

5 Electrical specifications

5.1 Absolute maximum ratings

Table 3 Absolute maximum ratings^[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID1	V _{DDD_ABS}	Digital supply relative to V _{SS}	-0.5	-	6	V	-
SID2	V _{CCD_ABS}	Direct digital core voltage input relative to V _{SS}	-0.5	-	1.95		-
SID3	V _{GPIO_ABS}	GPIO voltage	-0.5	-	V _{DD} + 0.5		-
SID4	I _{GPIO_ABS}	Maximum current per GPIO	-25	-	25	mA	-
SID5	I _{GPIO_injection}	GPIO injection current, Max for V _{IH} > V _{DDD} , and Min for V _{IL} < V _{SS}	-0.5	-	0.5		Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	-	-	V	-
BID45	ESD_CDM	Electrostatic discharge charged device model	500	-	-		-
BID46	LU	Pin current for latch-up	-140	-	140	mA	-

Note

- Usage above the absolute maximum conditions listed in [Table 3](#) may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, high temperature storage life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Electrical specifications

5.2 Device level specifications

All specifications are valid for $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ for grade-A devices, $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ for grade-S devices, and $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ for grade-E devices. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 4 DC specifications

Typical values measured at $V_{DD} = 3.3\text{ V}$ and 25°C .

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID53	V_{DD}	Power supply input voltage	1.8	–	5.5	V	Internally regulated supply
SID255	V_{DD}	Power supply input voltage ($V_{CCD} = V_{DDD} = V_{DDA}$)	1.71	–	1.89		Internally unregulated supply
SID54	V_{CCD}	Output voltage (for core logic)	–	1.8	–		–
SID55	C_{EFC}	External regulator voltage bypass	–	0.1	–	μF	X5R ceramic or better
SID56	C_{EXC}	Power supply bypass capacitor	–	1	–		X5R ceramic or better

Active mode, $V_{DD} = 1.8\text{ V}$ to 5.5 V . Typical values measured at $V_{DD} = 3.3\text{ V}$ and 25°C .

SID10	I_{DD5}	Execute from flash; CPU at 6 MHz	–	1.8	2.7	mA	Max is at 125°C and 5.5 V
SID16	I_{DD8}	Execute from flash; CPU at 24 MHz	–	3.0	5		Max is at 125°C and 5.5 V
SID19	I_{DD11}	Execute from flash; CPU at 48 MHz	–	5.4	7.6		Max is at 125°C and 5.5 V

Sleep mode, $V_{DDD} = 1.8\text{ V}$ to 5.5 V (Regulator on)

SID22	I_{DD17}	$I^2\text{C}$ wakeup WDT, and Comparators on	–	1.1	2.2	mA	6 MHz. Max is at 125°C and 5.5 V
SID25	I_{DD20}	$I^2\text{C}$ wakeup, WDT, and Comparators on	–	1.5	2.5		12 MHz. Max is at 125°C and 5.5 V

Sleep mode, $V_{DDD} = 1.71\text{ V}$ to 1.89 V (Regulator bypassed)

SID28	I_{DD23}	$I^2\text{C}$ wakeup, WDT, and Comparators on	–	1.1	1.8	mA	6 MHz. Max is at 125°C and 1.89 V .
SID28A	I_{DD23A}	$I^2\text{C}$ wakeup, WDT, and Comparators on	–	1.5	2.1		12 MHz. Max is at 125°C and 1.89 V .

Deep sleep mode, $V_{DD} = 1.8\text{ V}$ to 3.6 V (Regulator on)

SID30	I_{DD25}	$I^2\text{C}$ wakeup and WDT on	–	2.5	40	μA	$T = -40^{\circ}\text{C}$ to 60°C
SID31	I_{DD26}	$I^2\text{C}$ wakeup and WDT on	–	2.5	350		Max is at 3.6 V and 125°C

Deep sleep mode, $V_{DD} = 3.6\text{ V}$ to 5.5 V (Regulator on)

SID33	I_{DD28}	$I^2\text{C}$ wakeup and WDT on	–	2.5	40	μA	$T = -40^{\circ}\text{C}$ to 60°C
SID34	I_{DD29}	$I^2\text{C}$ wakeup and WDT on	–	2.5	350		Max is at 5.5 V and 125°C

Deep sleep mode, $V_{DD} = V_{CCD} = 1.71\text{ V}$ to 1.89 V (Regulator bypassed)

SID36	I_{DD31}	$I^2\text{C}$ wakeup and WDT on	–	2.5	60	μA	$T = -40^{\circ}\text{C}$ to 60°C
SID37	I_{DD32}	$I^2\text{C}$ wakeup and WDT on	–	2.5	400		Max is at 125°C and 1.89 V .

XRES current

SID307	I_{DD_XR}	Supply current while XRES asserted	–	2	5	mA	–
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Electrical specifications

Table 5 AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID48	F _{CPU}	CPU frequency	DC	–	48	MHz	1.71 ≤ V _{DD} ≤ 5.5
SID49	T _{SLEEP}	Wakeup from sleep mode	–	0	–	μs	–
SID50	T _{DEEPSLEEP}	Wakeup from deep sleep mode	–	35	–	–	–

5.2.1 GPIO**Table 6 GPIO DC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID57	V _{IH} ^[2]	Input voltage high threshold	0.7 × V _{DDD}	–	–	V	CMOS Input
SID58	V _{IL}	Input voltage low threshold	–	–	0.3 × V _{DDD}		CMOS Input
SID241	V _{IH} ^[2]	LVTTL input, V _{DDD} < 2.7 V	0.7 × V _{DDD}	–	–		–
SID242	V _{IL}	LVTTL input, V _{DDD} < 2.7 V	–	–	0.3 × V _{DDD}		–
SID243	V _{IH} ^[2]	LVTTL input, V _{DDD} ≥ 2.7 V	2.0	–	–		–
SID244	V _{IL}	LVTTL input, V _{DDD} ≥ 2.7 V	–	–	0.8		–
SID59	V _{OH}	Output voltage high level	V _{DDD} – 0.6	–	–		I _{OH} = 4 mA at 3 V V _{DDD}
SID60	V _{OH}	Output voltage high level	V _{DDD} – 0.5	–	–		I _{OH} = 1 mA at 1.8 V V _{DDD}
SID61	V _{OL}	Output voltage low level	–	–	0.6		I _{OL} = 4 mA at 1.8 V V _{DDD}
SID62	V _{OL}	Output voltage low level	–	–	0.6		I _{OL} = 10 mA at 3 V V _{DDD}
SID62A	V _{OL}	Output voltage low level	–	–	0.4		I _{OL} = 3 mA at 3 V V _{DDD}
SID63	R _{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID64	R _{PULLDOWN}	Pull-down resistor	3.5	5.6	8.5		–
SID65	I _{IL}	Input leakage current (absolute value)	–	–	2	nA	25°C, V _{DDD} = 3.0 V
SID66	C _{IN}	Input capacitance	–	–	7	pF	–
SID67 ^[3]	V _{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	V _{DDD} ≥ 2.7 V
SID68 ^[3]	V _{HYSCMOS}	Input hysteresis CMOS	0.05 × V _{DDD}	–	–		V _{DD} < 4.5 V
SID68A ^[3]	V _{HYSCMOS5V5}	Input hysteresis CMOS	200	–	–		V _{DD} > 4.5 V
SID69 ^[3]	I _{DIODE}	Current through protection diode to V _{DD} /V _{SS}	–	–	100	μA	–
SID69A ^[3]	I _{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Notes

- V_{IH} must not exceed V_{DDD} + 0.2 V.
- Guaranteed by characterization.

Electrical specifications

Table 7 GPIO AC specifications

(Guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID70	T _{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V _{DDD} , Cload = 25 pF
SID71	T _{FALLF}	Fall time in fast strong mode	2	–	12		3.3 V V _{DDD} , Cload = 25 pF
SID72	T _{RISES}	Rise time in slow strong mode	10	–	60	–	3.3 V V _{DDD} , Cload = 25 pF
SID73	T _{FALLS}	Fall time in slow strong mode	10	–	60	–	3.3 V V _{DDD} , Cload = 25 pF
SID74	F _{GPIOUT1}	GPIO F _{OUT} ; 3.3 V ≤ V _{DDD} ≤ 5.5 V fast strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	F _{GPIOUT2}	GPIO F _{OUT} ; 1.71 V ≤ V _{DDD} ≤ 3.3 V fast strong mode	–	–	16.7		90/10%, 25 pF load, 60/40 duty cycle
SID76	F _{GPIOUT3}	GPIO F _{OUT} ; 3.3 V ≤ V _{DDD} ≤ 5.5 V slow strong mode	–	–	7		90/10%, 25 pF load, 60/40 duty cycle
SID245	F _{GPIOUT4}	GPIO F _{OUT} ; 1.71 V ≤ V _{DDD} ≤ 3.3 V slow strong mode.	–	–	3.5		90/10%, 25 pF load, 60/40 duty cycle
SID246	F _{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V _{DDD} ≤ 5.5 V	–	–	48		90/10% V _{IO}

Electrical specifications

5.2.2 XRES

Table 8 XRES DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID77	V_{IH}	Input voltage high threshold	$0.7 \times V_{DD}$	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	$0.3 \times V_{DD}$		
SID79	R_{PULLUP}	Pull-up resistor	–	60	–	k Ω	–
SID80	C_{IN}	Input capacitance	–	–	7	pF	–
SID81 ^[4]	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Typical hysteresis is 200 mV for $V_{DD} > 4.5$ V
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	μ A	–

Table 9 XRES AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID83 ^[4]	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	μ s	–
BID194 ^[4]	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	2.7	ms	–

Note

4. Guaranteed by characterization.

Electrical specifications

5.3 Analog peripherals

5.3.1 CTBm opamp

Table 10 CTBm opamp specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
	I_{DD}	Opamp block current, External load					
SID269	I_{DD_HI}	power = hi	-	1100	1850	μA	-
SID270	I_{DD_MED}	power = med	-	550	950		-
SID271	I_{DD_LOW}	power = lo	-	150	350		-
	G_{BW}	Load = 20 pF, 0.1 mA $V_{DDA} = 2.7 V$					
SID272	G_{BW_HI}	power = hi	6	-	-	MHz	Input and output are 0.2 V to $V_{DDA} - 0.2 V$
SID273	G_{BW_MED}	power = med	3	-	-		Input and output are 0.2 V to $V_{DDA} - 0.2 V$
SID274	G_{BW_LO}	power = lo	-	1	-		Input and output are 0.2 V to $V_{DDA} - 0.2 V$
	I_{OUT_MAX}	$V_{DDA} = 2.7 V$, 500 mV from rail					
SID275	$I_{OUT_MAX_HI}$	power = hi	10	-	-	mA	Output is 0.5 V to $V_{DDA} - 0.5 V$
SID276	$I_{OUT_MAX_MID}$	power = mid	10	-	-		Output is 0.5 V to $V_{DDA} - 0.5 V$
SID277	$I_{OUT_MAX_LO}$	power = lo	-	5	-		Output is 0.5 V to $V_{DDA} - 0.5 V$
	I_{OUT}	$V_{DDA} = 1.71 V$, 500 mV from rail					
SID278	$I_{OUT_MAX_HI}$	power = hi	4	-	-	mA	Output is 0.5 V to $V_{DDA} - 0.5 V$
SID279	$I_{OUT_MAX_MID}$	power = mid	4	-	-		Output is 0.5 V to $V_{DDA} - 0.5 V$
SID280	$I_{OUT_MAX_LO}$	power = lo	-	2	-		Output is 0.5 V to $V_{DDA} - 0.5 V$
	I_{DD_Int}	Opamp block current Internal Load					
SID269_I	$I_{DD_HI_Int}$	power = hi	-	1500	1700	μA	-
SID270_I	$I_{DD_MED_Int}$	power = med	-	700	900		-
SID271_I	$I_{DD_LOW_Int}$	power = lo	-	-	-		-
	G_{BW}	$V_{DDA} = 2.7 V$	-	-	-		-
SID272_I	$G_{BW_HI_Int}$	power = hi	8	-	-	MHz	Output is 0.25 V to $V_{DDA} - 0.25 V$

Electrical specifications

Table 10 CTBm opamp specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
		General opamp specs for both internal and external modes					
SID281	V _{IN}	Charge-pump on, V _{DDA} = 2.7 V	-0.05	-	V _{DDA} - 0.2	V	-
SID282	V _{CM}	Charge-pump on, V _{DDA} = 2.7 V	-0.05	-	V _{DDA} - 0.2		-
	V _{OUT}	V _{DDA} = 2.7 V					
SID283	V _{OUT_1}	power = hi, Iload = 10 mA	0.5	-	V _{DDA} - 0.5	V	-
SID284	V _{OUT_2}	power = hi, Iload = 1 mA	0.2	-	V _{DDA} - 0.2		-
SID285	V _{OUT_3}	power = med, Iload = 1 mA	0.2	-	V _{DDA} - 0.2		-
SID286	V _{OUT_4}	power = lo, Iload = 0.1 mA	0.2	-	V _{DDA} - 0.2		-
SID288	V _{OS_TR}	Offset voltage, trimmed	-1.0	±0.5	1.0	mV	High mode, input 0 V to V _{DDA} - 0.2 V
SID288A	V _{OS_TR}	Offset voltage, trimmed	-	±1.4	-		Medium mode, input 0 V to V _{DDA} - 0.2 V
SID288B	V _{OS_TR}	Offset voltage, trimmed	-	±2	-		Low mode, input 0 V to V _{DDA} - 0.2 V
SID290	V _{OS_DR_TR}	Offset voltage drift, trimmed	-10	±3	10	μV/°C	High mode
SID290A	V _{OS_DR_TR}	Offset voltage drift, trimmed	-	±10	-	μV/°C	Medium mode
SID290B	V _{OS_DR_TR}	Offset voltage drift, trimmed	-	±10	-	μV/°C	Low mode
SID291	CMRR	DC	70	80	-	dB	Input is 0 V to V _{DDA} - 0.2 V, Output is 0.2 V to V _{DDA} - 0.2 V
SID292	PSRR	At 1 kHz, 10-mV ripple	70	85	-		V _{DDD} = 3.6 V, high-power mode, input is 0.2 V to V _{DDA} - 0.2 V
	Noise						
SID294	VN2	Input-referred, 1 kHz, power = Hi	-	72	-	nV/rtHz	-
SID295	VN3	Input-referred, 10 kHz, power = Hi	-	28	-		Input and output are at 0.2 V to V _{DDA} - 0.2 V
SID296	VN4	Input-referred, 100 kHz, power = Hi	-	15	-		Input and output are at 0.2 V to V _{DDA} - 0.2 V
SID297	C _{LOAD}	Stable up to max. load. Performance specs at 50 pF.	-	-	125	pF	-
SID298	SLEW_RATE	Cload = 50 pF, Power = High, V _{DDA} = 2.7 V	6	-	-	V/μs	-
SID299	T _{OP_WAKE}	From disable to enable, no external RC dominating	-	-	25	μs	-
SID299A	OL_GAIN	Open Loop Gain	-	90	-	dB	-

Electrical specifications

Table 10 CTBm opamp specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
	COMP_MODE	Comparator mode; 50 mV drive, $T_{rise} = T_{fall}$ (approx.)					
SID300	TPD1	Response time; power = hi	–	150	–	ns	Input is 0.2 V to $V_{DDA} - 0.2$ V
SID301	TPD2	Response time; power = med	–	500	–		Input is 0.2 V to $V_{DDA} - 0.2$ V
SID302	TPD3	Response time; power = lo	–	2500	–		Input is 0.2 V to $V_{DDA} - 0.2$ V
SID303	VHYST_OP	Hysteresis	–	10	–	mV	–
SID304	WUP_CTB	Wake-up time from Enabled to Usable	–	–	25	µs	–
	Deep sleep mode	Mode 2 is lowest current range. Mode 1 has higher GBW.					
SID_DS_1	I _{DD_HI_M1}	Mode 1, high current	–	1400	–	µA	25°C
SID_DS_2	I _{DD_MED_M1}	Mode 1, medium current	–	700	–		25°C
SID_DS_3	I _{DD_LOW_M1}	Mode 1, low current	–	200	–		25°C
SID_DS_4	I _{DD_HI_M2}	Mode 2, high current	–	120	–		25°C
SID_DS_5	I _{DD_MED_M2}	Mode 2, medium current	–	60	–		25°C
SID_DS_6	I _{DD_LOW_M2}	Mode 2, low current	–	15	–		25°C
SID_DS_7	G _{BW_HI_M1}	Mode 1, high current	–	4	–	MHz	20-pF load, no DC load 0.2 V to $V_{DDA} - 0.2$ V
SID_DS_8	G _{BW_MED_M1}	Mode 1, medium current	–	2	–		20-pF load, no DC load 0.2 V to $V_{DDA} - 0.2$ V
SID_DS_9	G _{BW_LOW_M1}	Mode 1, low current	–	0.5	–		20-pF load, no DC load 0.2 V to $V_{DDA} - 0.2$ V
SID_DS_10	G _{BW_HI_M2}	Mode 2, high current	–	0.5	–		20-pF load, no DC load 0.2 V to $V_{DDA} - 0.2$ V
SID_DS_11	G _{BW_MED_M2}	Mode 2, medium current	–	0.2	–		20-pF load, no DC load 0.2 V to $V_{DDA} - 0.2$ V
SID_DS_12	G _{BW_Low_M2}	Mode 2, low current	–	0.1	–		20-pF load, no DC load 0.2 V to $V_{DDA} - 0.2$ V
SID_DS_13	V _{OS_HI_M1}	Mode 1, high current	–	5	–	mV	With trim 25°C, 0.2 V to $V_{DDA} - 0.2$ V
SID_DS_14	V _{OS_MED_M1}	Mode 1, medium current	–	5	–		With trim 25°C, 0.2 V to $V_{DDA} - 0.2$ V
SID_DS_15	V _{OS_LOW_M2}	Mode 1, low current	–	5	–		With trim 25°C, 0.2 V to $V_{DDA} - 0.2$ V
SID_DS_16	V _{OS_HI_M2}	Mode 2, high current	–	5	–		With trim 25°C, 0.2V to $V_{DDA} - 0.2$ V
SID_DS_17	V _{OS_MED_M2}	Mode 2, medium current	–	5	–		With trim 25°C, 0.2 V to $V_{DDA} - 0.2$ V
SID_DS_18	V _{OS_LOW_M2}	Mode 2, low current	–	5	–		With trim 25°C, 0.2 V to $V_{DDA} - 0.2$ V

Electrical specifications

Table 10 CTBm opamp specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID_DS_19	I _{OUT_HI_M1}	Mode 1, high current	–	10	–	mA	Output is 0.5 V to V _{DDA} – 0.5 V
SID_DS_20	I _{OUT_MED_M1}	Mode 1, medium current	–	10	–		Output is 0.5 V to V _{DDA} – 0.5 V
SID_DS_21	I _{OUT_LOW_M1}	Mode 1, low current	–	4	–		Output is 0.5 V to V _{DDA} – 0.5 V
SID_DS_22	I _{OUT_HI_M2}	Mode 2, high current	–	1	–		–
SID_DS_23	I _{OU_MED_M2}	Mode 2, medium current	–	1	–		–
SID_DS_24	I _{OU_LOW_M2}	Mode 2, low current	–	0.5	–		–

Electrical specifications

5.3.2 Comparator

Table 11 Comparator DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID84	V _{OFFSET1}	Input offset voltage, factory trim	-	-	±10	mV	-
SID85	V _{OFFSET2}	Input offset voltage, custom trim	-	-	±4		-
SID86	V _{HYST}	Hysteresis when enabled	-	10	35		-
SID87	V _{ICM1}	Input common mode voltage in normal mode	0	-	V _{DDD} -0.1	V	Modes 1 and 2
SID247	V _{ICM2}	Input common mode voltage in low power mode	0	-	V _{DDD}		-
SID247A	V _{ICM3}	Input common mode voltage in ultra low power mode	0	-	V _{DDD} -1.15		V _{DDD} ≥ 2.2 V at -40°C
SID88	C _{MRR}	Common mode rejection ratio	50	-	-	dB	V _{DDD} ≥ 2.7 V
SID88A	C _{MRR}	Common mode rejection ratio	42	-	-		V _{DDD} ≤ 2.7 V
SID89	I _{CMP1}	Block current, normal mode	-	-	400	μA	-
SID248	I _{CMP2}	Block current, low power mode	-	-	100		-
SID259	I _{CMP3}	Block current in ultra low-power mode	-	-	6		V _{DDD} ≥ 2.2 V at -40°C
SID90	Z _{CMP}	DC Input impedance of comparator	35	-	-	MΩ	-

Table 12 Comparator AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID91	T _{RESP1}	Response time, normal mode, 50 mV overdrive	-	38	110	ns	-
SID258	T _{RESP2}	Response time, low power mode, 50 mV overdrive	-	70	200		-
SID92	T _{RESP3}	Response time, ultra-low power mode, 200 mV overdrive	-	2.3	15	μs	V _{DDD} ≥ 2.2 V at -40°C

5.3.3 Temperature sensor

Table 13 Temperature sensor specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID93	T _{SENSACC}	Temperature sensor accuracy	-5	±1	5	°C	-40 to +85°C
SID93A	T _{SENSACC}	Temperature sensor accuracy	-15	±1	+15	°C	+85 to +150°C

Electrical specifications

5.3.4 SAR ADC

Table 14 SAR ADC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SAR ADC DC specifications							
SID94	A_RES	Resolution	–	–	12	bits	–
SID95	A_CHNLS_S	Number of channels - single ended	–	–	16		–
SID96	A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1 V reference
SID100	A_ISAR	Current consumption	–	–	1	mA	–
SID101	A_VINS	Input voltage range - single ended	V _{SS}	–	V _{DDA}	V	–
SID102	A_VIND	Input voltage range - differential	V _{SS}	–	V _{DDA}	V	–
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	–
SID104	A_INCAP	Input capacitance	–	–	10	pF	–
SID260	VREFSAR	Trimmed internal reference to SAR	1.188	1.2	1.212	V	–

Electrical specifications

Table 14 SAR ADC specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SAR ADC AC specifications							
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	–
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP	Sample rate	–	–	1	Msp/s	–
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	$F_{IN} = 10 \text{ kHz}$
SID110	A_BW	Input bandwidth without aliasing	–	–	$A_{\text{sam}}/2$	kHz	–
SID111	A_INL	Integral non linearity. $V_{DD} = 1.71 \text{ to } 5.5, 1 \text{ Msps}$	–1.7	–	2	LSB	$V_{REF} = 1 \text{ to } V_{DD}$
SID111A	A_INL	Integral non linearity. $V_{DD} = 1.71 \text{ to } 3.6, 1 \text{ Msps}$	–1.5	–	1.7	LSB	$V_{REF} = 1.71 \text{ to } V_{DD}$
SID111B	A_INL	Integral non linearity. $V_{DD} = 1.71 \text{ to } 5.5, 500 \text{ ksps}$	–1.5	–	1.7	LSB	$V_{REF} = 1 \text{ to } V_{DD}$
SID112	A_DNL	Differential non linearity. $V_{DD} = 1.71 \text{ to } 5.5, 1 \text{ Msps}$	–1	–	2.2	LSB	$V_{REF} = 1 \text{ to } V_{DD}$
SID112A	A_DNL	Differential non linearity. $V_{DD} = 1.71 \text{ to } 3.6, 1 \text{ Msps}$	–1	–	2	LSB	$V_{REF} = 1.71 \text{ to } V_{DD}$
SID112B	A_DNL	Differential non linearity. $V_{DD} = 1.71 \text{ to } 5.5, 500 \text{ ksps}$	–1	–	2.2	LSB	$V_{REF} = 1 \text{ to } V_{DD}$
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	$F_{in} = 10 \text{ kHz}$
SID261	FSARINTREF	SAR operating speed without external reference bypass	–	–	100	ksps	12-bit resolution

Electrical specifications

5.3.5 CSD and IDAC

Table 15 CSD and IDAC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	-	-	±50	mV	$V_{DD} > 2\text{ V}$ (with ripple), $25^\circ\text{C } T_A$, sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	-	-	±25	mV	$V_{DD} > 1.75\text{ V}$ (with ripple), $25^\circ\text{C } T_A$, parasitic capacitance (C_P) < 20 pF, sensitivity $\geq 0.4\text{ pF}$
SID.CSD.BLK	ICSD	Maximum block current	-	-	4000	μA	Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator
SID.CSD#15	V _{REF}	Voltage reference for CSD and comparator	0.6	1.2	$V_{DDA} - 0.6$	V	$V_{DDA} - 0.06$ or 4.4, whichever is lower
SID.CSD#15A	VREF_EXT	External voltage reference for CSD and comparator	0.6		$V_{DDA} - 0.6$	V	$V_{DDA} - 0.06$ or 4.4, whichever is lower
SID.CSD#16	IDAC1IDD	IDAC1 (7-bits) block current	-	-	1750	μA	-
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	-	-	1750	μA	-
SID308	VCSD	Voltage range of operation	1.71	-	5.5	V	$1.8\text{ V} \pm 5\%$ or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.6	-	$V_{DDA} - 0.6$	V	$V_{DDA} - 0.06$ or 4.4, whichever is lower
SID309	IDAC1DNL	DNL	-1	-	1	LSB	-
SID310	IDAC1INL	INL	-2	-	2	LSB	INL is ± 5.5 LSB for $V_{DDA} < 2\text{ V}$
SID311	IDAC2DNL	DNL	-1	-	1	LSB	-
SID312	IDAC2INL	INL	-2	-	2	LSB	INL is ± 5.5 LSB for $V_{DDA} < 2\text{ V}$
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	-	-	Ratio	Capacitance range of 5 to 35 pF, 0.1-pF sensitivity. All use cases. $V_{DDA} > 2\text{ V}$.
SID314	IDAC1CRT1	Output current of IDAC1 (7 bits) in low range	4.2	-	5.4	μA	LSB = 37.5 nA typ
SID314A	IDAC1CRT2	Output current of IDAC1 (7 bits) in medium range	34	-	41	μA	LSB = 300 nA typ
SID314B	IDAC1CRT3	Output current of IDAC1 (7 bits) in high range	275	-	330	μA	LSB = 2.4 μA typ
SID314C	IDAC1CRT12	Output current of IDAC1 (7 bits) in low range, 2X mode	8	-	10.5	μA	LSB = 75 nA typ

Electrical specifications

Table 15 CSD and IDAC specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID314D	IDAC1CRT22	Output current of IDAC1 (7 bits) in medium range, 2X mode	69	–	82	μA	LSB = 600 nA typ.
SID314E	IDAC1CRT32	Output current of IDAC1 (7 bits) in high range, 2X mode	540	–	660	μA	LSB = 4.8 μA typ
SID315	IDAC2CRT1	Output current of IDAC2 (7 bits) in low range	4.2	–	5.4	μA	LSB = 37.5 nA typ
SID315A	IDAC2CRT2	Output current of IDAC2 (7 bits) in medium range	34	–	41	μA	LSB = 300 nA typ
SID315B	IDAC2CRT3	Output current of IDAC2 (7 bits) in high range	275	–	330	μA	LSB = 2.4 μA typ
SID315C	IDAC2CRT12	Output current of IDAC2 (7 bits) in low range, 2X mode	8	–	10.5	μA	LSB = 75 nA typ
SID315D	IDAC2CRT22	Output current of IDAC2 (7 bits) in medium range, 2X mode	69	–	82	μA	LSB = 600 nA typ
SID315E	IDAC2CRT32	Output current of IDAC2 (7 bits) in high range, 2X mode	540	–	660	μA	LSB = 4.8 μA typ
SID315F	IDAC3CRT13	Output current of IDAC in 8-bit mode in low range	8	–	10.5	μA	LSB = 37.5 nA typ
SID315G	IDAC3CRT23	Output current of IDAC in 8-bit mode in medium range	69	–	82	μA	LSB = 300 nA typ
SID315H	IDAC3CRT33	Output current of IDAC in 8-bit mode in high range	540	–	660	μA	LSB = 2.4 μA typ
SID320	IDACOFFSET	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode
SID321	IDACGAIN	Full-scale error less offset	–	–	±10	%	–
SID322	IDACMIS-MATCH1	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5 nA typ
SID322A	IDACMIS-MATCH2	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	5.6	LSB	LSB = 300 nA typ
SID322B	IDACMIS-MATCH3	Mismatch between IDAC1 and IDAC2 in High mode	–	–	6.8	LSB	LSB = 2.4 μA typ
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	5	μs	Full-scale transition. No external load
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	5	μs	Full-scale transition. No external load
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap

Electrical specifications

5.3.6 10-bit CAPSENSE™ ADC

Table 16 10-bit CAPSENSE™ ADC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SIDA94	A_RES	Resolution	–	–	10	bits	Auto-zeroing is required every millisecond
SIDA95	A_CHNLS_S	Number of channels - single ended	–	–	16		Defined by AMUX Bus
SIDA97	A-MONO	Monotonicity	–	–	–	Yes	–
SIDA98	A_GAINERR	Gain error	–	–	±3	%	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 μ F
SIDA99	A_OFFSET	Input offset voltage	–	–	±18	mV	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 μ F
SIDA101	A_VINS	Input voltage range - single ended	V_{SSA}	–	V_{DDA}	V	–
SIDA103	A_INRES	Input resistance	–	2.2	–	K Ω	–
SIDA104	A_INCAP	Input capacitance	–	20	–	pF	–
SIDA106	A_PSRR	Power supply rejection ratio	–	60	–	dB	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 μ F
SIDA107	A_TACQ	Sample acquisition time	–	1	–	μ s	–
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = $F_{hclk}/(2^{(N+2)})$. Clock frequency = 48 MHz.	–	–	21.3	μ s	Does not include acquisition time. Equivalent to 44.8 ksps including acquisition time.
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = $F_{hclk}/(2^{(N+2)})$. Clock frequency = 48 MHz.	–	–	85.3	μ s	Does not include acquisition time. Equivalent to 11.6 ksps including acquisition time.
SIDA109	A_SND	Signal-to-noise and Distortion ratio (SINAD)	–	61	–	dB	With 10-Hz input sine wave, external 2.4-V reference, V_{REF} (2.4 V) mode
SIDA110	A_BW	Input bandwidth without aliasing	–	–	22.4	KHz	8-bit resolution
SIDA111	A_INL	Integral Non Linearity. 1 ksps	–	–	2	LSB	$V_{REF} = 2.4$ V or greater
SIDA112	A_DNL	Differential Non Linearity. 1 ksps	–	–	1		–

Electrical specifications

5.3.7 Inductive sensing

Table 17 Inductive sense specifications (Preliminary data; unless otherwise mentioned $V_{DD} > 2.7 V$)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID500	Nsense	Number of sensors	–	4	–	–	–
SID501	Lsmp	Sample rate	–	–	12	ksps	Measured at below conditions: Resolution = 11bits, sensor operating frequency (Fout) = 12 MHz refer sec 2.8.8
SID502	Lres	Resolution	–	–	16	bits	–
SID503	Lfreq	Sensor excitation frequency	1	–	12	MHz	–
SID505	Lval	Inductance range	1	–	10000	μH	–
SID506	Lprox	Proximity detection range	–	0.75 × coil diameter	–	–	–
			–	1.5 × coil diameter	–	–	If ECO is used
SID507	Rp	Tank impedance	500	–	10000	Ω	–

Electrical specifications

5.4 Digital peripherals

5.4.1 Timer counter pulse-width modulator (TCPWM)

Table 18 TCPWM specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	μA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155		All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650		All modes (TCPWM)
SID.TCPWM.3	TCPWM _{FREQ}	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS Maximum = 48 MHz
SID.TCPWM.4	TPWM _{ENEXT}	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events ^[5]
SID.TCPWM.5	TPWM _{EXT}	Output trigger pulse widths	2/Fc	–	–		Minimum possible width of overflow, underflow, and CC (counter equals compare value) outputs
SID.TCPWM.5A	TC _{RES}	Resolution of counter	1/Fc	–	–		Minimum time between successive counts
SID.TCPWM.5B	PWM _{RES}	PWM resolution	1/Fc	–	–		Minimum pulse width of PWM Output
SID.TCPWM.5C	Q _{RES}	Quadrature inputs resolution	1/Fc	–	–		Minimum pulse width between Quadrature phase inputs

Note

5. Guaranteed by characterization.

Electrical specifications

5.4.2 I²CTable 19 Fixed I²C DC specifications^[6]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID149	I _{I2C1}	Block current consumption at 100 kHz	-	-	50	μA	-
SID150	I _{I2C2}	Block current consumption at 400 kHz	-	-	135		-
SID151	I _{I2C3}	Block current consumption at 1 Mbps	-	-	310		-
SID152	I _{I2C4}	I ² C enabled in deep sleep mode	-	1	-		-

Table 20 Fixed I²C AC specifications^[6]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID153	F _{I2C1}	Bit rate	-	-	1	Mbps	-

Note

6. Guaranteed by characterization.

Electrical specifications

5.4.3 SPI

Table 21 SPI DC specifications^[7]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID163	ISPI1	Block current consumption at 1 Mbps	-	-	360	μA	-
SID164	ISPI2	Block current consumption at 4 Mbps	-	-	560		-
SID165	ISPI3	Block current consumption at 8 Mbps	-	-	600		-

Table 22 SPI AC specifications^[8]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID166	FSPI	SPI Operating frequency (Master; 6X Oversampling)	-	-	8	MHz	-

Fixed SPI master mode AC specifications

SID167	TDMO	MOSI Valid after Sclock driving edge	-	-	15	ns	-
SID168	TDSI	MISO Valid before Sclock capturing edge	20	-	-		Full clock, late MISO sampling
SID169	THMO	Previous MOSI data hold time	0	-	-		Referred to slave capturing edge

Fixed SPI slave mode AC specifications

SID170	TDMI	MOSI valid before Sclock capturing edge	40	-	-	ns	-
SID171	TDSO	MISO valid after Sclock driving edge	-	-	42 + (3 × Tcpu)		$T_{CPU} = 1/F_{CPU}$
SID171A	TDSO_EXT	MISO valid after Sclock driving edge in Ext. Clk mode	-	-	48		-
SID172	THSO	Previous MISO data hold time	0	-	-		-
SID172A	TSSELSSCK	SSEL Valid to first SCK valid edge	-	-	100	ns	-

Note

7. Guaranteed by characterization.

Electrical specifications

5.4.4 UART

Table 23 UART DC specifications^[8]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID160	I _{UART1}	Block current consumption at 100 Kbps	–	–	55	μA	–
SID161	I _{UART2}	Block current consumption at 1000 Kbps	–	–	312	μA	–

Table 24 UART AC specifications^[8]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID162	F _{UART}	Bit rate	–	–	1	Mbps	–

5.4.5 LCD direct drive

Table 25 LCD direct drive DC specifications^[8]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID154	I _{LCDLOW}	Operating current in low power mode	–	5	–	μA	16 × 4 small segment disp. at 50 Hz
SID155	C _{LDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD _{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I _{LCDOP1}	LCD system operating current V _{bias} = 5 V	–	2	–	mA	32 × 4 segments at 50 Hz, 25°C
SID158	I _{LCDOP2}	LCD system operating current V _{bias} = 3.3 V	–	2	–		32 × 4 segments at 50 Hz, 25°C

Table 26 LCD direct drive AC specifications^[8]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID159	F _{LCD}	LCD frame rate	10	50	150	Hz	–

Note

8. Guaranteed by characterization.

Electrical specifications

5.5 Memory

5.5.1 Flash

Table 27 Flash DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID173	V _{PE}	Erase and program voltage	1.71	–	5.5	V	–

Table 28 Flash AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID174	T _{ROWWRITE} ^[9]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 256 bytes
SID175	T _{ROWERASE} ^[9]	Row erase time	–	–	16		–
SID176	T _{ROWPROGRAM} ^[9]	Row program time after erase	–	–	4		–
SID178	T _{BULKERASE} ^[9]	Bulk erase time (64KB)	–	–	35		–
SID180 ^[10]	T _{DEVPROG} ^[9]	Total device program time	–	–	7	Seconds	–
SID181 ^[10]	F _{END}	Flash endurance	100K	–	–	Cycles	–
SID182 ^[10]	F _{RET}	Flash retention. T _A ≤ 55°C, 100K P/E cycles	20	–	–	Years	–
SID182A ^[10]	F _{RET}	Flash retention. T _A ≤ 85°C, 10K P/E cycles	10	–	–		–
SID182B	F _{RETQ}	Flash retention. T _A ≤ 105°C, 10K P/E cycles with no more than 3 years at T _A > 85°C	10	–	–		Guaranteed by design
SID256	TWS48	Number of Wait states at 48 MHz	2	–	–		CPU execution from Flash
SID257	TWS24	Number of Wait states at 24 MHz	1	–	–		CPU execution from Flash

Notes

9. It can take as much as 20 milliseconds to write to flash. During this time the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

10. Guaranteed by characterization.

Electrical specifications

5.6 System resources

5.6.1 Power-on reset (POR)

Table 29 Power-on reset (PRES)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#6	SR_POWER	Power supply slew rate	1 ^[11]	–	67	V/ms	On power-up and power-down
SID185 ^[12]	V _{RISEIPOR}	Rising trip voltage	0.80	–	1.5	V	–
SID186 ^[12]	V _{FALLIPOR}	Falling trip voltage	0.70	–	1.4		–

5.6.2 Brown-out detect (BOD)

Table 30 Brown-out detect (BOD) for V_{CCD}

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID190 ^[12]	V _{FALLPPOR}	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID192 ^[12]	V _{FALLDPSLP}	BOD trip voltage in Deep Sleep	1.11	–	1.5		–

5.6.3 SWD interface

Table 31 SWD interface specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID213	F_SWDCCLK1	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCLK \leq 1/3 CPU clock frequency
SID214	F_SWDCCLK2	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7		SWDCLK \leq 1/3 CPU clock frequency
SID215 ^[12]	T_SWDI_SETUP	$T = 1/f\text{ SWDCLK}$	$0.25 \times T$	–	–	ns	–
SID216 ^[12]	T_SWDI_HOLD	$T = 1/f\text{ SWDCLK}$	$0.25 \times T$	–	–		–
SID217 ^[12]	T_SWDO_VALID	$T = 1/f\text{ SWDCLK}$	–	–	$0.5 \times T$		–
SID217A ^[12]	T_SWDO_HOLD	$T = 1/f\text{ SWDCLK}$	1	–	–		–

Notes

11.If the minimum ramp rate cannot be met, XRES should be asserted during the voltage ramp (1.5 V > V_{DDD} > 1.0 V for ramp-down or until the voltage is stable for ramp-up). Note that a glitch on the I2C bus could occur during the voltage ramp in this case.

12.Guaranteed by characterization.

Electrical specifications

5.6.4 Internal Main Oscillator

Table 32 IMO DC specifications

(Guaranteed by design)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID218	I _{IMO1}	IMO operating current at 48 MHz	–	–	250	μA	–
SID219	I _{IMO2}	IMO operating current at 24 MHz	–	–	180	μA	–

Table 33 IMO AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID223	F _{IMOTOL1}	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±2	%	–40°C ≤ T _A ≤ 105°C
SID223A	F _{IMOTOL1A}	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±2.5	%	–40°C ≤ T _A ≤ 125°C
SID333	IMO _{WCO}	All IMO settings	–	–	±0.25	%	IMO variation in WCO-locked DPLL mode
SID226	T _{STARTIMO}	IMO startup time	–	–	7	μs	–
SID228	T _{JITRMSIMO2}	RMS jitter at 24 MHz	–	145	–	ps	–

5.6.5 Internal low-speed oscillator

Table 34 ILO DC specifications

(Guaranteed by design)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID231	I _{ILO1}	ILO operating current	–	0.3	1.05	μA	–

Table 35 ILO AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID234 ^[13]	T _{STARTILO1}	ILO startup time	–	–	2	ms	–
SID236 ^[13]	T _{ILODUTY}	ILO duty cycle	40	50	60	%	–
SID237	F _{ILOTRIM1}	ILO frequency range	20	40	80	kHz	–

Notes

13. Guaranteed by characterization.

Electrical specifications

5.6.6 Watch crystal oscillator (WCO)

Table 36 WCO specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID398	FWCO	Crystal frequency	–	32.768	–	kHz	–
SID399	FTOL	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	–
SID401	PD	Drive level	–	–	1	μW	–
SID402	TSTART	Startup time	–	–	500	ms	–
SID403	CL	Crystal load capacitance	6	–	12.5	pF	–
SID404	C0	Crystal shunt capacitance	–	1.35	–	pF	–
SID405	IWCO1	Operating current (high power mode)	–	–	8	μA	–

5.6.7 External clock

Table 37 External clock specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID305 ^[14]	ExtClkFreq	External clock input frequency	0	–	48	MHz	–40°C ≤ T _A ≤ 85°C
SID306 ^[14]	ExtClkDuty	Duty cycle; measured at V _{DD/2}	45	–	55	%	–40°C ≤ T _A ≤ 85°C

Notes

14. Guaranteed by design.

Electrical specifications

5.6.8 External Crystal Oscillator (ECO) and PLL

Table 38 ECO specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID316 ^[15]	IECO1	External clock input frequency	–	–	1.5	mA	–
SID317 ^[15]	FECO	Crystal frequency range	4	–	33	MHz	–

Table 39 PLL specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID410	IDD_PLL_48	In = 3 MHz, Out = 48 MHz	–	530	610	μA	–
SID411	IDD_PLL_24	In = 3 MHz, Out = 24 MHz	–	300	405	μA	–
SID412	Fpffin	PLL input frequency	1	–	48	MHz	–
SID413	Fpffint	PLL intermediate frequency; prescaler out	1	–	3	MHz	–
SID414	Fpffvco	VCO output frequency before post-divide	22.5	–	104	MHz	–
SID415	Divvco	VCO Output post-divider range; PLL output frequency is Fpffvco/Divvco	1	–	8		–
SID416	Pllocktime	Lock time at startup	–	–	250	μs	–
SID417	Jperiod_1	Period jitter for VCO ≥ 67 MHz	–	–	150	ps	Guaranteed by design –40°C ≤ T _A ≤ 85°C
SID416A	Jperiod_2	Period jitter for VCO ≤ 67 MHz	–	–	200	ps	Guaranteed by design –40°C ≤ T _A ≤ 85°C

5.6.9 System clock

Table 40 Block specs

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID262 ^[15]	T _{CLKSWITCH}	System clock source switching time	3	–	4	Periods	–

5.6.10 Smart I/O

Table 41 Smart I/O pass-through time (delay in bypass mode)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID252	PRG_BYPASS	Max delay added by smart I/O in bypass mode	–	–	1.6	ns	–

Notes

15. Guaranteed by design.

6 Ordering information

Table 42 lists the marketing part numbers (MPNs) for the PSoC™ 4700S Plus devices.

Table 42 Ordering information

PSoC™ family category	MPN	Features																		Packages	Operating temperature		
		Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Op-amp (CTBm)	CAPSENSE™	Inductive sense	Direct LCD drive	12-bit SAR ADC	LP Comparators	TCPWM blocks	SCB blocks	WCO	ECO	Smart I/Os	CAN	GPIO	40-QFN		-40 to +85°C	-40 to +105°C	-40 to +125°C
4700S Plus	CY8C4746LQS-S263	48	64	8	-	-	X	X	-	1000 Ksps	2	8	4	X	X	19	-	34	X	-	X	-	
4700S Plus	CY8C4747LQS-S453	48	128	8	-	2	X	X	X	1000 Ksps	2	8	4	X	X	19	-	34	X	-	X	-	

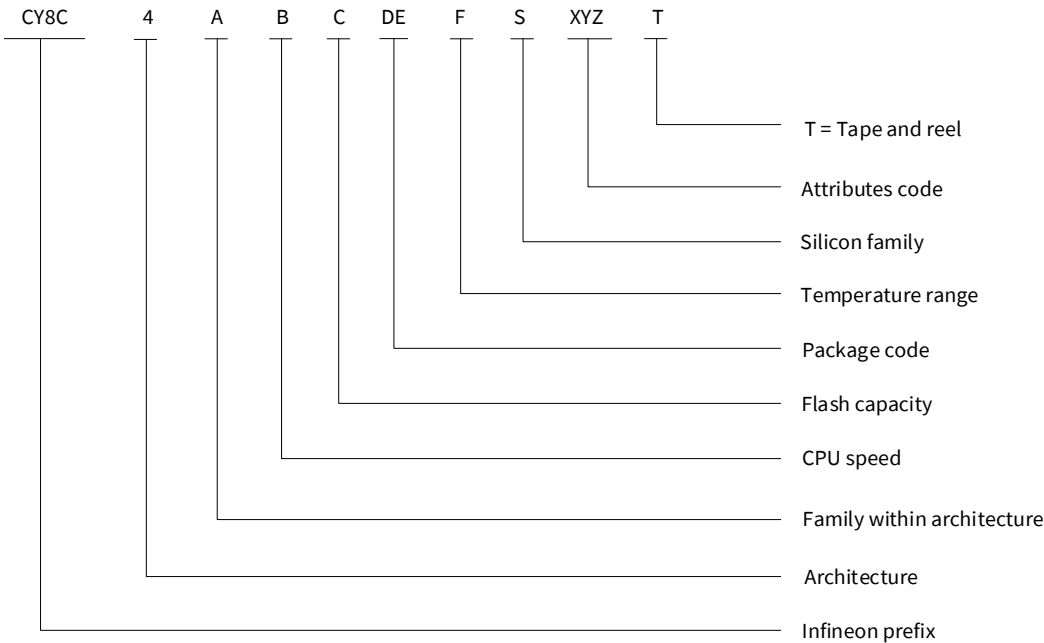


Ordering information

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Infineon prefix		
4	Architecture	4	PSoC™ 4
A	Family	7	4700S family
B	CPU speed	2	24 MHz
		4	48 MHz
C	Flash capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package code	LQ	QFN
F	Temperature range	S	Automotive (AEC-Q100: -40°C to +105°C)
S	Silicon family	S	PSoC™ 4 S-series
		M	PSoC™ 4 M-series
		L	PSoC™ 4 L-series
XYZ	Attributes code	000-999	Code of feature set in the specific family

The following is an example of a part number:



Example

- 4: PSoC™ 4
- 1: 4700S Plus family
- 4: 48 MHz
- 6: 64 KB
- LQ: QFN
- S: Automotive

Packaging

7 Packaging

The PSoC™ 4700S Plus will be offered in 40-QFN package.

Table 43 provides the package dimensions and drawing numbers.

Table 43 Package list

Spec ID#	Package	Description	Package dwg
BID27A	40-pin QFN	6 × 6 × 0.6-mm height with 0.5-mm pitch with wettable flanks	002-25105

Table 44 Package thermal characteristics

Parameter	Description	Package	Conditions	Min	Typ	Max	Unit
T _A	Operating ambient temperature	–	For S-grade devices	–40	25	105	
T _J	Operating junction temperature	–	For S-grade devices	–40	–	115	
T _{JA}	Package θ_{JA}	40-pin QFN	–	–	25	–	°C/W
T _{JC}	Package θ_{JC}	40-pin QFN	–	–	3	–	°C/W

Table 45 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time at peak temperature
All	260 °C	30 seconds

Table 46 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-020

Package	MSL
All	MSL 3

Packaging

7.1 Package diagram

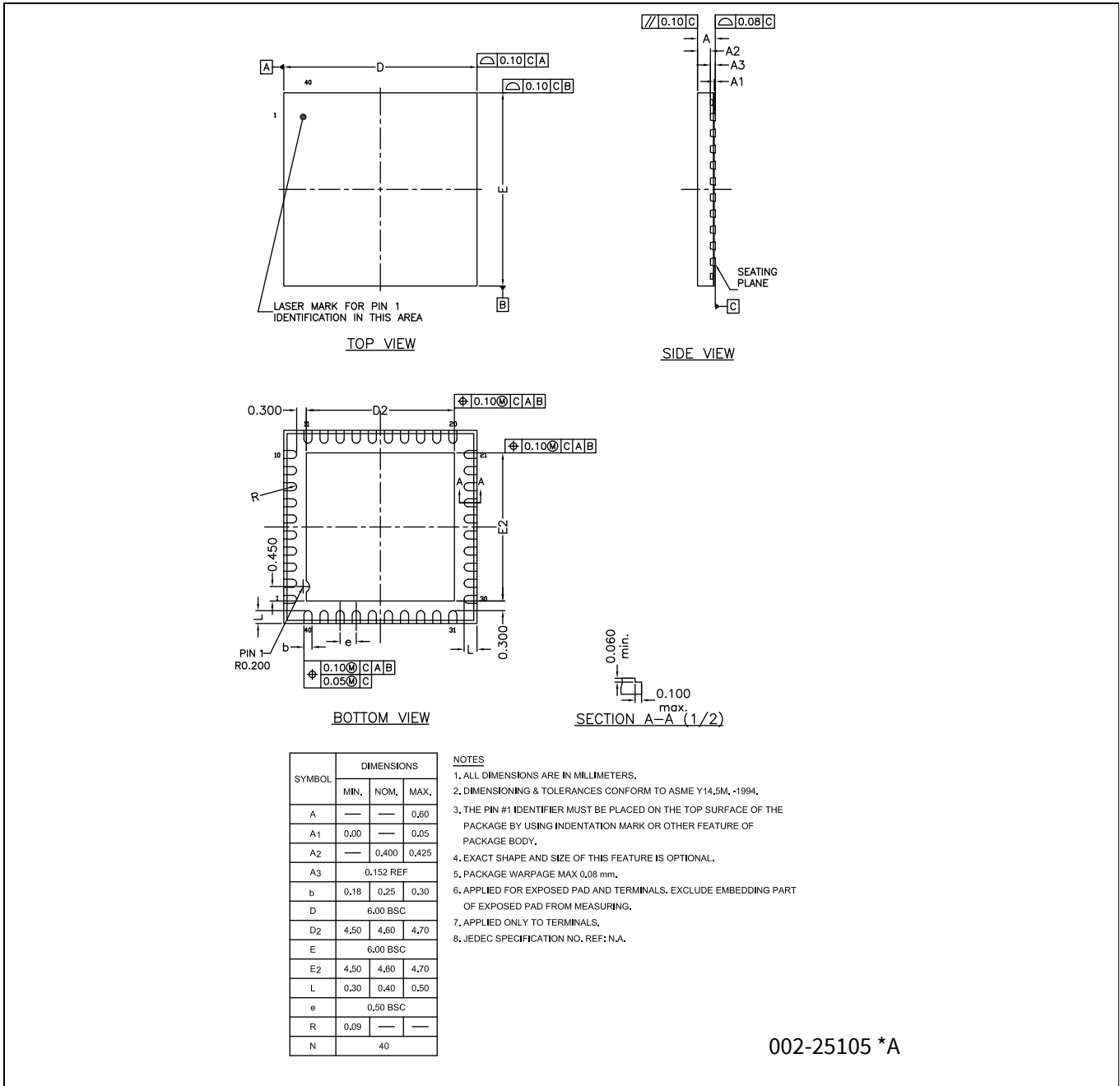


Figure 8 40-pin QFN (6 × 6 × 0.6 mm (4.6 × 4.6 mm E-Pad (Sawn))) package outline

8 Acronyms

Table 47 Acronyms used in this document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint

Acronyms

Table 47 Acronyms used in this document (continued)

Acronym	Description
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC™ pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I ² C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array

Acronyms

Table 47 Acronyms used in this document (continued)

Acronym	Description
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC™	Programmable system-on-chip
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I ² C serial clock
SDA	I ² C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block

Acronyms

Table 47 Acronyms used in this document *(continued)*

Acronym	Description
USB	Universal Serial Bus
USBIO	USB input/output, PSoC™ pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

9 Document conventions

9.1 Units of measure

Table 48 Units of measure

Symbol	Unit of measure
°C	degrees celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
MspS	meegasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision history

Revision history

Document revision	Date	Description of changes
**	2021-12-16	Initial release.
*A	2022-03-21	<p>Changed the datasheet status from Target datasheet to Datasheet (Final). Updated Electrical specifications: Updated Analog peripherals: Updated Inductive sensing: Updated Table 17. Updated System resources: Updated Power-on reset (POR): Added Note 11 and referred the same note in minimum value of SR_POWER parameter in Table 29. Updated Packaging: Updated Table 44.</p>
*B	2022-09-19	<p>Updated Block diagram: Updated Figure 2. Updated Functional definition: Updated Inductive sensing: Added SNR vs target distance. Added Distance delta (metal target displacement) when SNR = 5. Added Raw counts vs target distance. Added Noiseless precision. Added Sensitivity. Added Noise floor (%). Added Effective number of bits (ENOB). Added Scan time. Added Detection range. Updated Electrical specifications: Updated Analog peripherals: Updated Inductive sensing: Updated Table 17. Completing Sunset Review.</p>
*C	2023-03-17	<p>Updated General description: Updated description. Updated Features: Updated description. Updated Block diagram: Updated Figure 2. Updated Functional definition: Updated Inductive sensing: Updated description. Added Figure 5. Updated Pinouts: Updated description. Updated Alternate pin functions: Updated description. Updated Table 2. Updated Power: Updated Mode 2: 1.8 V ± 5% external supply: Updated Figure 7.</p>



Revision history

Document revision	Date	Description of changes
*C	2023-03-17	Updated Electrical specifications : Updated Analog peripherals : Updated Inductive sensing : Updated Table 17 . Updated Ordering information : Updated Table 42 (No change in part numbers; updated details under “Smart IOs” column). Updated to new template.

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Email:

erratum@infineon.com

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