

FQA7N90M_F109

900V N-Channel MOSFET

Features

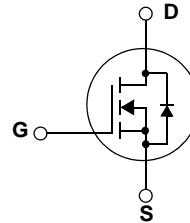
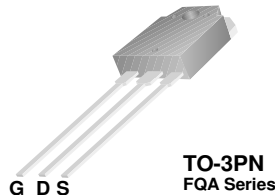
- 7.0A, 900V, $R_{DS(on)} = 1.8\Omega @ V_{GS} = 10V$
- Low gate charge (typical 40 nC)
- Low Crss (typical 17pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant



Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies, active power factor correction, electronic lamp ballast based on half bridge topology.



Absolute Maximum Ratings

Symbol	Parameter	FQA7N90M_F109	Units
V_{DSS}	Drain-Source Voltage	900	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	7.0	A
	- Continuous ($T_C = 100^\circ\text{C}$)	4.4	A
I_{DM}	Drain Current - Pulsed (Note 1)	28	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	780	mJ
I_{AR}	Avalanche Current (Note 1)	6.4	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	21	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.0	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	210	W
	- Derate above 25°C	1.69	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.59	$^\circ\text{C/W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.24	--	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	40	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQA7N90M	FQA7N90M_F109	TO-3PN	--	--	30

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units	
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	900	--	--	V	
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	--	0.96	--	V°C	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 900\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA	
		$V_{DS} = 720\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	μA	
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA	
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA	
On Characteristics							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	--	5.0	V	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 3.5\text{ A}$	--	1.5	1.8	Ω	
g_{FS}	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 3.5\text{ A}$ (Note 4)	--	5.7	--	S	
Dynamic Characteristics							
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1440	1880	pF	
C_{oss}	Output Capacitance		--	140	185	pF	
C_{rSS}	Reverse Transfer Capacitance		--	17	23	pF	
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 450\text{ V}, I_D = 7.0\text{ A},$ $R_G = 25\ \Omega$	--	35	80	ns	
t_r	Turn-On Rise Time		--	80	170	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4, 5)	--	95	200	ns
t_f	Turn-Off Fall Time		--	55	120	ns	
Q_g	Total Gate Charge	$V_{DS} = 720\text{ V}, I_D = 7.0\text{ A},$ $V_{GS} = 10\text{ V}$	--	40	52	nC	
Q_{gs}	Gate-Source Charge		(Note 4, 5)	--	8.5	--	nC
Q_{gd}	Gate-Drain Charge		--	20	--	nC	
Drain-Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	6.4	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	25.6	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 7.0\text{ A}$	--	--	1.4	V	
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 7.0\text{ A},$ $dI_F / dt = 100\text{ A}/\mu\text{s}$	--	400	--	ns	
Q_{rr}	Reverse Recovery Charge		(Note 4)	--	4.3	--	μC

NOTES:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 30\text{ mH}, I_{AS} = 7.0\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 7.0\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Performance Characteristics

Figure 1. On-Region Characteristics

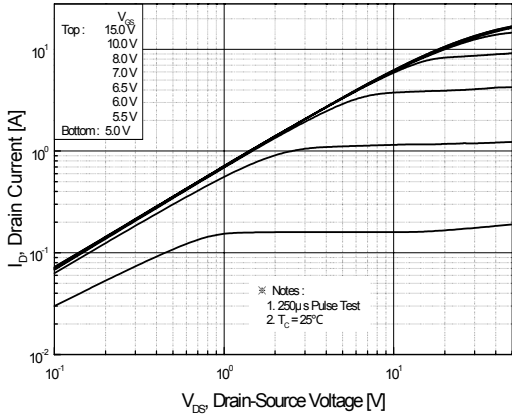


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

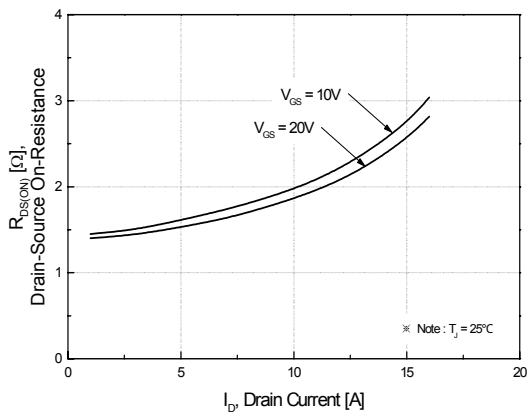


Figure 5. Capacitance Characteristics

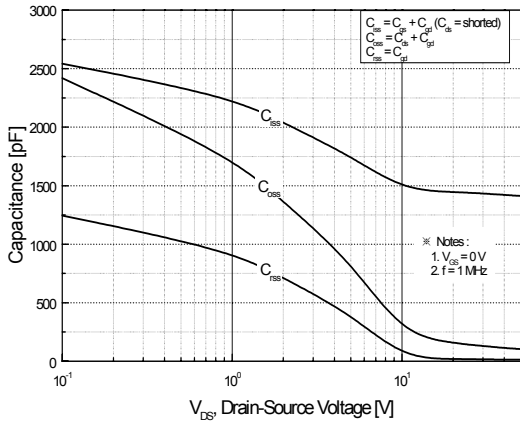


Figure 2. Transfer Characteristics

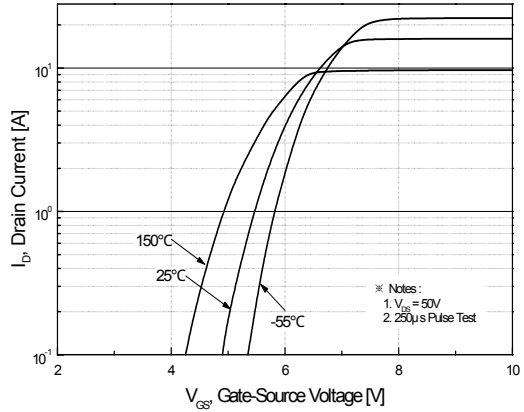


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

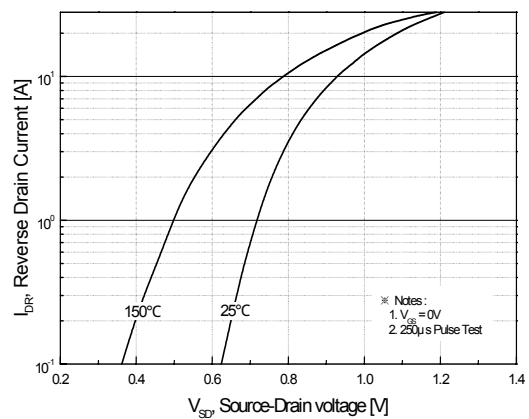
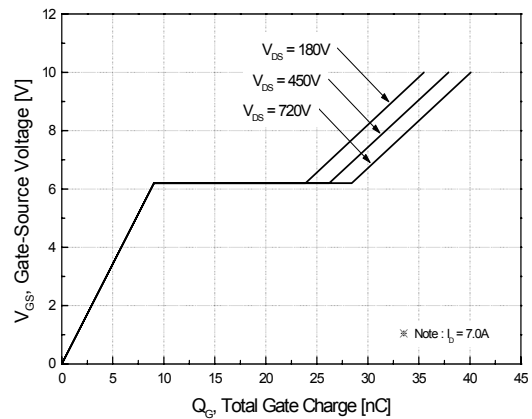


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

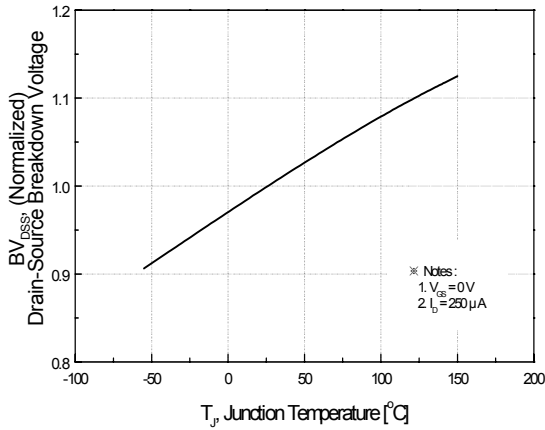


Figure 8. On-Resistance Variation vs. Temperature

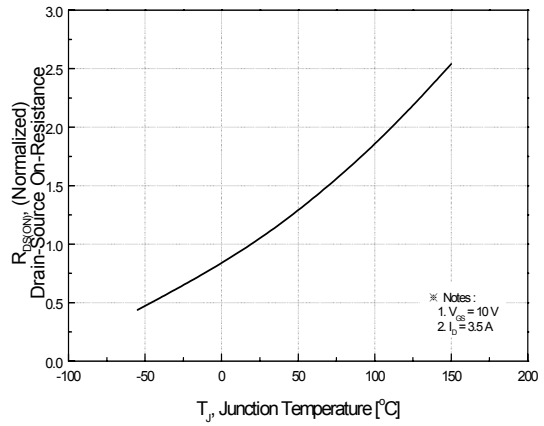


Figure 9. Maximum Safe Operating Area

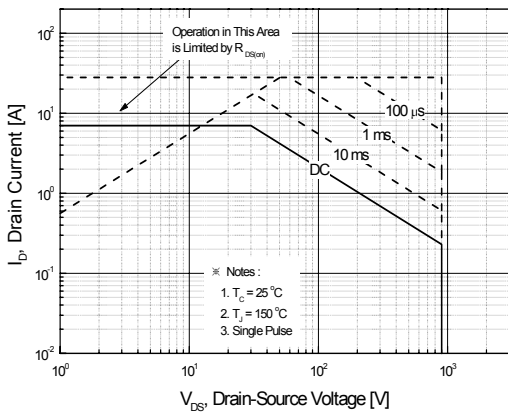


Figure 10. Maximum Drain Current vs. Case Temperature

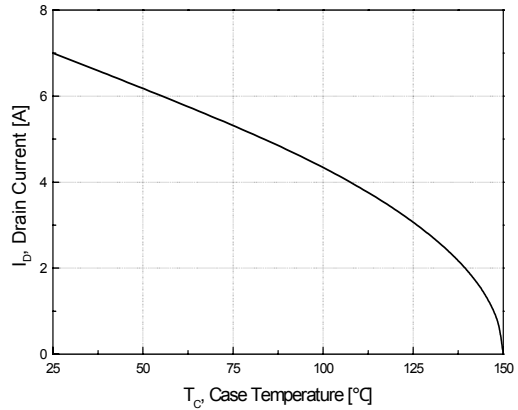
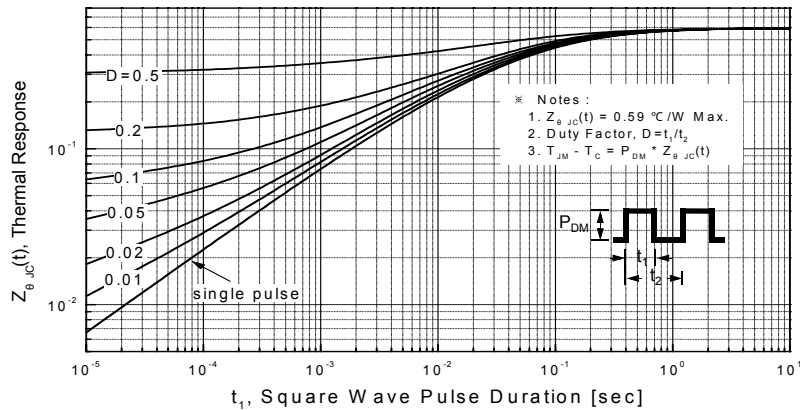


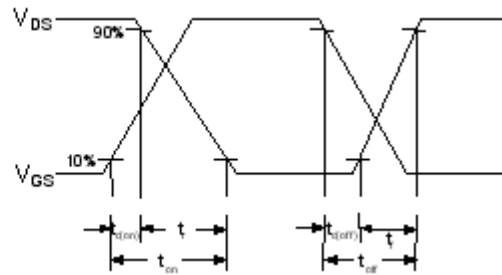
Figure 11. Transient Thermal Response Curve



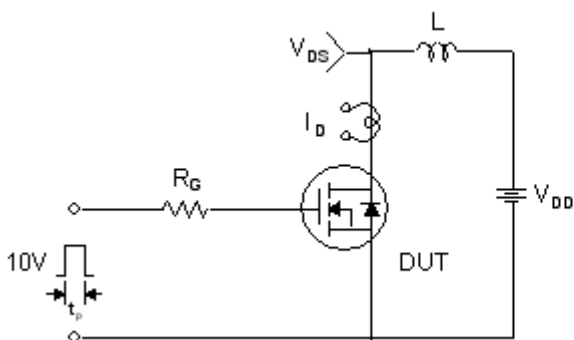
Gate Charge Test Circuit & Waveform



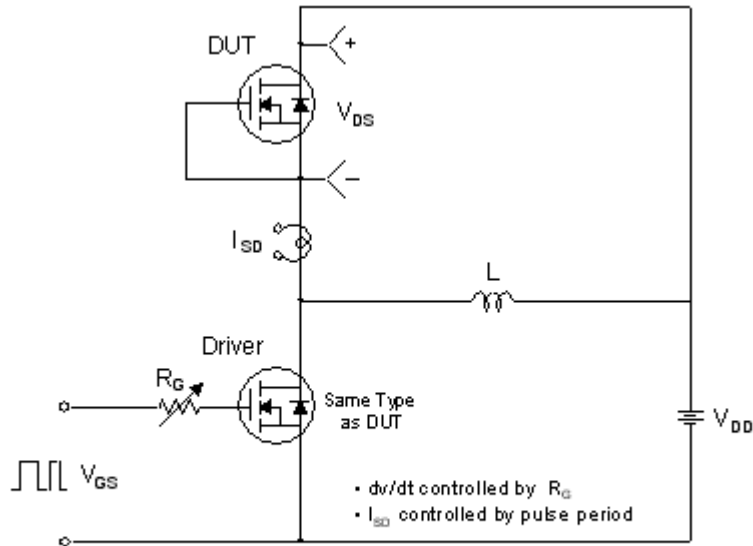
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

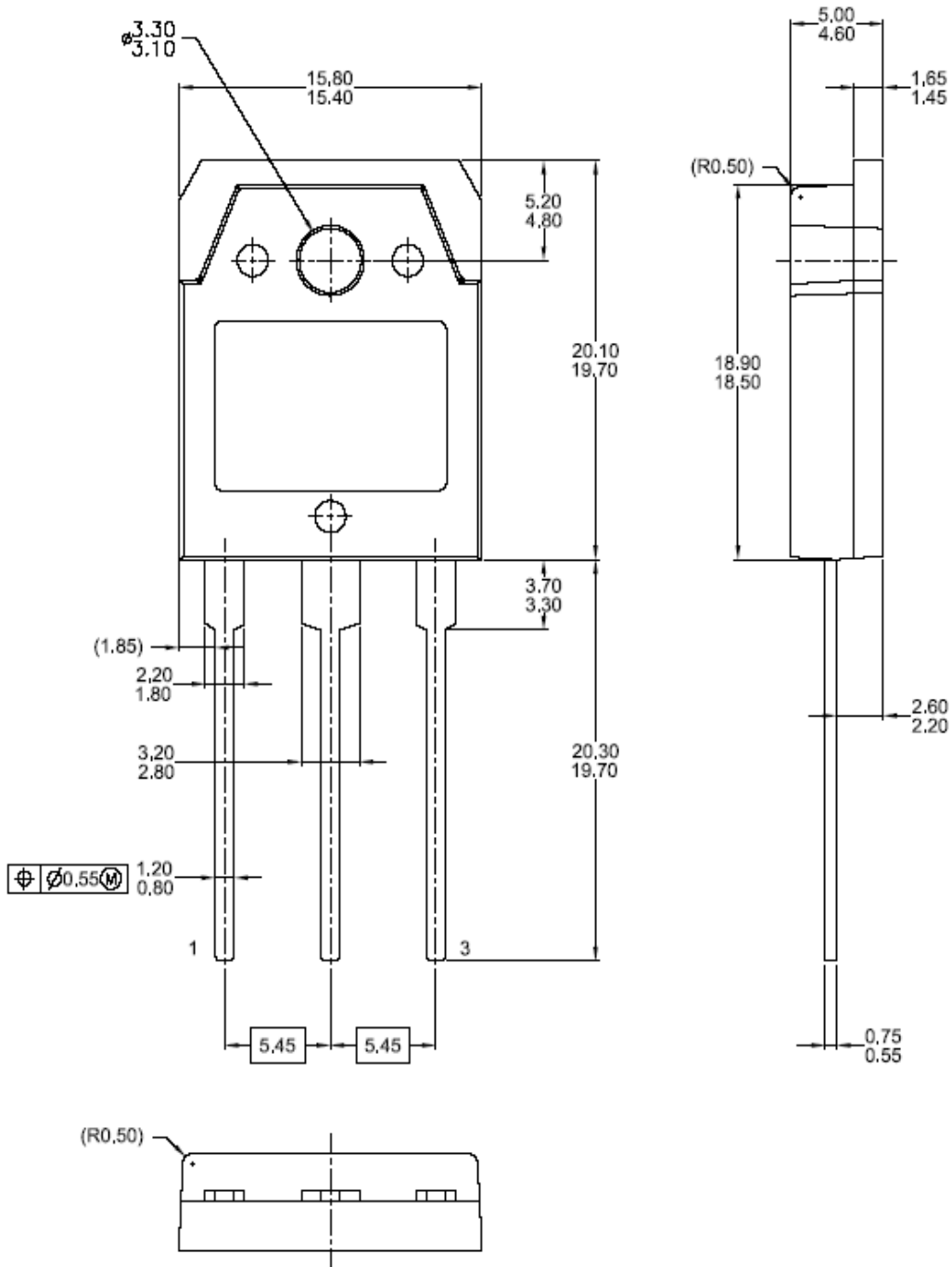


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-3PN




Dimensions in Millimeters



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Rev. I31