

## CMOS Programmable Timer

High-Voltage Types (20-Volt Rating)

■ CD4536B is a programmable timer consisting of 24 ripple-binary counter stages. The salient feature of this device is its flexibility. The device can count from 1 to  $2^{24}$  or the first 8 stages can be bypassed to allow an output, selectable by a 4-bit code, from any one of the remaining 16 stages. It can be driven by an external clock or an RC oscillator that can be constructed using on-chip components. Input IN1 serves as either the external clock input or the input to the on-chip RC oscillator. OUT1 and OUT2 are connection terminals for the external RC components. In addition, an on-chip monostable circuit is provided to allow a variable pulse width output. Various timing functions can be achieved using combinations of these capabilities.

A logic 1 on the 8-BYPASS input enables a bypass of the first 8 stages and makes stage 9 the first counter stage of the last 16 stages. Selection of 1 of 16 outputs is accomplished by the decoder and the BCD inputs A, B, C and D. MONO IN is the timing input for the on-chip monostable oscillator. Grounding of the MONO IN terminal through a resistor of 10K ohms or higher, disables the one-shot circuit and connects the decoder directly to the DECODE OUT terminal. A resistor to  $V_{DD}$  and a capacitor to ground from the MONO IN terminal enables the one-shot circuit and controls its pulse width.

A fast test mode is enabled by a logic 1 on 8-BYPASS, SET, and RESET. This mode

### Features:

- 24 flip-flop stages — counts from  $2^0$  to  $2^{24}$
- Last 16 stages selectable by BCD select code.
- Bypass input allows bypassing first 8 stages
- On-chip RC oscillator provision
- Clock inhibit input
- Schmitt-trigger in clock line permits operation with very long rise and fall times
- On-chip monostable output provision
- Typical  $f_{CL} = 3$  MHz at  $V_{DD} = 10$  V
- Test mode allows fast test sequence
- Set and reset inputs
- Capable of driving two low power TTL loads, one lower-power Schottky load, or two HTL loads over the rated temperature range
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

divides the 24-stage counter into three 8-stage sections to facilitate a fast test sequence.

The CD4536B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (DW, DWR, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

### MAXIMUM RATINGS, Absolute-Maximum Values:

#### DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )

Voltages referenced to  $V_{SS}$  Terminal ..... -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to  $V_{DD} + 0.5V$

DC INPUT CURRENT, ANY ONE INPUT .....  $\pm 10$  mA

#### POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For  $T_A = -55^\circ\text{C}$  to  $+100^\circ\text{C}$  ..... 500mW

For  $T_A = +100^\circ\text{C}$  to  $+125^\circ\text{C}$  ..... Derate Linearly at 12mW/ $^\circ\text{C}$  to 200mW

#### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

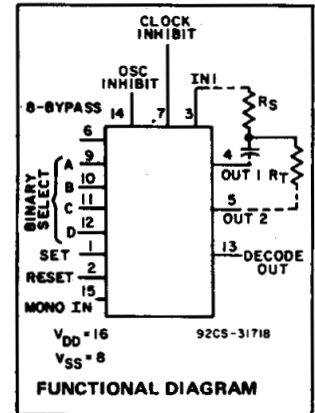
FOR  $T_A =$  FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW

OPERATING-TEMPERATURE RANGE ( $T_A$ ) .....  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE ( $T_{stg}$ ) .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

#### LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16  $\pm$  1/32 inch (1.59  $\pm$  0.79mm) from case for 10s max .....  $+285^\circ\text{C}$



### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For $T_A =$ Full Package Temperature Range)	3	18	V

### DECODE OUT SELECTION TABLE

D	C	B	A	NUMBER OF STAGES IN DIVIDER CHAIN	
				8-BYPASS = 0	8-BYPASS = 1
				0	0
0	0	0	1	10	2
0	0	1	0	11	3
0	0	1	1	12	4
0	1	0	0	13	5
0	1	0	1	14	6
0	1	1	0	15	7
0	1	1	1	16	8
1	0	0	0	17	9
1	0	0	1	18	10
1	0	1	0	19	11
1	0	1	1	20	12
1	1	0	0	21	13
1	1	0	1	22	14
1	1	1	0	23	15
1	1	1	1	24	16

0 = Low Level    1 = High Level

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

# CD4536B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	-	0,5	5	5	5	150	150	-	0,04	5	μA
	-	0,10	10	10	10	300	300	-	0,04	10	
	-	0,15	15	20	20	600	600	-	0,04	20	
	-	0,20	20	100	100	3000	3000	-	0,08	100	
Output Low (Sink) Current I <sub>OL</sub> Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	-	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	-	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	-	
Output High (Source) Current, I <sub>OH</sub> Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	-	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	-	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	-	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	-	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	-	0,5	5	0,05				-	0	0,05	V
	-	0,10	10	0,05				-	0	0,05	
	-	0,15	15	0,05				-	0	0,05	
Output Voltage: High-Level, V <sub>OH</sub> Min.	-	0,5	5	4,95				4,95	5	-	V
	-	0,10	10	9,95				9,95	10	-	
	-	0,15	15	14,95				14,95	15	-	
Input Low Voltage V <sub>IL</sub> Max.	0,5,4,5	-	5	1,5				-	-	1,5	V
	1,9	-	10	3				-	-	3	
	1,5,13,5	-	15	4				-	-	4	
Input High Voltage V <sub>IH</sub> Min.	0,5,4,5	-	5	3,5				3,5	-	-	V
	1,9	-	10	7				7	-	-	
	1,5,13,5	-	15	11				11	-	-	
Input Current I <sub>IN</sub> Max.	-	0,18	18	±0,1	±0,1	±1	±1	-	±10 <sup>-5</sup>	±0,1	μA

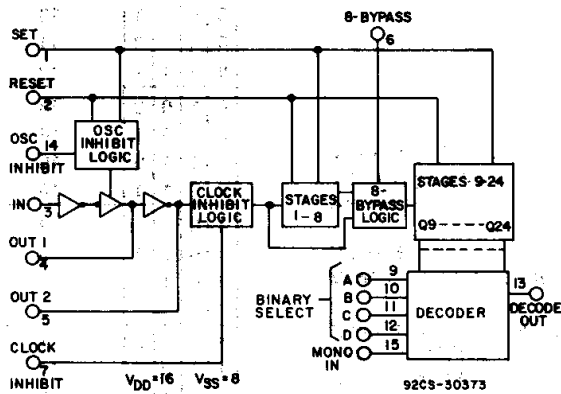


Fig. 1 - Functional block diagram.

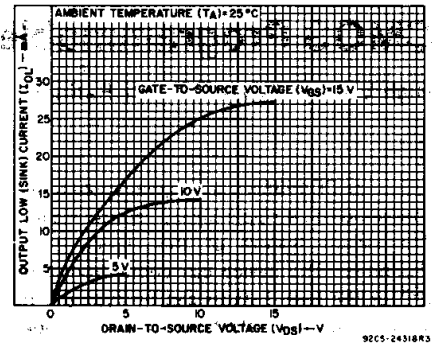


Fig. 2 - Typical output low (sink) current characteristics.

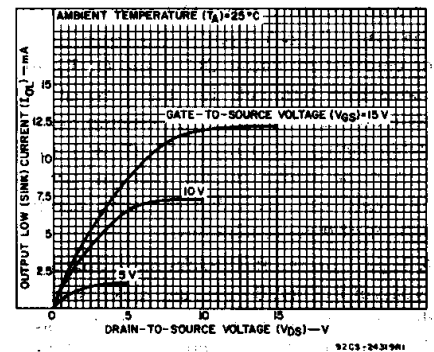


Fig. 3 - Minimum output low (sink) current characteristics.

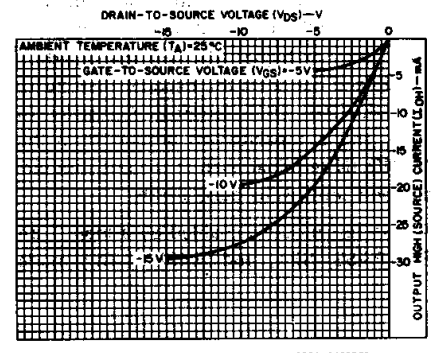


Fig. 4 - Typical output high (source) current characteristics.

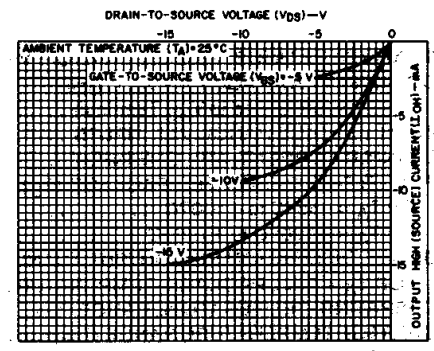


Fig. 5 - Minimum output high (source) current characteristics.

# CD4536B Types

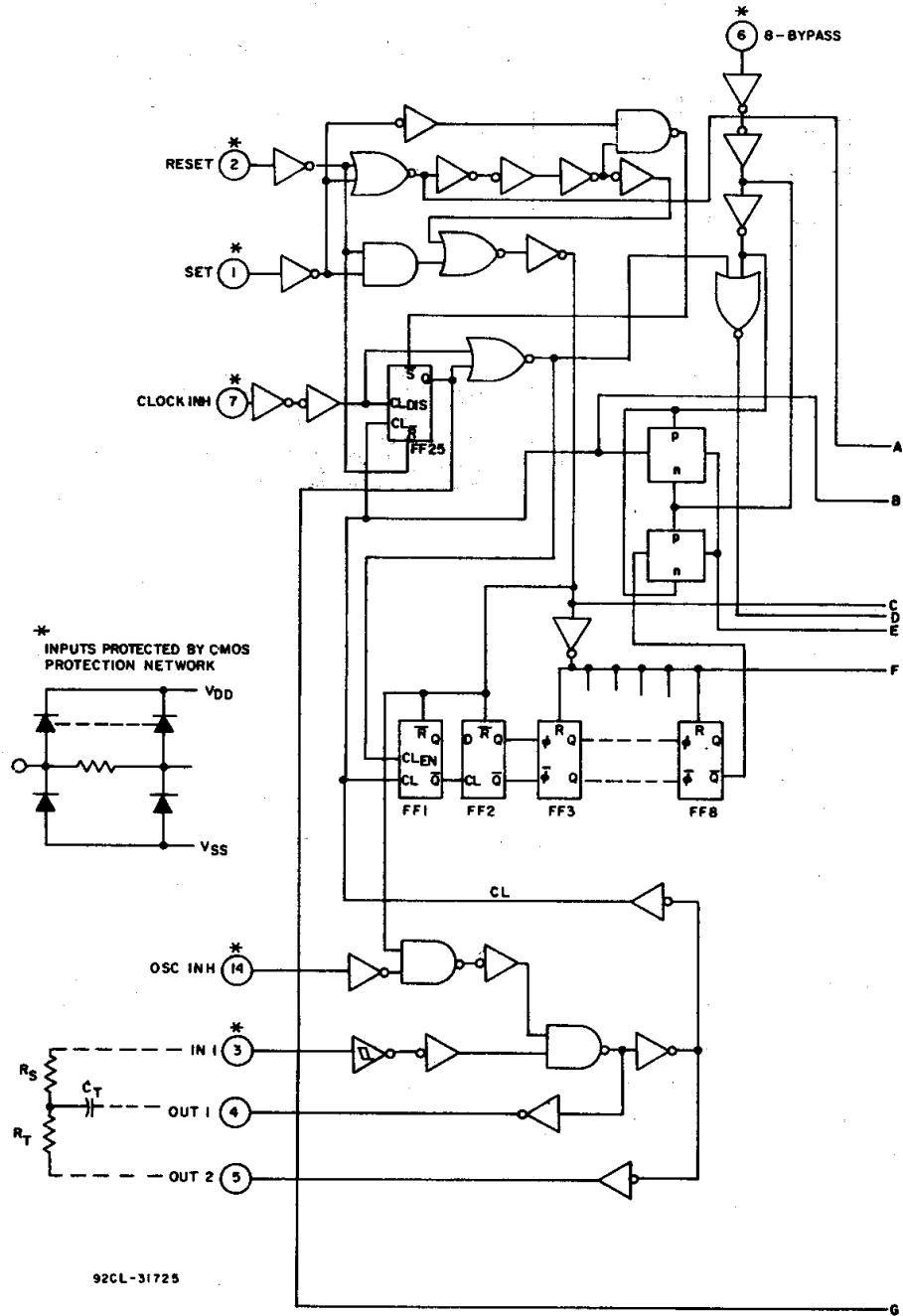


Fig.6 - Logic diagram for CD4536B [continued on next page].

NOTE:  $f \approx \frac{1}{3R_T C_T}$ ,  $R_S \approx (5 \rightarrow 10) \times R_T$

# CD4536B Types

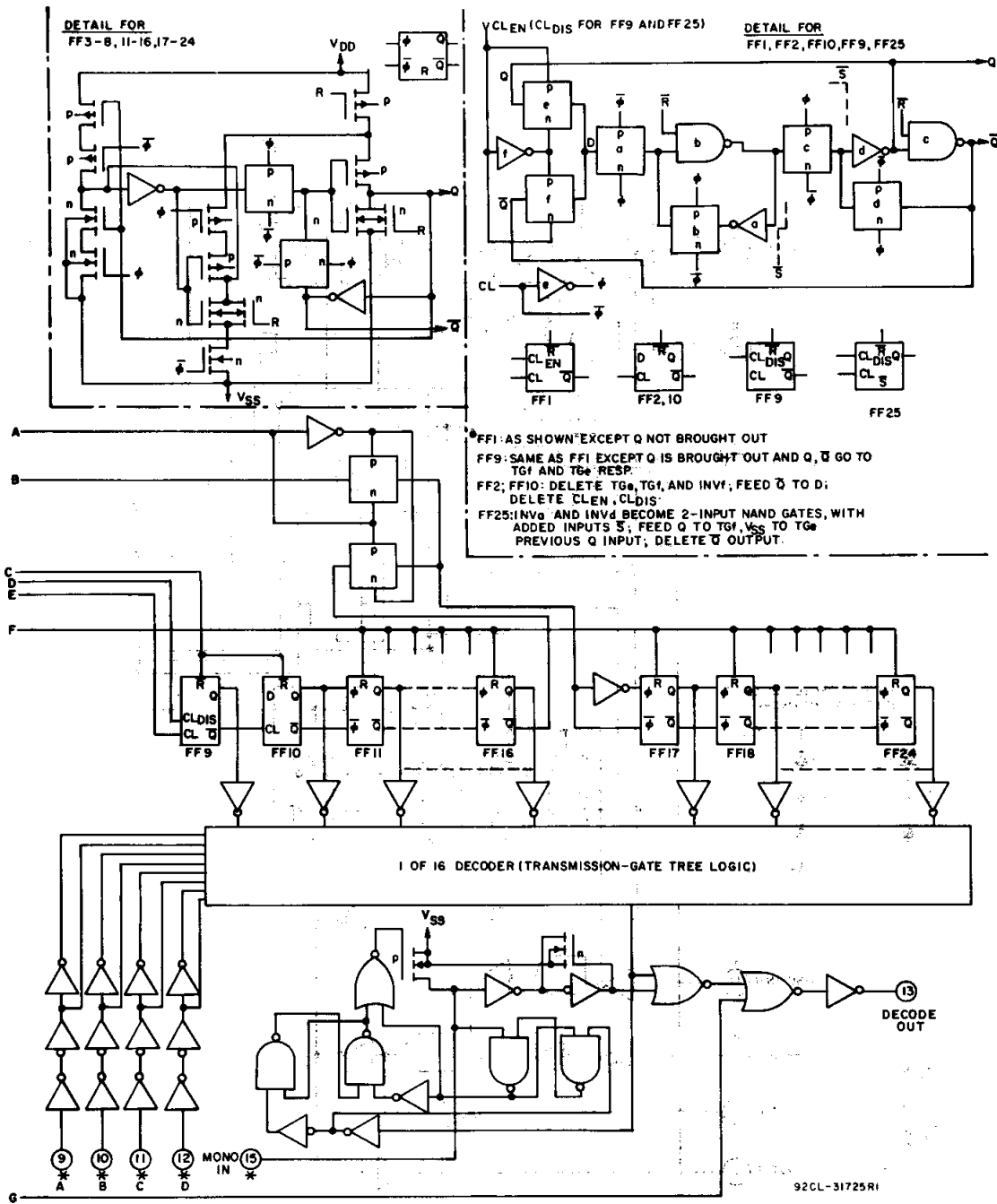
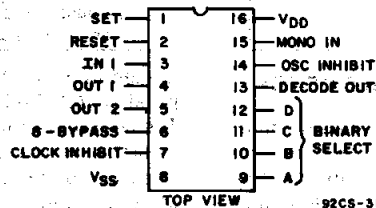


Fig.6 - Logic diagram for CD4536B [continued from previous page].

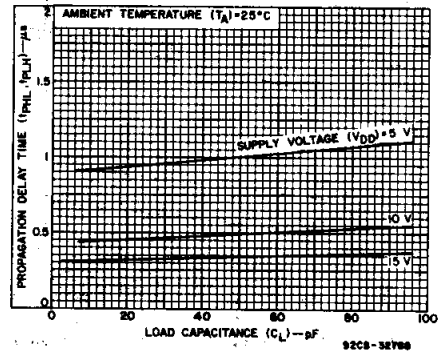
# CD4536B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS, at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$**

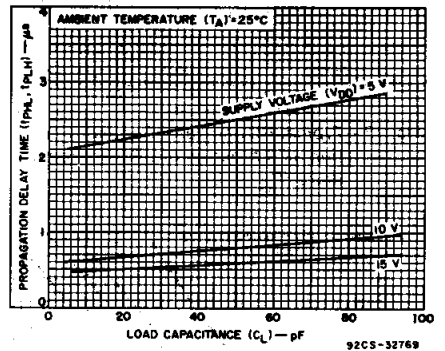
CHARACTERISTIC	V <sub>DD</sub> (V)	LIMITS			UNITS
		Min.	Typ.	Max.	
Propagation Delay Times:	5	—	1	2	$\mu\text{s}$
Clock to Q1, 8-Bypass High	10	—	0.5	1	
$t_{PHL}, t_{PLH}$	15	—	0.35	0.7	
Clock to Q1, 8-Bypass Low	5	—	2.5	5	$\mu\text{s}$
$t_{PHL}, t_{PLH}$	10	—	0.8	1.6	
$t_{PHL}, t_{PLH}$	15	—	0.6	1.2	
Clock to Q16, $T_{PHL}, t_{PLH}$	5	—	4	8	$\mu\text{s}$
$T_{PHL}, t_{PLH}$	10	—	1.5	3	
$T_{PHL}, t_{PLH}$	15	—	1	2	
$Q_n$ to $Q_{n+1}$ , $t_{PHL}, t_{PLH}$	5	—	150	300	ns
$t_{PHL}, t_{PLH}$	10	—	75	150	
$t_{PHL}, t_{PLH}$	15	—	50	100	
Set to $Q_n$ , $t_{PLH}$	5	—	300	600	ns
$t_{PLH}$	10	—	125	250	
$t_{PLH}$	15	—	80	160	
Reset to $Q_n$ , $t_{PHL}$	5	—	3	6	$\mu\text{s}$
$t_{PHL}$	10	—	1	2	
$t_{PHL}$	15	—	0.75	1.5	
Transition Time, $t_{THL}, t_{TLH}$	5	—	100	200	ns
$t_{THL}, t_{TLH}$	10	—	50	100	
$t_{THL}, t_{TLH}$	15	—	40	80	
Minimum Pulse Widths:	5	—	200	400	ns
Clock	10	—	75	150	
Clock	15	—	50	100	
Set	5	—	200	400	ns
Set	10	—	100	200	
Set	15	—	60	120	
Reset	5	—	3	6	$\mu\text{s}$
Reset	10	—	1	2	
Reset	15	—	0.75	1.5	
Minimum Set Recovery Time,	5	—	2.5	5	$\mu\text{s}$
Minimum Set Recovery Time,	10	—	1	2	
Minimum Set Recovery Time,	15	—	0.6	1.6	
Minimum Reset Recovery Time,	5	—	3.5	7	$\mu\text{s}$
Minimum Reset Recovery Time,	10	—	1.5	3	
Minimum Reset Recovery Time,	15	—	1	2	
Maximum Clock Pulse Input Frequency, $f_{CL}$	5	0.5	1	—	MHz
$f_{CL}$	10	1.5	3	—	
$f_{CL}$	15	2.5	5	—	
Maximum Clock Pulse Input Rise or Fall Time, $t_r, t_f$	5, 10, 15	Unlimited			$\mu\text{s}$



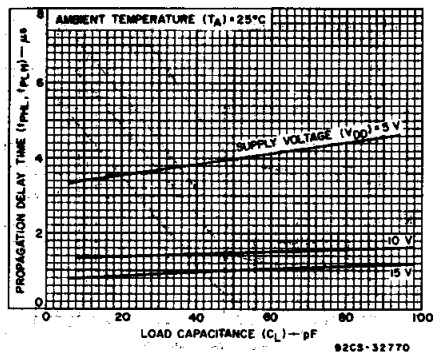
**Terminal Assignment**



**Fig. 7—Typical propagation delay time as a function of load capacitance (CLOCK to Q1, 8-BYPASS high).**



**Fig. 8—Typical propagation delay time as a function of load capacitance (CLOCK to Q1, 8-BYPASS low).**



**Fig. 9—Typical propagation delay time as a function of load capacitance (CLOCK to Q16, 8-BYPASS high).**

**3**  
**COMMERCIAL CMOS**  
**HIGH VOLTAGE ICs**

# CD4536B Types

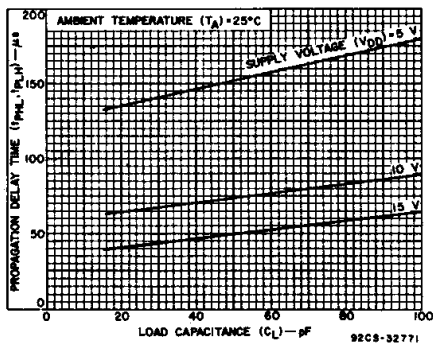


Fig. 10—Typical propagation delay time as a function of load capacitance ( $Q_N$  to  $Q_{N+1}$ ).

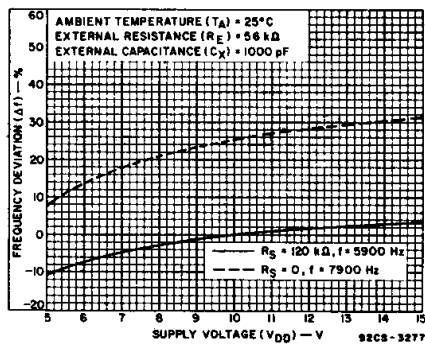


Fig. 11—Typical RC oscillator frequency deviation as a function of supply voltage.

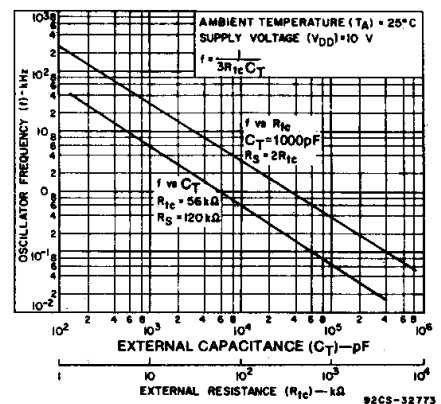


Fig. 12—Typical RC oscillator frequency deviation as a function of time constant resistance and capacitance.

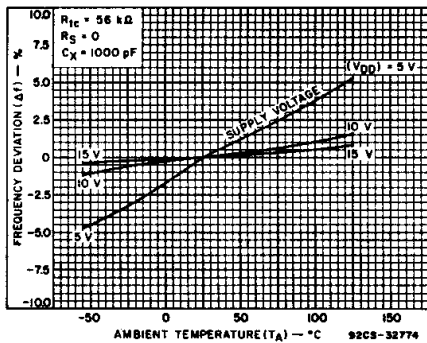


Fig. 13—Typical RC oscillator frequency deviation as a function of ambient temperature ( $R_S = 0$ ).

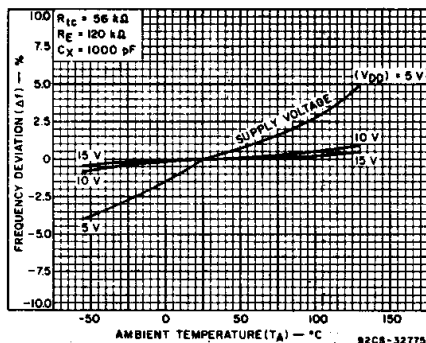


Fig. 14—Typical RC oscillator frequency deviation as a function of ambient temperature ( $R_S = 120$  kΩ).

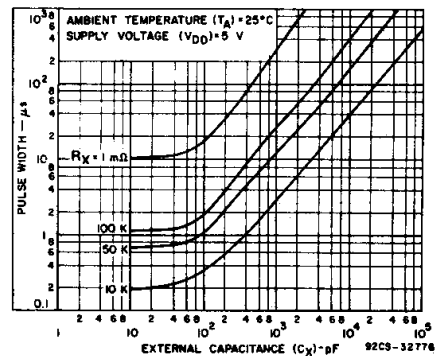


Fig. 15—Typical pulse width as a function of external capacitance ( $V_{DD} = 5$  V).

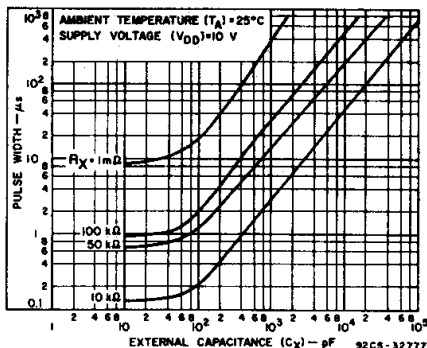


Fig. 16—Typical pulse width as a function of external capacitance ( $V_{DD} = 10$  V).

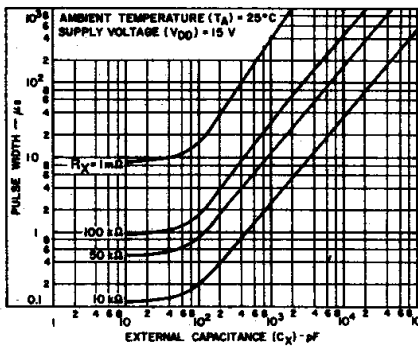


Fig. 17—Typical pulse width as a function of external capacitance ( $V_{DD} = 15$  V).

Functional Test Sequence					
Inputs				Outputs	Comments
In <sub>1</sub>	Set	Reset	8-Bypass	Decode Out Q1 thru Q24	
1	0	1	1	0	All 24 steps are in Reset mode
1	1	1	1	0	
0	1	1	1	0	Counter is in three 8-stage section in parallel mode
1	0	1	1	0	First "1" to "0" transition of clock
0	1	1	1	0	255 "1" to "0" transitions are clocked in the counter
0	0	0	0	1	
0	0	0	0	1	The 255 "1" to "0" transition Counter converted back to 24 stages in series mode
1	0	0	0	1	Set and Reset must be connected together and simultaneously go from "1" to "0"
0	0	0	0	0	In <sub>1</sub> Switches to a "1"
0	0	0	0	0	Counter Ripples from an all "1" state to an all "0" state

## FUNCTIONAL TEST SEQUENCE

Test Function (Figure 23) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections and 255 counts are

loaded in each of the 8-stage sections in parallel. All flip-flops are now at a "1". The counter is now returned to the normal 24-steps in series configuration. One more pulse is entered into In<sub>1</sub> which will cause the counter to ripple from an all "1" state to an all "0" state.

# CD4536B Types

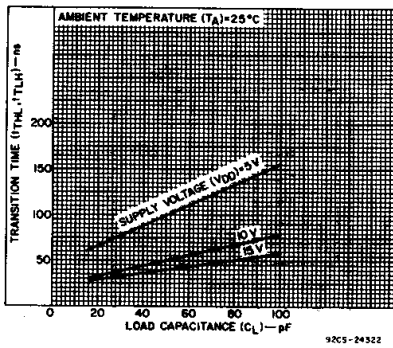


Fig. 18—Typical transition time as a function of load capacitance.

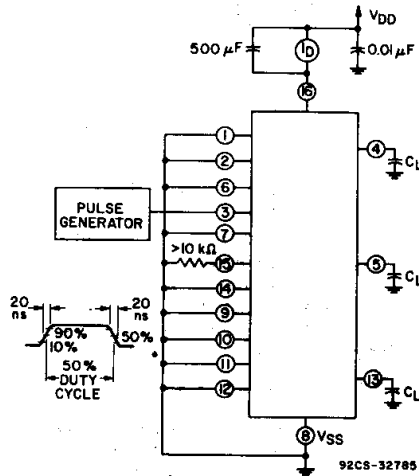
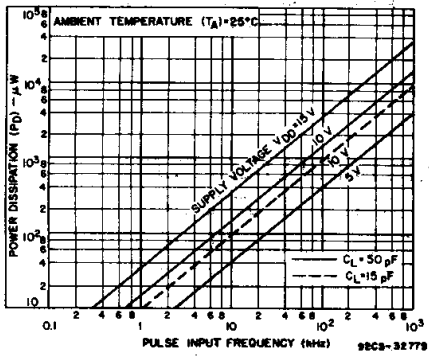


Fig. 20—Dynamic power dissipation test circuit and waveform.



19—Typical dynamic power dissipation as a function of input pulse frequency.

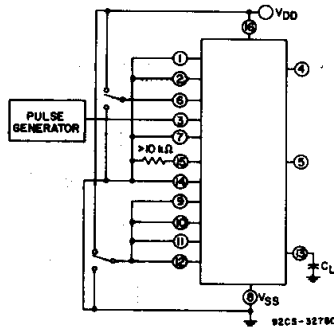


Fig. 21—Switching time test circuit.

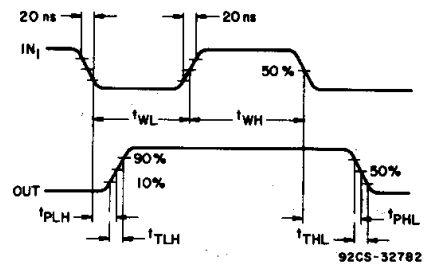


Fig. 22—Input waveforms for switching-time test circuit.

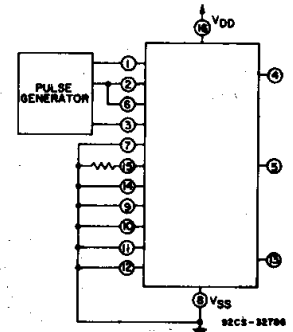


Fig. 23—Functional test circuit.

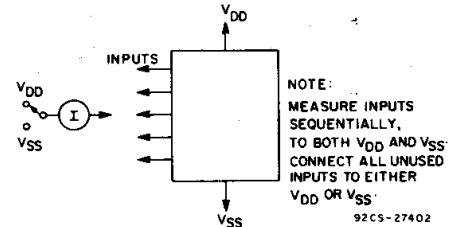


Fig. 24—Input-current test circuit.

## TRUTH TABLE

IN1	SET	RESET	CLOCK INH	OSC INH	OUT1	OUT2	DECODE OUT
	0	0	0	0			No Change
	0	0	0	0			Advance to Next State
X	1	0	0	0	0	1	1
X	0	1	0	0	0	1	0
X	0	0	1	0			No Change
0	0	0	0	X	0	1	No Change
1	0	0	0				Advance to Next State

0 = Low Level    1 = High Level    X = Don't Care

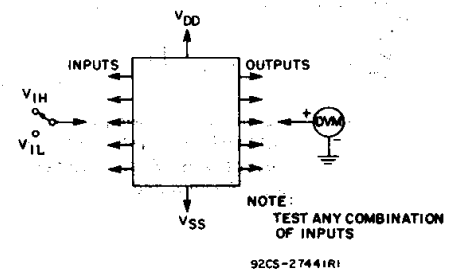


Fig. 25—Input-voltage test circuit.

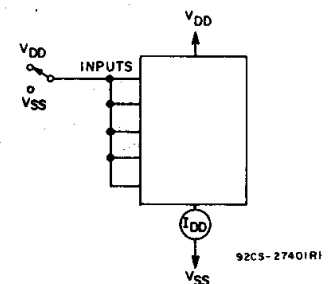


Fig. 26—Quiescent-device current test circuit.

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

# CD4536B Types

## APPLICATIONS

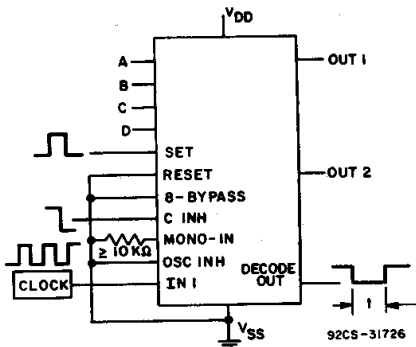


Fig. 27—Time interval configuration using external clock; set and clock inhibit functions.

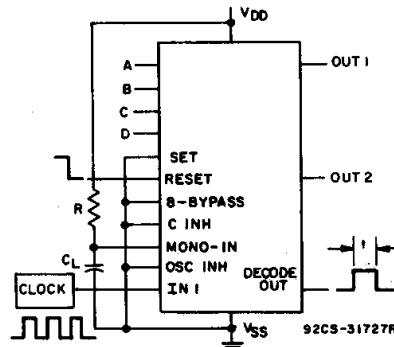


Fig. 28—Time interval configuration using external clock; reset and output monostable to achieve a pulse output.

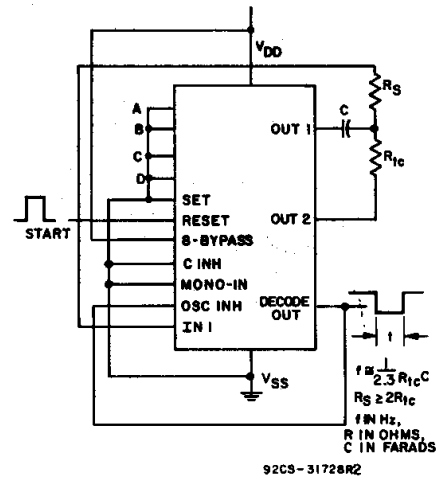


Fig. 29—Time interval configuration using on-chip RC oscillator and reset input to initiate time interval.

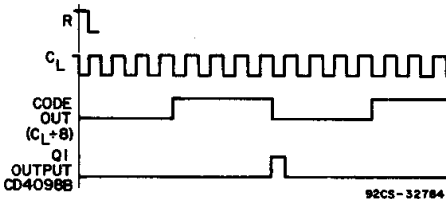
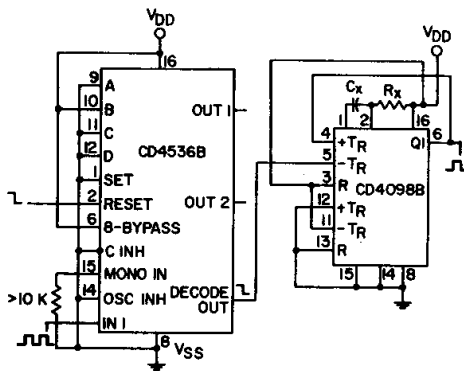
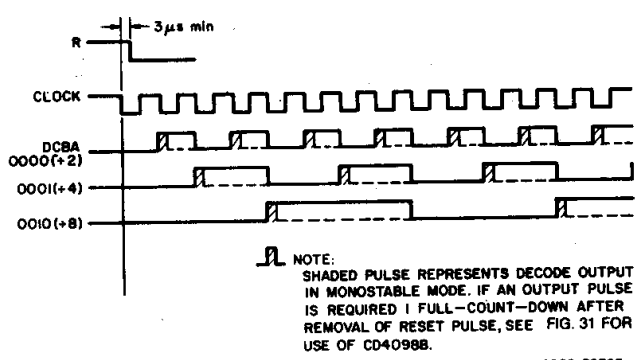


Fig. 30—Application showing use of CD4098B and CD4536B to get decode pulse 8 clock pulses after Reset pulse.

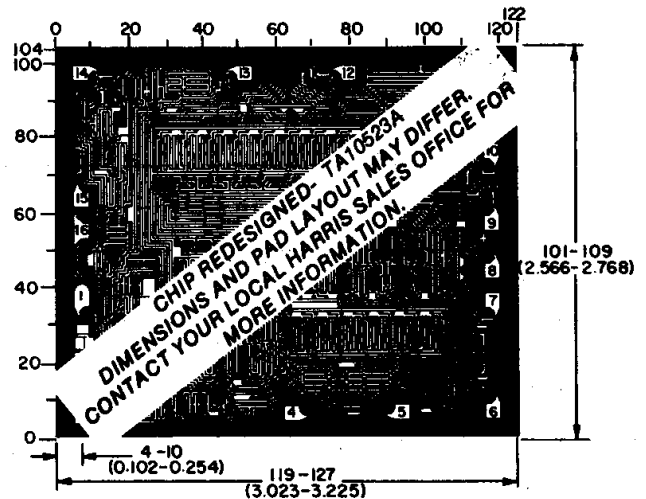


NOTE:  
SHADED PULSE REPRESENTS DECODE OUTPUT IN MONOSTABLE MODE. IF AN OUTPUT PULSE IS REQUIRED 1 FULL-COUNT-DOWN AFTER REMOVAL OF RESET PULSE, SEE FIG. 31 FOR USE OF CD4098B.

Fig. 31—CD4536B Timing Diagram.

Dimensions and pad layout for CD4536BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).



92CM-32787



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4536BDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4536BM	<a href="#">Samples</a>
CD4536BDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4536BM	<a href="#">Samples</a>
CD4536BE	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-55 to 125	CD4536BE	<a href="#">Samples</a>
CD4536BEE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-55 to 125	CD4536BE	<a href="#">Samples</a>
CD4536BF3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	CD4536BF3A	<a href="#">Samples</a>
CD4536BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4536B	<a href="#">Samples</a>
CD4536BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM536B	<a href="#">Samples</a>
CD4536BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM536B	<a href="#">Samples</a>
CD4536BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM536B	<a href="#">Samples</a>
CD4536BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM536B	<a href="#">Samples</a>
CD4536BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM536B	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD4536B, CD4536B-MIL :**

- Catalog: [CD4536B](#)
- Military: [CD4536B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4536BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
CD4536BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4536BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4536BDWR	SOIC	DW	16	2000	350.0	350.0	43.0
CD4536BNSR	SO	NS	16	2000	367.0	367.0	38.0
CD4536BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

# PW0016A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220204/A 02/2017

### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

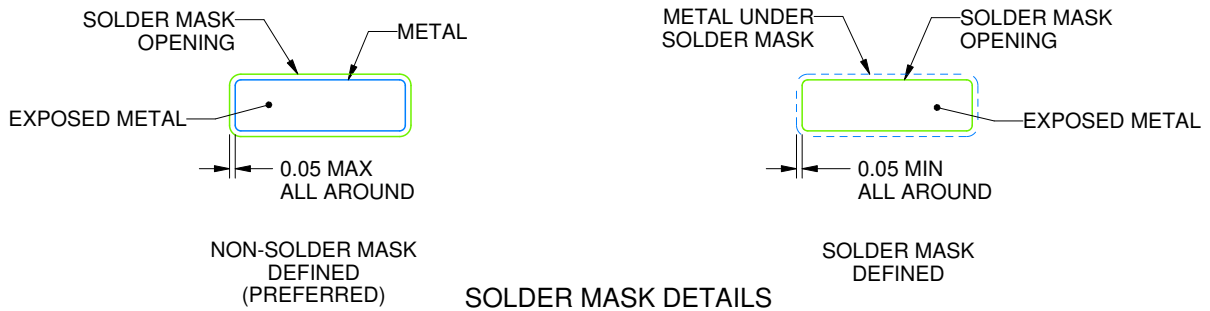
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



## GENERIC PACKAGE VIEW

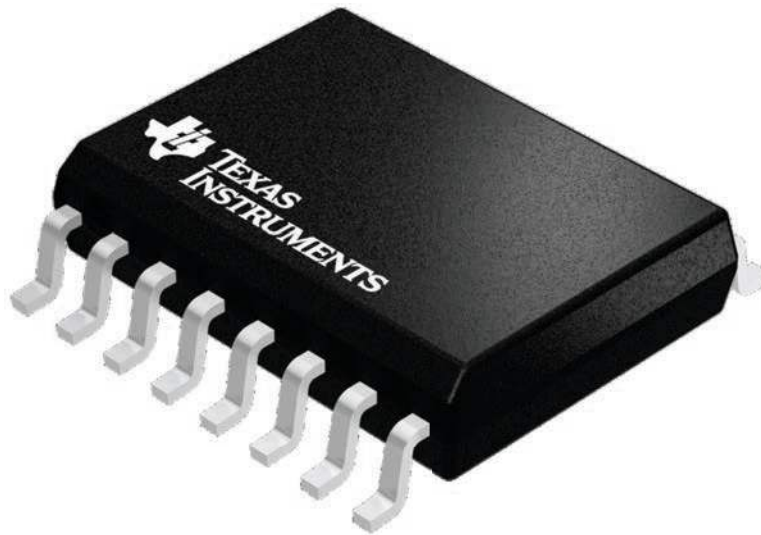
**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



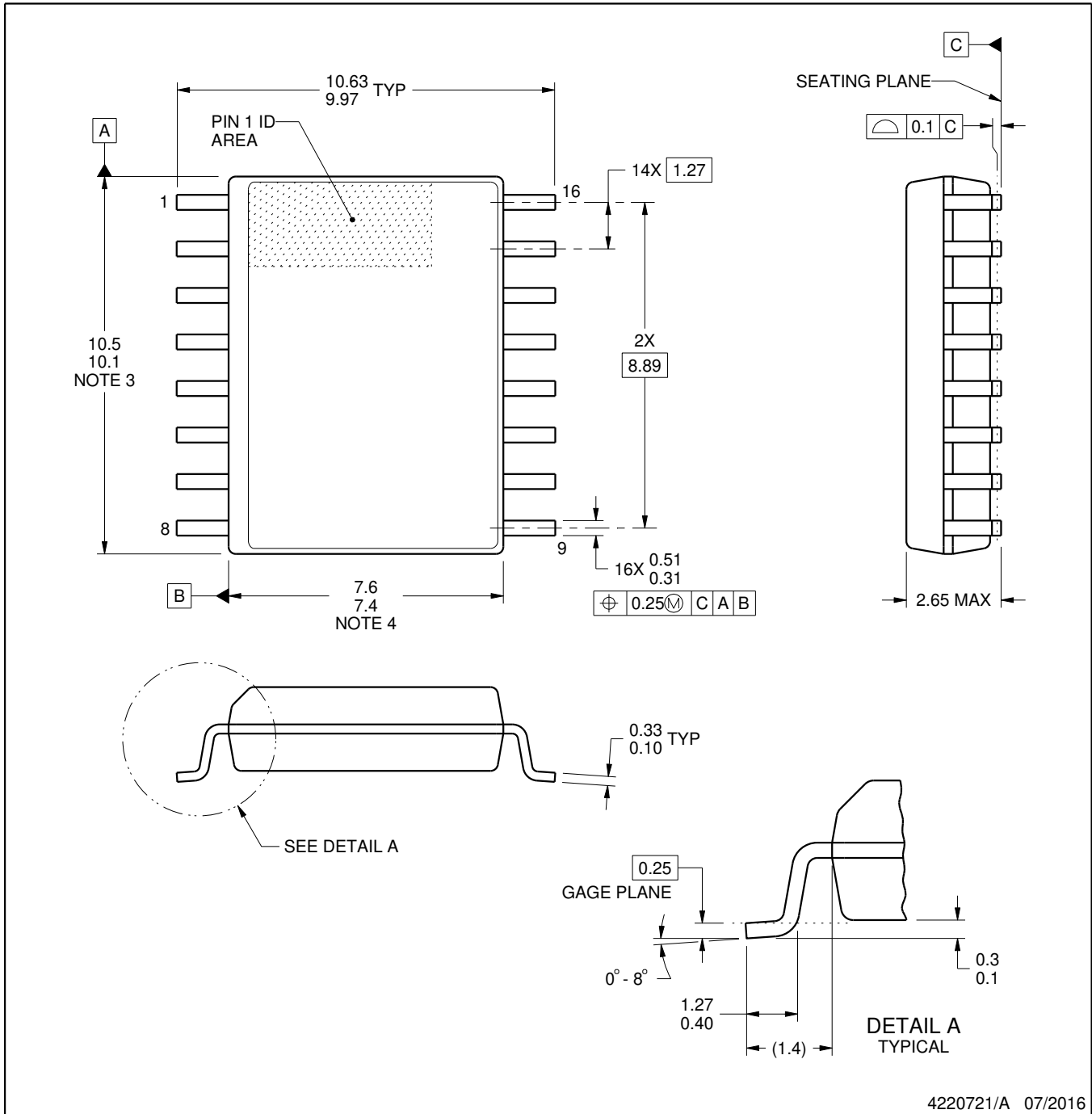
4224780/A



# DW0016A

# PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

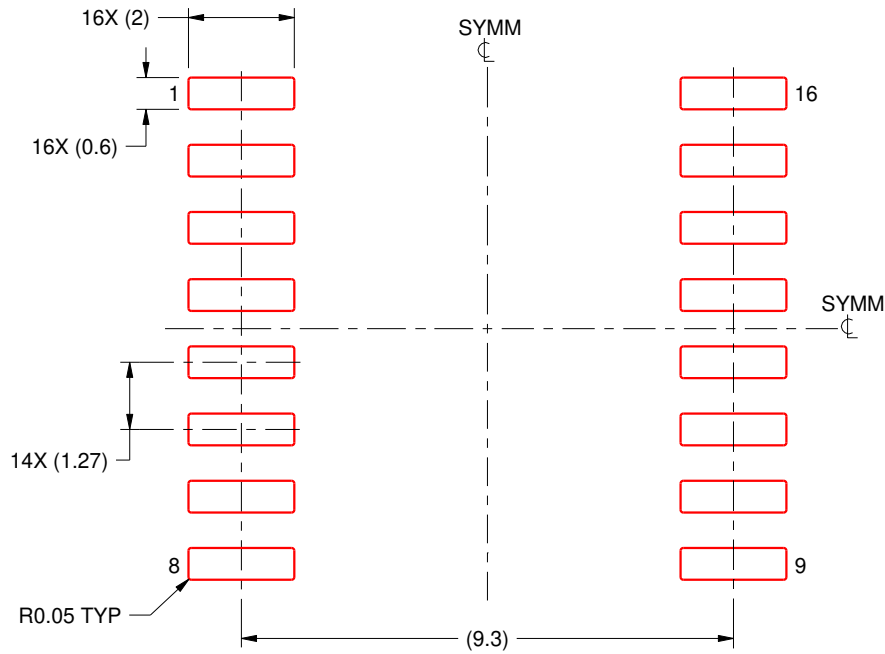


# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated