PC MAIN CLOCK ICS9UMS9610

## Recommended Application:

Poulsbo Based Ultra-Mobile PC (UMPC) - CK610

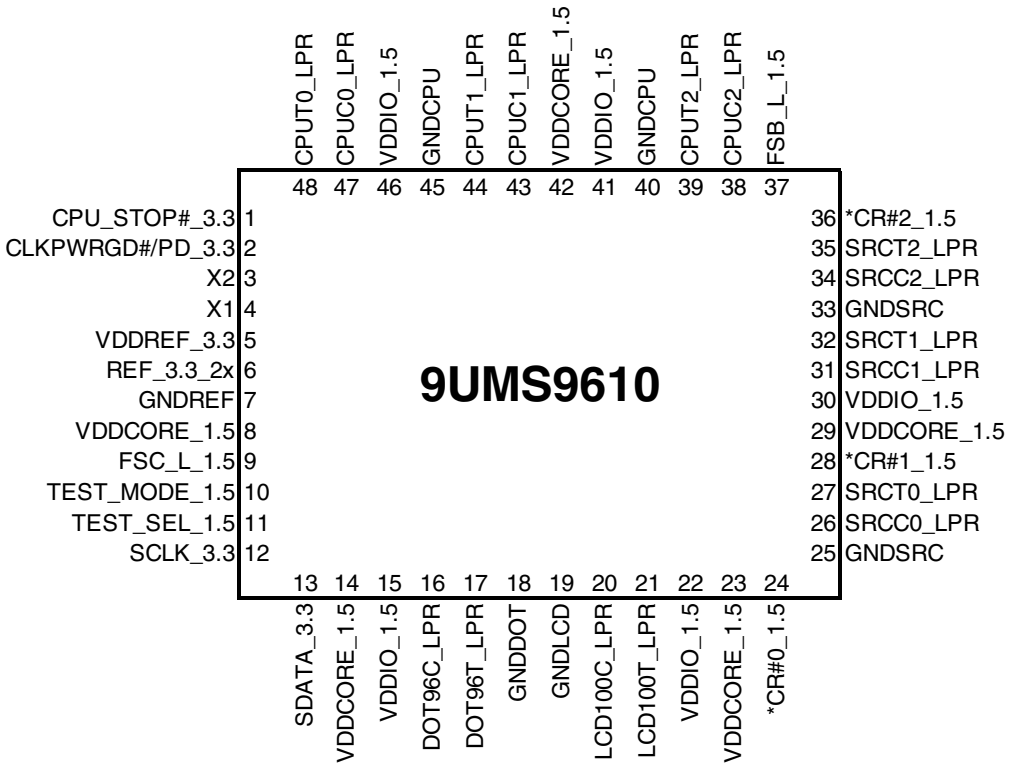
## Output Features:

- 3 - CPU low power differential push-pull pairss
- 3 - SRC low power differential push-pull pairs
- 1 - LCD100 SSCD low power differential push-pull pair
- 1 - DOT96 low power differential push-pull pair
- 1 - REF, 14.31818MHz, 3.3V SE output

## Features/Benefits:

- Supports Dothan ULV CPUs with 100 to 200 MHz CPU outputs
- Dedicated TEST/SEL and TEST/MODE pins saves isolation resistors on pins
- CPU STOP# input for power manangment
- Fully integrated Vreg
- Integrated series resistors on differential outputs
- 1.5V VDD IO, 1.5V VDD core, 3.3V VDD supply pin for REF

## Pin Configuration




**48-pin MLF, 6x6 mm, 0.4mm pitch**

* indicates inputs with internal pull up of ~10Kohm to 1.5V

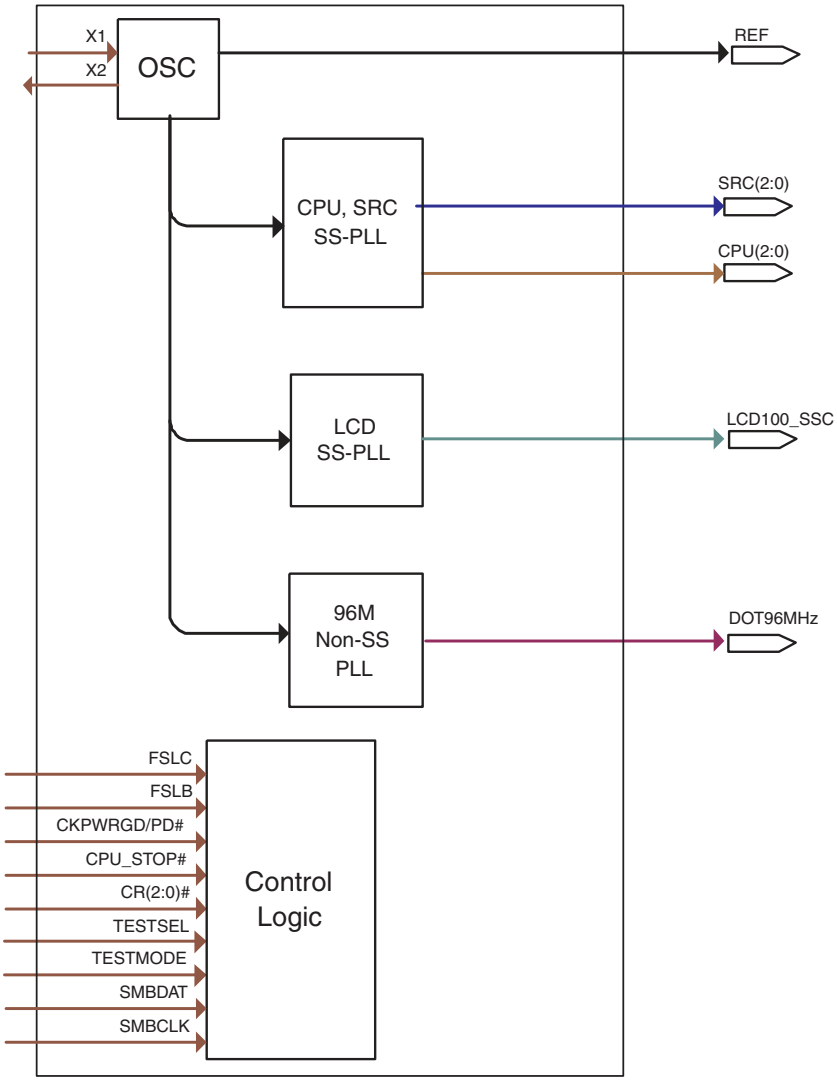
# Pin Description

| PIN # | PIN NAME | TYPE | DESCRIPTION | Logic Level (V) | Input Level Tolerance (V) |
|---|---|---|---|---|---|
| 1 | CPU_STOP#_3.3 | IN | This active-low input stops all CPU clocks that are set to be stoppable. | 3.3 | 3.3 |
| 2 | CLKPWRGD#/PD_3.3 | IN | This level sensitive strobe determines when latch inputs are valid and are ready to be sampled. When high, this asynchronous input places the device into the power down state. | 3.3 | 3.3 |
| 3 | X2 | OUT | Crystal output, Nominally 14.318MHz | N/A | N/A |
| 4 | X1 | IN | Crystal input, Nominally 14.318MHz. | 1.5 | 1.5 |
| 5 | VDDREF_3.3 | PWR | Power pin for the XTAL and REF clocks, nominal 3.3V | 3.3 | 3.3 |
| 6 | REF_3.3_2x | OUT | 3.3V 14.318 MHz reference clock. Default 2 load drive strength | 3.3 | N/A |
| 7 | GNDREF | GND | Ground pin for the REF outputs. | 0 | N/A |
| 8 | VDDCORE_1.5 | PWR | 1.5V power for the PLL core | 1.5 | 1.5 |
| 9 | FSC_L_1.5 | IN | Low threshold input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. 1.5V Max input voltage. | 1.5 | 1.5 |
| 10 | TEST_MODE_1.5 | IN | TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. Max input voltage is 1.5V. | 1.5 | 3.3 |
| 11 | TEST_SEL_1.5 | IN | TEST_SEL: latched input to select TEST MODE. Max input voltage is 1.5V<br>1 = All outputs are tri-stated for test<br>0 = All outputs behave normally. | 1.5 | 3.3 |
| 12 | SCLK_3.3 | IN | Clock pin of SMBus circuitry, 3.3V tolerant. | 3.3 | 3.3 |
| 13 | SDATA_3.3 | I/O | Data pin for SMBus circuitry, 3.3V tolerant. | 3.3 | 3.3 |
| 14 | VDDCORE_1.5 | PWR | 1.5V power for the PLL core | 1.5 | 1.5 |
| 15 | VDDIO_1.5 | PWR | Power supply for low power differential outputs, nominal 1.5V. | 1.5 | 1.5 |
| 16 | DOT96C_LPR | OUT | Complement clock of low power differential pair for 96.00MHz DOT clock. No 50ohm resistor to GND needed. No Rs needed. | 0.8 | N/A |
| 17 | DOT96T_LPR | OUT | True clock of low power differential pair for 96.00MHz DOT clock. No 50ohm resistor to GND needed. No Rs needed. | 0.8 | N/A |
| 18 | GNDDOT | GND | Ground pin for DOT clock output | 0 | N/A |
| 19 | GNDLCD | GND | Ground pin for LCD clock output | 0 | N/A |
| 20 | LCD100C_LPR | OUT | Complement clock of low power differential pair for LCD100 SS clock. No 50ohm resistor to GND needed. No Rs needed. | 0.8 | N/A |
| 21 | LCD100T_LPR | OUT | True clock of low power differential pair for LCD100 SS clock. No 50ohm resistor to GND needed. No Rs needed. | 0.8 | N/A |
| 22 | VDDIO_1.5 | PWR | Power supply for low power differential outputs, nominal 1.5V. | 1.5 | 1.5 |
| 23 | VDDCORE_1.5 | PWR | 1.5V power for the PLL core | 1.5 | 1.5 |
| 24 | *CR#0_1.5 | IN | 1.5V Clock request for SRC0, 0 = enable, 1 = disable | 1.5 | 1.5 |

## Pin Description (continued)

| PIN # | PIN NAME | TYPE | DESCRIPTION | Logic Level (V) | Input Level Tolerance (V) |
|---|---|---|---|---|---|
| 25 | GNDSRC | GND | Ground pin for the SRC outputs | 0 | N/A |
| 26 | SRCC0_LPR | OUT | Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. | 0.8 | N/A |
| 27 | SRCT0_LPR | OUT | True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. | 0.8 | N/A |
| 28 | *CR#1_1.5 | IN | 1.5V Clock request for SRC1, 0 = enable, 1 = disable | 1.5 | 1.5 |
| 29 | VDDCORE_1.5 | PWR | 1.5V power for the PLL core | 1.5 | 1.5 |
| 30 | VDDIO_1.5 | PWR | Power supply for low power differential outputs, nominal 1.5V. | 1.5 | 1.5 |
| 31 | SRCC1_LPR | OUT | Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. | 0.8 | N/A |
| 32 | SRCT1_LPR | OUT | True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. | 0.8 | N/A |
| 33 | GNDSRC | GND | Ground pin for the SRC outputs | 0 | N/A |
| 34 | SRCC2_LPR | OUT | Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. | 0.8 | N/A |
| 35 | SRCT2_LPR | OUT | True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. | 0.8 | N/A |
| 36 | *CR#2_1.5 | IN | 1.5V Clock request for SRC2, 0 = enable, 1 = disable | 1.5 | 1.5 |
| 37 | FSB_L_1.5 | IN | Low threshold input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. 1.5V Max input voltage. | 1.5 | 1.5 |
| 38 | CPUC2_LPR | OUT | Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. | 0.8 | N/A |
| 39 | CPUT2_LPR | OUT | True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. | 0.8 | N/A |
| 40 | GNDCPU | GND | Ground pin for the CPU outputs | 0 | N/A |
| 41 | VDDIO_1.5 | PWR | Power supply for low power differential outputs, nominal 1.5V. | 1.5 | 1.5 |
| 42 | VDDCORE_1.5 | PWR | 1.5V power for the PLL core | 1.5 | 1.5 |
| 43 | CPUC1_LPR | OUT | Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. | 0.8 | N/A |
| 44 | CPUT1_LPR | OUT | True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. | 0.8 | N/A |
| 45 | GNDCPU | GND | Ground pin for the CPU outputs | 0 | N/A |
| 46 | VDDIO_1.5 | PWR | Power supply for low power differential outputs, nominal 1.5V. | 1.5 | 1.5 |
| 47 | CPUC0_LPR | OUT | Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. | 0.8 | N/A |
| 48 | CPUT0_LPR | OUT | True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. | 0.8 | N/A |

## Funtional Block Diagram




## Power Groups

| Pin Number | | Description | |
|---|---|---|---|
| VDD | GND | | |
| 41, 46 | 40, 45 | CPUCLK | Low power outputs |
| 42 | | | VDDCORE_1.5V |
| 30 | 25, 33 | SRCCLK | Low power outputs |
| 29 | | | VDDCORE_1.5V |
| 22 | 19 | LCDCLK | Low power outputs |
| 23 | | | VDDCORE_1.5V |
| 15 | 18 | DOT 96Mhz | Low power outputs |
| 14 | | | VDDCORE_1.5V |
| 5 | 7 | Xtal, REF | |

## Absolute Maximum Ratings

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|
| 3.3V Supply Voltage | VDDxxx_3.3 | Supply Voltage | | 3.9 | V | 1,2 |
| 1.5V Supply Voltage | VDDxxx_1.5 | Supply Voltage | | 2.1 | V | 1,2 |
| 3.3_Input High Voltage | $V_{IH3.3}$ | 3.3V Inputs | | VDD_3.3+ 0.3V | V | 1,2,3 |
| 1.5_Input High Voltage | $V_{IH1.5}$ | 1.5V Inputs | | VDD_1.5+ 0.3V | V | 1,2,3 |
| Minimum Input Voltage | $V_{IL}$ | Any Input | GND - 0.5 | | V | 1 |
| Storage Temperature | Ts | - | -65 | 150 | °C | 1,2 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | V | 1,2 |

**Notes:**

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied, nor guaranteed.

[3] Maximum input voltage is not to exceed maximum VDD

## Electrical Characteristics - Input/Supply/Common Output Parameters

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|
| Ambient Operating Temp | Tambient | No Airflow | 0 | 85 | °C | 1 |
| 3.3V Supply Voltage | VDDxxx_3.3 | 3.3V +/- 5% | 3.135 | 3.465 | V | 1 |
| 1.5V Supply Voltage | VDDxxx_1.5 | 1.5V +/- 5% | 1.425 | 1.575 | V | 1 |
| 3.3V Input High Voltage | $V_{IHSE3.3}$ | Single-ended inputs | 2 | $V_{DDxx\_3.3}$ + 0.3 | V | 1 |
| 3.3V Input Low Voltage | $V_{ILSE3.3}$ | Single-ended inputs | $V_{SS}$ - 0.3 | 0.8 | V | 1 |
| 1.5V Input High Voltage | $V_{IHSE1.5}$ | Single-ended inputs | 1.2 | $V_{DDxxx\_1.5}$ + 0.3 | V | 1 |
| 1.5V Input Low Voltage | $V_{ILSE1.5}$ | Single-ended inputs | $V_{SS}$ - 0.3 | 0.3 | V | 1 |
| Input Leakage Current | $I_{IN}$ | $V_{IN} = V_{DD}$ , $V_{IN}$ = GND | -5 | 5 | uA | 1 |
| Input Leakage Current | $I_{INRES}$ | Inputs with pull or pull down resistors $V_{IN} = V_{DD}$ , $V_{IN}$ = GND | -200 | 200 | uA | 1 |
| Output High Voltage | $V_{OHSE}$ | Single-ended output, $I_{OH}$ = -1mA | 2.4 | | V | 1 |
| Output Low Voltage | $V_{OLSE}$ | Single-ended output, $I_{OL}$ = 1 mA | | 0.4 | V | 1 |
| Low Threshold Input-High Voltage | $V_{IH\_FS}$ | 1.5 V +/-5% | 0.7 | 1.5 | V | 1 |
| Low Threshold Input-Low Voltage | $V_{IL\_FS}$ | 1.5 V +/-5% | $V_{SS}$ - 0.3 | 0.35 | V | 1 |
| Operating Supply Current | $I_{DD\_3.3}$ | 3.3V supply | | 10 | mA | 1 |
| | $I_{DD\_DEFAULT1.5}$ | 1.5V core supply, LCDPLL off | | 45 | mA | 1 |
| | $I_{DD\_LCDEN1.5}$ | 1.5V core supply, LCDPLL enabled | | 55 | mA | 1 |
| | $I_{DD\_IO1.5}$ | 1.5V supply, Differential IO current, all outputs enabled | | 15 | mA | 1 |
| Power Down Current | $I_{DD\_PD3.3}$ | 3.3V supply, Power Down Mode | | 0.5 | mA | 1 |
| | $I_{DD\_PD1.5CORE}$ | 1.5V CORE supply, Power Down Mode | | 0.5 | mA | 1 |
| | $I_{DD\_PD1.5IO}$ | 1.5V IO supply, Power Down Mode | | 0.1 | mA | 1 |
| Input Frequency | $F_i$ | $V_{DD}$ = 3.3 V | | 15 | MHz | 2 |
| Pin Inductance | $L_{pin}$ | | | 7 | nH | 1 |
| Input Capacitance | $C_{IN}$ | Logic Inputs | 1.5 | 5 | pF | 1 |
| | $C_{OUT}$ | Output pin capacitance | | 6 | pF | 1 |
| | $C_{INX}$ | X1 & X2 pins | 3 | 5 | pF | 1 |
| Spread Spectrum Modulation Frequency | $f_{SSMOD}$ | Triangular Modulation | 30 | 33 | kHz | 1 |

## AC Electrical Characteristics - Input/Common Parameters

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|
| Clk Stabilization | $T_{STAB}$ | From VDD Power-Up or de-assertion of PD# to 1st clock | | 1.8 | ms | 1 |
| Tdrive_PD# | $T_{DRPD}$ | Differential output enable after PD# de-assertion | | 300 | us | 1 |
| Tdrive_CPU | $T_{DRSRC}$ | CPU output enable after CPU_STOP# de-assertion | 2 | 6 | Cycles | 1 |
| Tfall_PD# | $T_{FALL}$ | Fall/rise time of PD# and CPU_STOP# inputs | | 5 | ns | 1 |
| Trise_PD# | $T_{RISE}$ | | | 5 | ns | 1 |

## AC Electrical Characteristics - Low Power Differential Outputs

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Rising Edge Slew Rate | $t_{SLR}$ | Differential Measurement | 0.6 | 4 | V/ns | 1,2 |
| Falling Edge Slew Rate | $t_{FLR}$ | Differential Measurement | 0.6 | 4 | V/ns | 1,2 |
| Rise/Fall Time Variation | $t_{SLVAR}$ | Single-ended Measurement | | 125 | ps | 1 |
| Maximum Output Voltage | $V_{HIGH}$ | Includes overshoot | | 1150 | mV | 1 |
| Minimum Output Voltage | $V_{LOW}$ | Includes undershoot | -300 | | mV | 1 |
| Differential Voltage Swing | $V_{SWING}$ | Differential Measurement | 300 | | mV | 1 |
| Crossing Point Voltage | $V_{XABS}$ | Single-ended Measurement | 300 | 550 | mV | 1,3,4 |
| Crossing Point Variation | $V_{XABSVAR}$ | Single-ended Measurement | | 140 | mV | 1,3,5 |
| Duty Cycle | $D_{CYC}$ | Differential Measurement | 45 | 55 | % | 1 |
| CPU Jitter - Cycle to Cycle | $CPUJ_{C2C}$ | Differential Measurement | | 85 | ps | 1 |
| SRC Jitter - Cycle to Cycle | $SRCJ_{C2C}$ | Differential Measurement | | 125 | ps | 1 |
| DOT Jitter - Cycle to Cycle | $DOTJ_{C2C}$ | Differential Measurement | | 250 | ps | 1 |
| LCD Jitter - Cycle to Cycle | $LCDJ_{C2C}$ | Differential Measurement | | 85 | ps | 1 |
| CPU[2:0] Skew | $CPU_{SKEW10}$ | Differential Measurement | | 100 | ps | 1 |
| SRC[2:0] Skew | $SRC_{SKEW}$ | Differential Measurement | | 250 | ps | 1 |

## Electrical Characteristics - REF-14.318MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|
| Long Accuracy | ppm | see Tperiod min-max values | -300 | 300 | ppm | 1,2 |
| Clock period | $T_{period}$ | 14.318MHz output nominal | 69.8203 | 69.8622 | ns | 2 |
| Absolute min/max period | $T_{abs}$ | 14.318MHz output nominal | 69.8203 | 70.86224 | ns | 2 |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | V | 1 |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | 0.4 | V | 1 |
| Output High Current | $I_{OH}$ | $V_{OH}$@MIN = 1.0 V, $V_{OH}$@MAX = 3.135 V | -33 | -33 | mA | 1 |
| Output Low Current | $I_{OL}$ | $V_{OL}$@MIN = 1.95 V, $V_{OL}$@MAX = 0.4 V | 30 | 38 | mA | 1 |
| Rising Edge Slew Rate | $t_{SLR}$ | Measured from 0.8 to 2.0 V | 1 | 4 | V/ns | 1 |
| Falling Edge Slew Rate | $t_{FLR}$ | Measured from 2.0 to 0.8 V | 1 | 4 | V/ns | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 1.5 V | 45 | 55 | % | 1 |
| Jitter | $t_{jcyc-cyc}$ | $V_T$ = 1.5 V | | 1000 | ps | 1 |

## Electrical Characteristics - SMBus Interface

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|
| SMBus Voltage | $V_{DD}$ | | 2.7 | 3.6 | V | 1 |
| Low-level Output Voltage | $V_{OLSMB}$ | @ $I_{PULLUP}$ | | 0.4 | V | 1 |
| Current sinking at $V_{OLSMB}$ = 0.4 V | $I_{PULLUP}$ | SMB Data Pin | 4 | | mA | 1 |
| SCLK/SDATA Clock/Data Rise Time | $T_{RI2C}$ | (Max VIL - 0.15) to (Min VIH + 0.15) | | 1000 | ns | 1 |
| SCLK/SDATA Clock/Data Fall Time | $T_{FI2C}$ | (Min VIH + 0.15) to (Max VIL - 0.15) | | 300 | ns | 1 |
| Maximum SMBus Operating Frequency | $F_{SMBUS}$ | Block Mode | | 100 | kHz | 1 |

### Notes on Electrical Characteristics:

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through Vswing centered around differential zero

[3] Vxabs is defined as the voltage where CLK = CLK#

[4] Only applies to the differential rising edge (CLK rising and CLK# falling)

[5] Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#. The average cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[6] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is at 14.31818MHz

[7] Operation under these conditions is neither implied, nor guaranteed.

[8] Maximum input voltage is not to exceed maximum VDD

[9] See PCI Clock-to-Clock Delay Figure

## Clock Periods Differential Outputs with Spread Spectrum Enabled

| Measurement Window | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | | Lg- | -SSC | -ppm error | 0ppm | + ppm error | +SSC | Lg+ | | |
| Definition | | Absolute Period | Short-term Average | Long-Term Average | Period | Long-Term Average | Short-term Average | Period | | |
| | | Minimum Absolute Period | Minimum Absolute Period | Minimum Absolute Period | Nominal | Maximum | Maximum | Maximum | Units | Notes |
| Signal Name | SRC 100 | 9.87400 | 9.99900 | 9.99900 | 10.00000 | 10.00100 | 10.05130 | 10.17630 | ns | 1,2 |
| | CPU 100 | 9.91400 | 9.99900 | 9.99900 | 10.00000 | 10.00100 | 10.05130 | 10.13630 | ns | 1,2 |
| | CPU 133 | 7.41425 | 7.49925 | 7.49925 | 7.50000 | 7.50075 | 7.53845 | 7.62345 | ns | 1,2 |

## Clock Periods Differential Outputs with Spread Spectrum Disabled

| Measurement Window | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | | Lg- | -SSC | -ppm error | 0ppm | + ppm error | +SSC | Lg+ | | |
| Definition | | Absolute Period | Short-term Average | Long-Term Average | Period | Long-Term Average | Short-term Average | Period | | |
| | | Minimum Absolute Period | Minimum Absolute Period | Minimum Absolute Period | Nominal | Maximum | Maximum | Maximum | Units | Notes |
| Signal Name | SRC 100 | 9.87400 | | 9.99900 | 10.00000 | 10.00100 | | 10.17630 | ns | 1,2 |
| | CPU 100 | 9.91400 | | 9.99900 | 10.00000 | 10.00100 | | 10.13630 | ns | 1,2 |
| | CPU 133 | 7.41425 | | 7.49925 | 7.50000 | 7.50075 | | 7.62345 | ns | 1,2 |
| | DOT 96 | 10.16560 | | 10.41560 | 10.41670 | 10.41770 | | 10.66770 | ns | 1,2 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

**Table 1: CPU Frequency Select Table**

| $FS_LC$[1] | $FS_LB$[1] | CPU MHz | SRC MHz | DOT MHz | LCD100 MHz | REF MHz |
|---|---|---|---|---|---|---|
| 0 | 0 | 133.33 | 100.00 | 96.00 | 100.00 | 14.318 |
| 0 | 1 | 166.67 | | | | |
| 1 | 0 | 100.00 | | | | |
| 1 | 1 | 200.00 | | | | |

1. $FS_LC$ is a low-threshold input.Please see $V_{IL\_FS}$ and $V_{IH\_FS}$ specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification Table.

**Table 2: LCD Spread Select Table (Pin 20/21)**

| B1b5 | B1b4 | B1b3 | Spread % | Comment |
|---|---|---|---|---|
| 0 | 0 | 0 | -0.5% | LCD100 |
| 0 | 0 | 1 | -1% | LCD100 |
| 0 | 1 | 0 | -2% | LCD100 |
| 0 | 1 | 1 | -2.5% | LCD100 |
| 1 | 0 | 0 | +/- 0.25% | LCD100 |
| 1 | 0 | 1 | +/-0.5% | LCD100 |
| 1 | 1 | 0 | +/-1% | LCD100 |
| 1 | 1 | 1 | +/-1.25% | LCD100 |

# General I²C serial interface information for the ICS9UMS9610

## How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

## How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

**Index Block Write Operation**

| Controller (Host) | | ICS (Slave/Receiver) |
|---|---|---|
| T | starT bit | |
| Slave Address D2(H) | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| Data Byte Count = X | | |
| | | ACK |
| Beginning Byte N | X Byte | |
| | | ACK |
| O | | |
| O | | O |
| O | | O |
| | | O |
| Byte N + X - 1 | | |
| | | ACK |
| P | stoP bit | |

**Index Block Read Operation**

| Controller (Host) | | ICS (Slave/Receiver) | |
|---|---|---|---|
| T | starT bit | | |
| Slave Address D2(H) | | | |
| WR | WRite | | |
| | | ACK | |
| Beginning Byte = N | | | |
| | | ACK | |
| RT | Repeat starT | | |
| Slave Address D3(H) | | | |
| RD | ReaD | | |
| | | ACK | |
| | | | |
| | | Data Byte Count = X | |
| ACK | | | |
| | X Byte | | Beginning Byte N |
| ACK | | | |
| | | | O |
| O | | | O |
| O | | | O |
| O | | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

**Byte 0 PLL & Divider Enable Register**

| Bit(s) | Pin # | Name | Description | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| 7 | - | PLL1 Enable | This bit controls whether the PLL driving the CPU and SRC clocks is enabled or not. | RW | 0 = Disabled | 1 = Enabled | 1 |
| 6 | - | PLL2 Enable | This bit controls whether the PLL driving the DOT and clock is enabled or not. | RW | 0 = Disabled | 1 = Enabled | 1 |
| 5 | - | PLL3 Enable | This bit controls whether the PLL driving the LCD clock is enabled or not. | RW | 0 = Disabled | 1 = Enabled | 1 |
| 4 | - | Reserved | | | | | 0 |
| 3 | - | CPU Divider Enable | This bit controls whether the CPU output divider is enabled or not. **NOTE:** This bit should be automatically set to '0' if bit 7 is set to '0'. | RW | 0 = Disabled | 1 = Enabled | 1 |
| 2 | - | SRC Output Divider Enable | This bit controls whether the SRC output divider is enabled or not. NOTE: This bit should be automatically set to '0' if bit 7 is set to '0'. | RW | 0 = Disabled | 1 = Enabled | 1 |
| 1 | - | LCD Output Divider Enable | This bit controls whether the LCD output divider is enabled or not. **NOTE:** This bit should be automatically set to '0' if bit 5 is set to '0'. | RW | 0 = Disabled | 1 = Enabled | 1 |
| 0 | - | DOT Output Divider Enable | This bit controls whether the DOT output divider is enabled or not. **NOTE:** This bit should be automatically set to '0' if bit 6 is set to '0'. | RW | 0 = Disabled | 1 = Enabled | 1 |

**Byte 1 PLL SS Enable/Control Register**

| Bit(s) | Pin # | Name | Description | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| 7 | | PLL1 SS Enable | This bit controls whether PLL1 has spread enabled or not. Spread spectrum for PLL1 is set at -0.5% down-spread. Note that PLL1 drives the CPU and SRC clocks. | RW | 0 = Disabled | 1 = Enabled | 1 |
| 6 | | PLL3 SS Enable | This bit controls whether PLL3 has spread enabled or not. Note that PLL3 drives the SSC clock, and that the spread spectrum amount is set in bits 3-5. | RW | 0 = Disabled | 1 = Enabled | 1 |
| 5 | | PLL3 FS Select | These 3 bits select the frequency of PLL3 and the SSC clock when Byte 1 Bit 6 (PLL3 Spread Spectrum Enable) is set. | RW | See Table 2: LCD Spread Select Table | | 0 |
| 4 | | | | | | | 0 |
| 3 | | | | | | | 0 |
| 2 | | Reserved | | | | | 0 |
| 1 | | Reserved | | | | | 0 |
| 0 | | Reserved | | | | | 0 |

**Byte 2 Output Enable Register**

| Bit(s) | Pin # | Name | Description | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| 7 | | CPU0 Enable | This bit controls whether the CPU[0] output buffer is enabled or not. | RW | 0 = Disabled | 1 = Enabled | 1 |
| 6 | | CPU1 Enable | This bit controls whether the CPU[1] output buffer is enabled or not. | RW | 0 = Disabled | 1 = Enabled | 1 |
| 5 | | CPU2 Enable | This bit controls whether the CPU[2] output buffer is enabled or not. | RW | 0 = Disabled | 1 = Enabled | 1 |
| 4 | | SRC0 Enable | This bit controls whether the SRC[0] output buffer is enabled or not. | RW | 0 = Disabled | 1 = Enabled | 1 |
| 3 | | SRC1 Enable | This bit controls whether the SRC[1] output buffer is enabled or not. | RW | 0 = Disabled | 1 = Enabled | 1 |
| 2 | | SRC2 Enable | This bit controls whether the SRC[2] output buffer is enabled or not. | RW | 0 = Disabled | 1 = Enabled | 1 |
| 1 | | DOT Enable | This bit controls whether the DOT output buffer is enabled or not. | RW | 0 = Disabled | 1 = Enabled | 1 |
| 0 | | LCD100 Enable | This bit controls whether the LCD output buffer is enabled or not. | RW | 0 = Disabled | 1 = Enabled | 1 |

**Byte 3 Output Control Register**

| Bit(s) | Pin # | Name | Description | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| 7 | | Reserved | | | | | 0 |
| 6 | | Reserved | | | | | 0 |
| 5 | | REF Enable | This bit controls whether the REF output buffer is enabled or not. | RW | 0 = Disabled | 1 = Enabled | 1 |
| 4 | | REF Slew | These bits control the edge rate of the REF clock. | RW | 00 = Slow Edge Rate<br>01 = Medium Edge Rate<br>10 = Fast Edge Rate<br>11 = Reserved | | 10 |
| 3 | | | | | | | |
| 2 | | CPU0 Stop Enable | This bit controls whether the CPU[0] output buffer is free-running or stoppable. If it is set to stoppable the CPU[0] output buffer will be disabled with the assertion of CPU_STP#. | RW | Free Running | Stoppable | 0 |
| 1 | | CPU1 Stop Enable | This bit controls whether the CPU[1] output buffer is free-running or stoppable. If it is set to stoppable the CPU[1] output buffer will be disabled with the assertion of CPU_STP#. | RW | Free Running | Stoppable | 0 |
| 0 | | CPU2 Stop Enable | This bit controls whether the CPU[2] output buffer is free-running or stoppable. If it is set to stoppable the CPU[2] output buffer will be disabled with the assertion of CPU_STP#. | RW | Free Running | Stoppable | 0 |

**Byte 4 CPU PLL M/N Register**

| Bit(s) | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | | CPU N Div8 | N Divider Prog bit 8 | RW | The decimal representation of M and N Divider in Byte 4 and 5 will configure the CPU VCO frequency. Default at power up = latch-in. VCO Frequency = 14.318 x [NDiv(11:0)] / [MDiv(5:0)] | | X |
| Bit 6 | | CPU N Div9 | N Divider Prog bit 9 | RW | | | X |
| Bit 5 | | CPU M Div5 | M Divider Programming bit (5:0) | RW | | | X |
| Bit 4 | | CPU M Div4 | | RW | | | X |
| Bit 3 | | CPU M Div3 | | RW | | | X |
| Bit 2 | | CPU M Div2 | | RW | | | X |
| Bit 1 | | CPU M Div1 | | RW | | | X |
| Bit 0 | | CPU M Div0 | | RW | | | X |

**Byte 5 CPU PLL M/N Register**

| Bit(s) | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | | CPU N Div7 | N Divider Programming Byte5 bit(7:0) and Byte5 bit(7:6) | RW | The decimal representation of M and N Divider in Byte 4 and 5 will configure the CPU VCO frequency. Default at power up = latch-in. VCO Frequency = 14.318 x [NDiv(11:0)] / [MDiv(5:0)] | | X |
| Bit 6 | | CPU N Div6 | | RW | | | X |
| Bit 5 | | CPU N Div5 | | RW | | | X |
| Bit 4 | | CPU N Div4 | | RW | | | X |
| Bit 3 | | CPU N Div3 | | RW | | | X |
| Bit 2 | | CPU N Div2 | | RW | | | X |
| Bit 1 | | CPU N Div1 | | RW | | | X |
| Bit 0 | | CPU N Div0 | | RW | | | X |

**Byte 6 DOT96 PLL M/N Register**

| Bit(s) | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | | DOT N Div8 | N Divider Prog bit 8 | RW | The decimal representation of M and N Divider in Byte 6 and 7 will configure the DOT VCO frequency. VCO Frequency = 14.318 x [NDiv(11:0)] / [MDiv(5:0)] | | X |
| Bit 6 | | DOT N Div9 | N Divider Prog bit 9 | RW | | | X |
| Bit 5 | | DOT M Div5 | M Divider Programming bit (5:0) | RW | | | X |
| Bit 4 | | DOT M Div4 | | RW | | | X |
| Bit 3 | | DOT M Div3 | | RW | | | X |
| Bit 2 | | DOT M Div2 | | RW | | | X |
| Bit 1 | | DOT M Div1 | | RW | | | X |
| Bit 0 | | DOT M Div0 | | RW | | | X |

**Byte 7 DOT96 PLL M/N Register**

| Bit(s) | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | | DOT N Div7 | N Divider Programming Byte7 bit(7:0) and Byte6 bit(7:6) | RW | The decimal representation of M and N Divider in Byte 6 and 7 will configure the DOT VCO frequency. VCO Frequency = 14.318 x [NDiv(11:0)] / [MDiv(5:0)] | | X |
| Bit 6 | | DOT N Div6 | | RW | | | X |
| Bit 5 | | DOT N Div5 | | RW | | | X |
| Bit 4 | | DOT N Div4 | | RW | | | X |
| Bit 3 | | DOT N Div3 | | RW | | | X |
| Bit 2 | | DOT N Div2 | | RW | | | X |
| Bit 1 | | DOT N Div1 | | RW | | | X |
| Bit 0 | | DOT N Div0 | | RW | | | X |

**Byte 8 LCD100 PLL M/N Register**

| Bit(s) | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | | LCD100 N Div8 | N Divider Prog bit 8 | RW | The decimal representation of M and N Divider in Byte 8 and 9 will configure the DOT VCO frequency. VCO Frequency = 14.318 x [NDiv(11:0)] / [MDiv(5:0)] | | X |
| Bit 6 | | LCD100 N Div9 | N Divider Prog bit 9 | RW | | | X |
| Bit 5 | | LCD100 M Div5 | M Divider Programming bit (5:0) | RW | | | X |
| Bit 4 | | LCD100 M Div4 | | RW | | | X |
| Bit 3 | | LCD100 M Div3 | | RW | | | X |
| Bit 2 | | LCD100 M Div2 | | RW | | | X |
| Bit 1 | | LCD100 M Div1 | | RW | | | X |
| Bit 0 | | LCD100 M Div0 | | RW | | | X |

**Byte 9 LCD100 PLL M/N Register**

| Bit(s) | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | | LCD100 N Div7 | N Divider Programming Byte9 bit(7:0) and Byte8 bit(7:6) | RW | The decimal representation of M and N Divider in Byte 8 and 9 will configure the DOT VCO frequency. VCO Frequency = 14.318 x [NDiv(11:0)] / [MDiv(5:0)] | | X |
| Bit 6 | | LCD100 N Div6 | | RW | | | X |
| Bit 5 | | LCD100 N Div5 | | RW | | | X |
| Bit 4 | | LCD100 N Div4 | | RW | | | X |
| Bit 3 | | LCD100 N Div3 | | RW | | | X |
| Bit 2 | | LCD100 N Div2 | | RW | | | X |
| Bit 1 | | LCD100 N Div1 | | RW | | | X |
| Bit 0 | | LCD100 N Div0 | | RW | | | X |

**Byte 10 Status Readback Register**

| Bit(s) | Pin # | Name | Description | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| 7 | 37 | FSB | Frequency Select B | R | See Table 1: CPU Frequency Select Table | | Latch |
| 6 | 9 | FSC | Frequency Select C | R | | | Latch |
| 5 | 24 | CR0# Readbk | Real time CR0# State Indicator | R | CR0# is Low | CR0# is High | X |
| 4 | 28 | CR1# Readbk | Real time CR1# State Indicator | R | CR1# is Low | CR1# is High | X |
| 3 | 36 | CR2# Readbk | Real time CR2# State Indicator | R | CR2# is Low | CR2# is High | X |
| 2 | | Reserved | | | | | 0 |
| 1 | | Reserved | | | | | 0 |
| 0 | | Reserved | | | | | 0 |

**Byte 11 Revision ID/Vendor ID Register**

| Bit(s) | Pin # | Name | Description | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| 7 | | Rev Code Bit 3 | Revision ID | R | Vendor specific | | X |
| 6 | | Rev Code Bit 2 | | R | | | X |
| 5 | | Rev Code Bit 1 | | R | | | X |
| 4 | | Rev Code Bit 0 | | R | | | X |
| 3 | | Vendor ID bit 3 | Vendor ID | R | | | 0 |
| 2 | | Vendor ID bit 2 | | R | | | 0 |
| 1 | | Vendor ID bit 1 | | R | | | 0 |
| 0 | | Vendor ID bit 0 | | R | | | 1 |

**Byte 12 Device ID Register**

| Bit(s) | Pin # | Name | Description | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| 7 | | DEV_ID3 | Device ID MSB | R | | | 1 |
| 6 | | DEV_ID2 | Device ID 2 | R | | | 0 |
| 5 | | DEV_ID1 | Device ID 1 | R | | | 1 |
| 4 | | DEV_ID0 | Device ID LSB | R | | | 0 |
| 3 | | Reserved | | | | | 0 |
| 2 | | Reserved | | | | | 0 |
| 1 | | Reserved | | | | | 0 |
| 0 | | Reserved | | | | | 0 |

**Byte 13 Reserved Register**

| Bit(s) | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| **Bit 7** | | Reserved | | | | | 0 |
| **Bit 6** | | Reserved | | | | | 0 |
| **Bit 5** | | Reserved | | | | | 0 |
| **Bit 4** | | Reserved | | | | | 0 |
| **Bit 3** | | Reserved | | | | | 0 |
| **Bit 2** | | Reserved | | | | | 0 |
| **Bit 1** | | Reserved | | | | | 0 |
| **Bit 0** | | Reserved | | | | | 0 |

**Byte 14 Reserved Register**

| Bit(s) | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| **Bit 7** | | Reserved | | | | | 0 |
| **Bit 6** | | Reserved | | | | | 0 |
| **Bit 5** | | Reserved | | | | | 0 |
| **Bit 4** | | Reserved | | | | | 0 |
| **Bit 3** | | Reserved | | | | | 0 |
| **Bit 2** | | Reserved | | | | | 0 |
| **Bit 1** | | Reserved | | | | | 0 |
| **Bit 0** | | Reserved | | | | | 0 |

**Byte 15 Byte Count Register**

| Bit(s) | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| **Bit 7** | | Reserved | | | | | 0 |
| **Bit 6** | | BC6 | Byte Count 6 (MSB) | RW | Specifies Number of bytes to be read back during an SMBus read. Default is 0xF. | | 0 |
| **Bit 5** | | BC5 | Byte Count 5 | RW | | | 0 |
| **Bit 4** | | BC4 | Byte Count 4 | RW | | | 0 |
| **Bit 3** | | BC3 | Byte Count 3 | RW | | | 1 |
| **Bit 2** | | BC2 | Byte Count 2 | RW | | | 1 |
| **Bit 1** | | BC1 | Byte Count 1 | RW | | | 1 |
| **Bit 0** | | BC0 | Byte Count LSB | RW | | | 1 |

**Byte 16 M/N Enable Register**

| Bit(s) | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | | MN Enable | Enables PLL MN programming | RW | MN Disabled | MN Enabled | 0 |
| Bit 6 | | Reserved | | | | | 0 |
| Bit 5 | | Reserved | | | | | 0 |
| Bit 4 | | Reserved | | | | | 0 |
| Bit 3 | | Reserved | | | | | 0 |
| Bit 2 | | Reserved | | | | | 0 |
| Bit 1 | | Reserved | | | | | 0 |
| Bit 0 | | Reserved | | | | | 0 |

**Byte 17 CPU PLL Spread Spectrum Index Register**

| Bit(s) | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | | CPUSSP7 | Spread Spectrum Programming bit(7:0) Contact IDT before editing these values. | RW | These Spread Spectrum bits in Byte 17 and 18 will program the spread percentage of the CPU and SRC outputs | | X |
| Bit 6 | | CPUSSP6 | | RW | | | X |
| Bit 5 | | CPUSSP5 | | RW | | | X |
| Bit 4 | | CPUSSP4 | | RW | | | X |
| Bit 3 | | CPUSSP3 | | RW | | | X |
| Bit 2 | | CPUSSP2 | | RW | | | X |
| Bit 1 | | CPUSSP1 | | RW | | | X |
| Bit 0 | | CPUSSP0 | | RW | | | X |

**Byte 18 CPU PLL Spread Spectrum Index Register**

| Bit(s) | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | | CPUSSP15 | Spread Spectrum Programming bit(15:8) Contact IDT before editing these values. | RW | These Spread Spectrum bits in Byte 17 and 18 will program the spread percentage of the CPU and SRC outputs | | X |
| Bit 6 | | CPUSSP14 | | RW | | | X |
| Bit 5 | | CPUSSP13 | | RW | | | X |
| Bit 4 | | CPUSSP12 | | RW | | | X |
| Bit 3 | | CPUSSP11 | | RW | | | X |
| Bit 2 | | CPUSSP10 | | RW | | | X |
| Bit 1 | | CPUSSP9 | | RW | | | X |
| Bit 0 | | CPUSSP8 | | RW | | | X |

**Byte 19 LCD100 PLL Spread Spectrum Index Register**

| Bit(s) | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | | LCDSSP7 | Spread Spectrum Programming bit(7:0) Contact IDT before editing these values. | RW | These Spread Spectrum bits in Byte 19 and 20 will program the spread percentage of the CPU and SRC outputs | | X |
| Bit 6 | | LCDSSP6 | | RW | | | X |
| Bit 5 | | LCDSSP5 | | RW | | | X |
| Bit 4 | | LCDSSP4 | | RW | | | X |
| Bit 3 | | LCDSSP3 | | RW | | | X |
| Bit 2 | | LCDSSP2 | | RW | | | X |
| Bit 1 | | LCDSSP1 | | RW | | | X |
| Bit 0 | | LCDSSP0 | | RW | | | X |

**Byte 20 LCD100 PLL Spread Spectrum Index Register**

| Bit(s) | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | | LCDSSP15 | Spread Spectrum Programming bit(15:8) Contact IDT before editing these values. | RW | These Spread Spectrum bits in Byte 19 and 20 will program the spread percentage of the CPU and SRC outputs | | X |
| Bit 6 | | LCDSSP14 | | RW | | | X |
| Bit 5 | | LCDSSP13 | | RW | | | X |
| Bit 4 | | LCDSSP12 | | RW | | | X |
| Bit 3 | | LCDSSP11 | | RW | | | X |
| Bit 2 | | LCDSSP10 | | RW | | | X |
| Bit 1 | | LCDSSP9 | | RW | | | X |
| Bit 0 | | LCDSSP8 | | RW | | | X |

**Byte 21 CPU PLL M/N Register**

| Bit(s) | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | | CPU NDIV 10 | N Divider Prog bit 10 | RW | See Byte 4/5 Description | | X |
| Bit 6 | | CPU NDIV 11 | N Divider Prog bit 11 | RW | | | X |
| Bit 5 | | Reserved | | | | | 0 |
| Bit 4 | | Reserved | | | | | 0 |
| Bit 3 | | Reserved | | | | | 0 |
| Bit 2 | | Reserved | | | | | 0 |
| Bit 1 | | Reserved | | | | | 0 |
| Bit 0 | | Reserved | | | | | 0 |

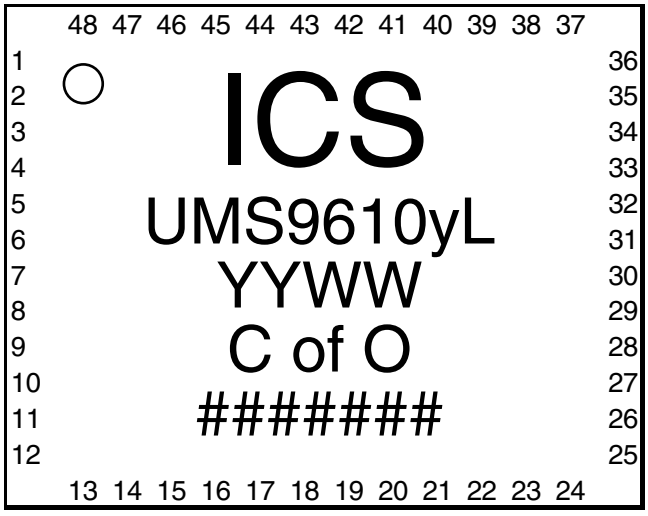
**Byte 22 LCD100 PLL M/N Register**

| Bit(s) | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | | LCD NDIV 10 | N Divider Prog bit 10 | RW | See Byte 8/9 Description | | X |
| Bit 6 | | LCD NDIV 11 | N Divider Prog bit 11 | RW | | | X |
| Bit 5 | | Reserved | | | | | 0 |
| Bit 4 | | Reserved | | | | | 0 |
| Bit 3 | | Reserved | | | | | 0 |
| Bit 2 | | Reserved | | | | | 0 |
| Bit 1 | | Reserved | | | | | 0 |
| Bit 0 | | Reserved | | | | | 0 |

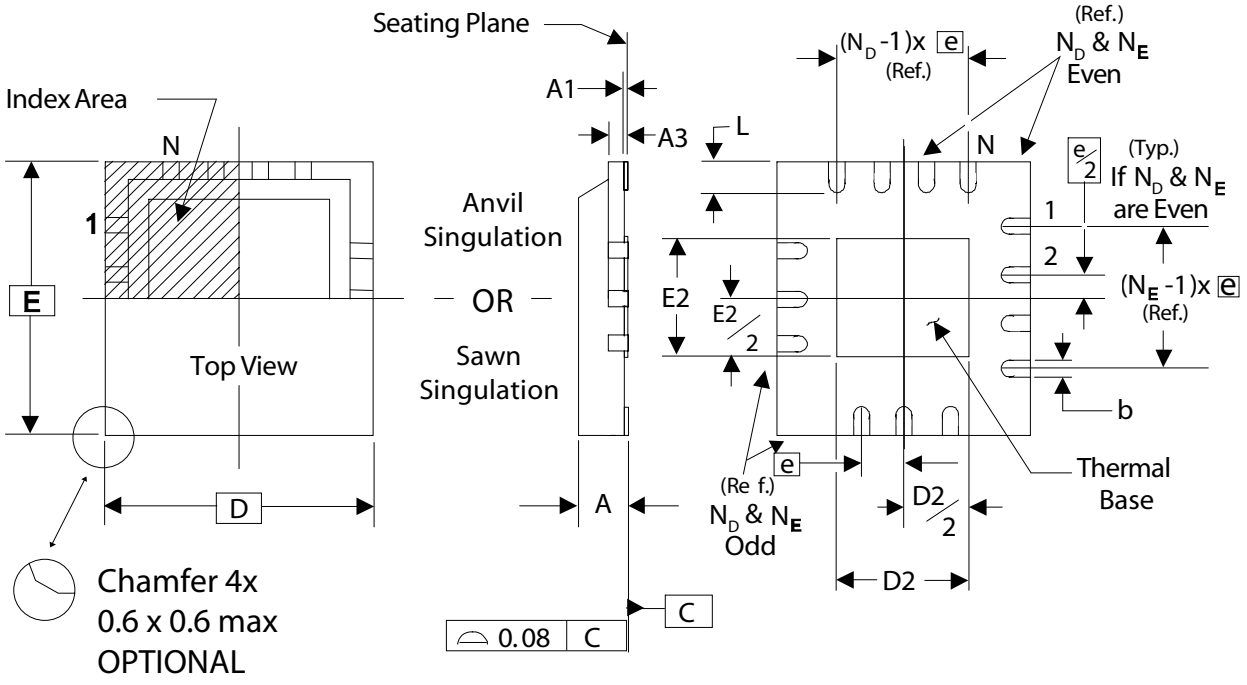
## Test Clarification Table

| Comments | HW | | |
|---|---|---|---|
| | TEST_SEL HW PIN | TEST_MODE HW PIN | OUTPUT |
| | <0.35V | X | NORMAL |
| Power-up w/ TEST_SEL = 1 to enter test mode<br>Cycle power to disable test mode<br>TEST_MODE -->low Vth input<br>TEST_MODE is a real time input | >0.7V | <0.35V | HI-Z |
| | >0.7V | >0.7V | REF/N |

## MLF Top Mark Information (9UMS9610)




Line 1. Company name
Line 2. Part Number
Line 3. YYWW = Date Code
Line 3. Country of Origin
Line 4. ####### = Lot Number




**THERMALLY ENHANCED, VERY THIN, FINE PITCH**
**QUAD FLAT / NO LEAD PLASTIC PACKAGE**

DIMENSIONS

| SYMBOL | MIN. | MAX. |
|---|---|---|
| A | 0.8 | 1.0 |
| A1 | 0 | 0.05 |
| A3 | 0.20 Reference | |
| b | 0.18 | 0.3 |
| e | 0.40 BASIC | |

DIMENSIONS

| SYMBOL | 48L TOLERANCE |
|---|---|
| N | 48 |
| $N_D$ | 12 |
| $N_E$ | 12 |
| D x E BASIC | 6.00 x 6.00 |
| D2 MIN. / MAX. | 3.95 / 4.25 |
| E2 MIN. / MAX. | 3.95 / 4.25 |
| L MIN. / MAX. | 0.30 / 0.50 |

## Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---|---|---|---|---|
| 9UMS9610CKLF | see page 18 | Tubes | 48-pin MLF | 0 to +85° C |
| 9UMS9610CKLFT | | Tape and Reel | 48-pin MLF | 0 to +85° C |

**Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.**

## Revision History

| Rev. | Issue Date | Description | Page # |
|---|---|---|---|
| 0.1 | 04/25/07 | Initial Release | - |
| 0.15 | 05/03/07 | Corrected CLKPWRGD#/PD polarity | 1 |
| 0.2 | 5/18/2007 | Updated Test Clarification Table with the correct voltage levels. | - |
| 0.3 | 8/31/2007 | Updated Input Pin names to indicate maximum Input voltage level | - |
| 0.4 | 9/11/2007 | Added Logic Level and Input Level Tolerance Columns to Pin Descriptions. | 2, 3 |
| 0.5 | 9/13/2007 | Clarified that X1 is 1.5V only input | 2 |
| 0.6 | 10/23/007 | 1. Byte Count in Byte 15 is 7 bits, not 8 bits. B15b7 is now reserved.<br>2. Modified PLL programming formulas in Bytes(4:9). N is 12 bits instead of 10 bits.<br>3. Changed REF_3.3 output name to reflect default drive strength (new name is REF_3.3_2x). | Various |
| 0.7 | 11/6/2007 | Updated Bytes [9:4]. | 12-13 |
| 0.8 | 11/29/2007 | Added Bytes 16-22 to the SMBUS. | 15-16 |
| 0.9 | 2/26/2008 | Added MLF Top Mark Information. | 18 |
| 0.91 | 7/8/2008 | Updated Electrical Specifications | 5-7 |
| 0.92 | 7/21/2008 | Updated Electrical Specifications | 5-7 |
| A | 5/21/2009 | Moved to final. | - |
| B | 6/1/2009 | Updated electrical specs; TA spec in ordering information. | Various |

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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

### Contact Information

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