

December 1996

Fast CMOS 3.3V 16-Bit Registered Transceiver

Features

- Compatible with LCX™ Families of Products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input Can Be 3V or 5V
- Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability:
 - Balanced Drives (24mA Sink and Source)
- Pin Compatible with Industry Standard Double-Density Pinouts
- Low Ground Bounce Outputs
- Hysteresis on All Inputs
- Multiple Center Pin and Distributed V_{CC}/GND Pins Minimizing Switching Noise

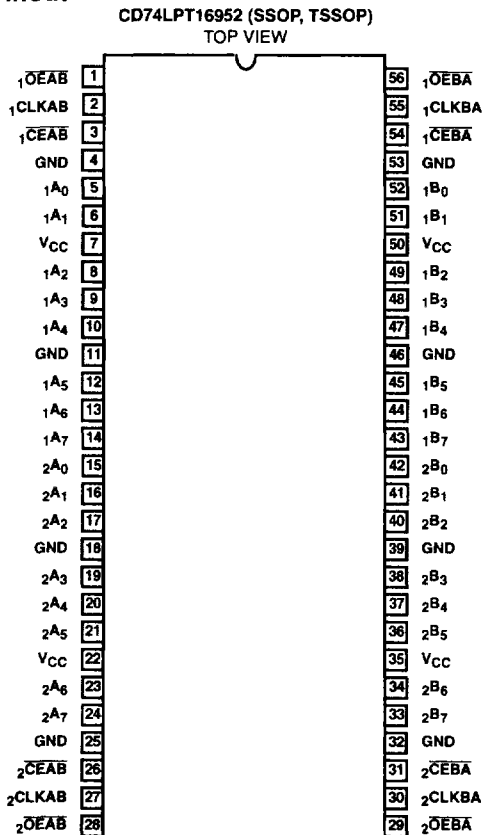
Description

Harris' CD74LPT16952 is produced in an advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The CD74LPT16952 is a 16-bit registered transceiver organized with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{\chi_{CEAB}}$) input must be LOW in order to enter data from χ_{Ax} . The data present on the A port will be clocked on the B register when χ_{CLKAB} toggles from LOW-to-HIGH. The χ_{OEAB} control performs the output enable function on the B port. Control of data from B to A is similar, but uses the χ_{CEAB} , χ_{CLKAB} , and χ_{OEAB} inputs. By connecting the control pins of the two independent transceivers together, a full 16-bit operation can be achieved. The output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74LPT16952 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Pinout



Ordering Information

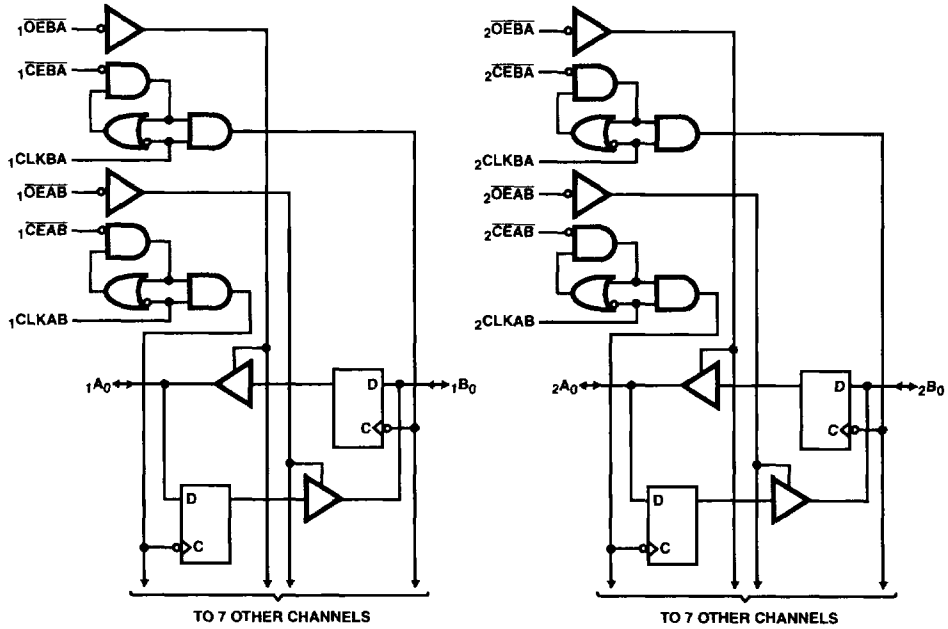
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT16952AMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16952ASM	-40 to 85	56 Ld SSOP	M56.300-P
CD74LPT16952BMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16952BSM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

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Functional Block Diagram



TRUTH TABLE (NOTES 1, 2)

INPUTS			OUTPUTS	
$\chi\overline{CEAB}$	$\chi\overline{CLKAB}$	$\chi\overline{OEAB}$	$\chi A\chi$	$\chi B\chi$
H	X	L	X	B (Note 3)
X	L	L	X	B (Note 3)
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	High Z

NOTES:

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care or Irrelevant
↑ = LOW-to-HIGH Transition
Z = High Impedance
2. A-to-B data flow shown. B-to-A flow control is the same, except using $\chi\overline{CEBA}$, $\chi\overline{CLKBA}$, and $\chi\overline{OEBA}$.
3. Level of B before the indicated steady-state input conditions were established.

Pin Description

PIN NAME	DESCRIPTION
$\chi\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\chi\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\chi\overline{CEAB}$	A-to-B Clock Enable Input (Active LOW)
$\chi\overline{CEBA}$	B-to-A Clock Enable Input (Active LOW)
$\chi\overline{CLKAB}$	A-to-B Clock Input
$\chi\overline{CLKBA}$	B-to-A Clock Input
$\chi A\chi$	A-to-B Data Inputs or B-to-A Three-State Outputs
$\chi B\chi$	B-to-A Data Inputs or A-to-B Three-State Outputs
GND	Ground
V _{CC}	Power

CD74LPT16952

Absolute Maximum Ratings

DC Input Voltage -0.5V to 7.0V
 DC Output Current 120mA

Operating Conditions

Operating Temperature Range -40°C to 85°C
 Supply Voltage to Ground Potential
 Inputs and V_{CC} Only -0.5V to 7.0V
 Supply Voltage to Ground Potential
 Outputs and D/O Only -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} (°C/W)
 TSSOP Package 85
 SSOP Package 70
 Maximum Junction Temperature 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS	MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T _A = -40°C to 85°C, V _{CC} = 2.7V to 3.6V						
Input HIGH Voltage (Input Pins)	V _{IH}	Guaranteed Logic HIGH Level	2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V _{IH}	Guaranteed Logic HIGH Level	2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V _{IL}	Guaranteed Logic LOW Level	-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I _{IH}	V _{CC} = Max V _{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I _{IH}	V _{CC} = Max V _{IN} = V _{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I _{IL}	V _{CC} = Max V _{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I _{IL}	V _{CC} = Max V _{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I _{OZH}	V _{CC} = Max V _{OUT} = 5.5V	-	-	±1	µA
	I _{OZL}	V _{CC} = Max V _{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V _{IK}	V _{CC} = Min, I _{IN} = -18mA	-	-0.7	-1.2	V
Output HIGH Current	I _{ODH}	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V (Note 7)	-36	-60	-110	mA
Output LOW Current	I _{ODL}	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V (Note 7)	50	90	200	mA
Output HIGH Voltage	V _{OH}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL} I _{OH} = -0.1mA	V _{CC} - 0.2	-	-	V
		I _{OH} = -3mA	2.4	3.0	-	V
	V _{CC} = 3.0V, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -8mA	2.4 (Note 9)	3.0	-	V
		I _{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL} I _{OL} = 0.1mA	-	-	0.2	V
		I _{OL} = 16mA	-	0.2	0.4	V
		I _{OL} = 24mA	-	0.3	0.5	V

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Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS	MIN	(NOTE 6) TYP	MAX	UNITS	
Short Circuit Current (Note 8)	I_{OS}	$V_{CC} = \text{Max (Note 7)}, V_{OUT} = \text{GND}$	-60	-85	-240	mA	
Power Down Disable	I_{OFF}	$V_{CC} = 0V, V_{IN} \text{ or } V_{OUT} \leq 4.5V$	-	-	± 100	μA	
Input Hysteresis	V_H		-	150	-	mV	
CAPACITANCE $T_A = 25^\circ C, f = 1\text{MHz}$							
Input Capacitance (Note 10)	C_{IN}	$V_{IN} = 0V$	-	4.5	6	pF	
Output Capacitance (Note 10)	C_{OUT}	$V_{OUT} = 0V$	-	5.5	8	pF	
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	$V_{CC} = \text{Max}$	$V_{IN} = \text{GND}$ or V_{CC}	-	0.1	10	μA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	$V_{CC} = \text{Max}$	$V_{IN} = V_{CC} - 0.6V$ (Note 11)	-	2.0	30	μA
Dynamic Power Supply Current (Note 12)	I_{CCD}	$V_{CC} = \text{Max}, \text{Outputs Open}$ $\overline{xOE} = \text{GND}$ One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	50	75	$\mu A/\text{MHz}$
Total Power Supply Current (Note 14)	I_C	$V_{CC} = \text{Max}, \text{Outputs Open}$ $f_1 = 10\text{MHz}, 50\% \text{ Duty Cycle}$ $\overline{xOE} = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	-	0.6	2.3	mA
		$V_{CC} = \text{Max}, \text{Outputs Open}$ $f_1 = 2.5\text{MHz}, 50\% \text{ Duty Cycle}$ $\overline{xOE} = \text{GND}$ 16 Bits Toggling	$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	-	2.1	4.7 (Note 13)	mA

Switching Specifications Over Operating Range (Note 15)

PARAMETER	SYMBOL	(NOTE 16) TEST CONDITIONS	CD74LPT16952A		CD74LPT16952B		UNITS
			(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	
Propagation Delay $\overline{xCLKAB}, \overline{xCLKBA}$ to $\overline{xBx}, \overline{xAx}$	$t_{PLH},$ t_{PHL}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	2.0	10.0	2.0	7.5	ns
Output Enable Time $\overline{xOEBA}, \overline{xOEAB}$ to $\overline{xAx}, \overline{xBx}$	$t_{PZH},$ t_{PZL}		1.5	10.5	1.5	8.0	ns
Output Disable Time (Note 18) $\overline{xOEBA}, \overline{xOEAB}$ to $\overline{xAx}, \overline{xBx}$	$t_{PHZ},$ t_{PLZ}		1.5	10.0	1.5	7.5	ns
Setup Time HIGH or LOW, $\overline{xAx}, \overline{xBx}$ to $\overline{xCLKAB}, \overline{xCLKBA}$	t_{SU}		2.5	-	2.5	-	ns

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Switching Specifications Over Operating Range (Note 15) (Continued)

PARAMETER	SYMBOL	(NOTE 16) TEST CONDITIONS	CD74LPT16952A		CD74LPT16952B		UNITS
			(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	
Hold Time HIGH or LOW, χ_{AX} , χ_{BX} to χ_{CLKAB} , χ_{CLKBA}	t_H	$C_L = 50\text{pF}$ $R_L = 500\Omega$	2.0	-	2.0	-	ns
Setup Time HIGH or LOW, χ_{CEAB} , χ_{CEBA} to χ_{CLKAB} , χ_{CLKBA}	t_{SU}		3.0	-	3.0	-	ns
Hold Time HIGH or LOW, χ_{CEAB} , χ_{CEBA} to χ_{CLKAB} , χ_{CLKBA}	t_H		2.0	-	2.0	-	ns
Pulse Width HIGH (Note 18) or LOW, χ_{CLKAB} or χ_{CLKBA}	t_W		3.0	-	3.0	-	ns
Output Skew (Note 19)	$t_{SK(O)}$		-	0.5	-	0.5	ns

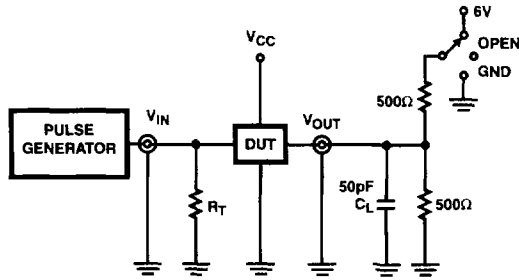
NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at $V_{CC} = 3.3\text{V}$, 25°C ambient and maximum loading.
7. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
8. This parameter is guaranteed but not tested.
9. $V_{OH} = V_{CC} - 0.6\text{V}$ at rated current.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input; all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 N_{CP} = Number of Clock Inputs at f_{CP}
 f_I = Input Frequency
 N_I = Number of Inputs at f_I
 All currents are in milliamps and all frequencies are in megahertz.
15. Propagation Delays and Enable/Disable times are with $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, normal range. For $V_{CC} = 2.7\text{V}$, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
16. See test circuit and wave forms.
17. Minimum limits are guaranteed but not tested on Propagation Delays.
18. This parameter is guaranteed but not production tested.
19. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

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Test Circuits and Waveforms



NOTE:

20. Pulse Generator for All Pulses: Rate \leq 1.0MHz; $Z_{OUT} \leq 50\Omega$;
 $t_f, t_r \leq 2.5ns$.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION	
TEST	SWITCH
t_{PLZ}, t_{PZL} , Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.
 R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

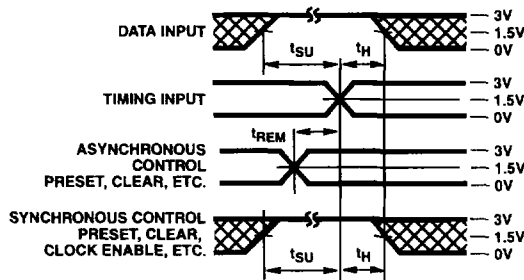


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

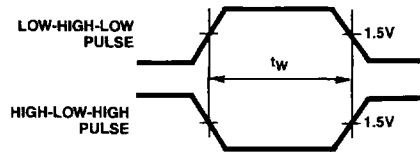


FIGURE 3. PULSE WIDTH

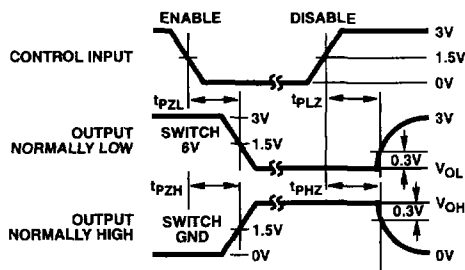


FIGURE 4. ENABLE AND DISABLE TIMING

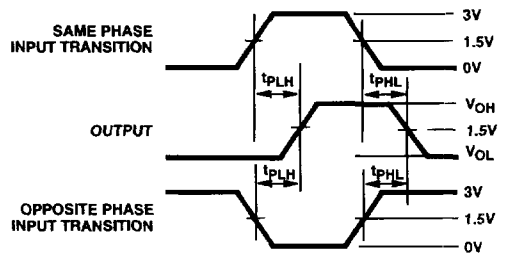


FIGURE 5. PROPAGATION DELAY