DSLVDS1001-1002EVM User's Guide

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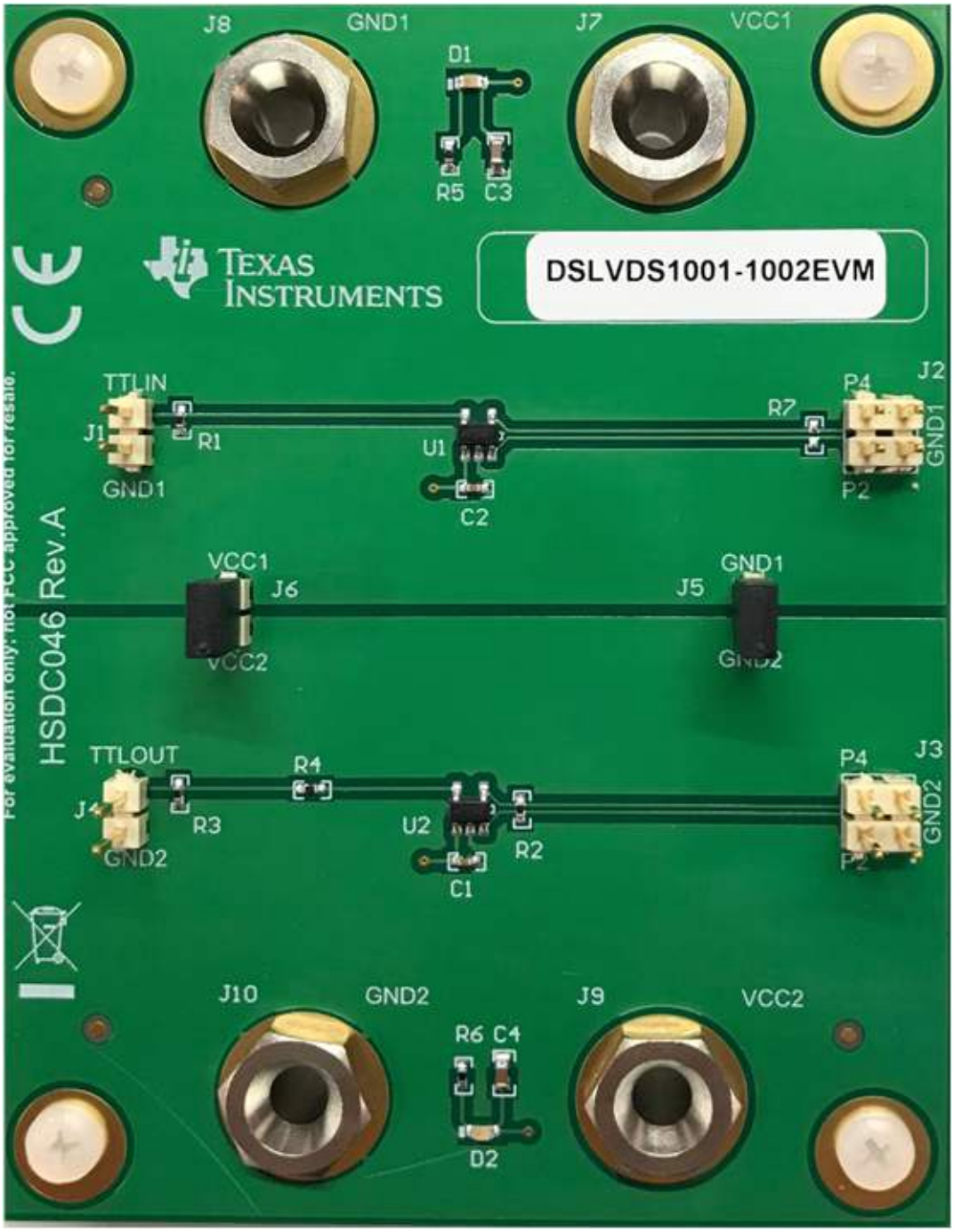
Trademarks

1 Introduction

The DSLVDS1001-1002EVM is an evaluation module designed for performance and functional evaluation of the Texas Instruments DSLVDS1001 3.3-V LVDS Single High Speed Differential Line Driver and DSLVDS1002 3.3-V LVDS Single High Speed Differential Line Receiver. With this kit, users can quickly evaluate the output waveform characteristics and signal integrity supported by the DSLVDS1001 and DSLVDS1002. Header pins allow access to the DSLVDS1001 and DSLVDS1002 inputs and outputs and also facilitate connection to lab equipment or user systems for performance evaluation.



1.1 Features

DSLVDS1001:

- Conforms to TIA/EIA-644-A Standard
- Up to 400-Mbps (200-MHz) Switching Rates
- 700-ps (100-ps Typical) Maximum Differential Skew
- 1.5-ns Maximum Propagation Delay
- Single 3.3-V Power Supply

DSLVDS1002:

- Compatible with ANSI TIA/EIA-644-A Standard
- Up to 400-Mbps (200-MHz) switching rates
- 100-ps differential skew (typical)
- 3.5-ns maximum propagation delay
- Single 3.3-V Power Supply

1.2 Applications

- Board to Board Communication
- Wireless/Telecom Infrastructure
- Medical/Health
- Multi-Function Printers
- Factory Automation and Control
- EPOS/ECR/Cash Drawer

2 Ordering Information

EVM ID	Device ID	Device Package
DSLVDS1001-1002EVM	DSLVDS1001, DSLVDS1002	SOT-23

3 Setup

The DSLVDS1001 is a LVDS Single High Speed Differential Line Driver, and the DSLVDS1002 is a LVDS Single High Speed Differential Line Receiver. When operating the DSLVDS1001-1002EVM, jumper setting definitions can be referenced in Table 1, while signal input and output connection descriptions can be found in Figure 1. When using the DSLVDS1001 and DSLVDS1002 together, the typical configuration is to connect the DSLVDS1001 outputs (J2) such that they drive the inputs of the DSLVDS1002 (J3). The setup configuration is shown in Figure 2

Table 1. Description of Jumper Settings

Component	Name	Comments
J5		Shunt for GND1 and GND2
J6		Shunt for VCC1 and VCC2
J7	GND1	GND for DSLVDS1001
J8	VCC1	3.3-V power supply for DSLVDS1001
J9	VCC2	3.3-V power supply for DSLVDS1002
J10	GND2	GND for DSLVDS1002

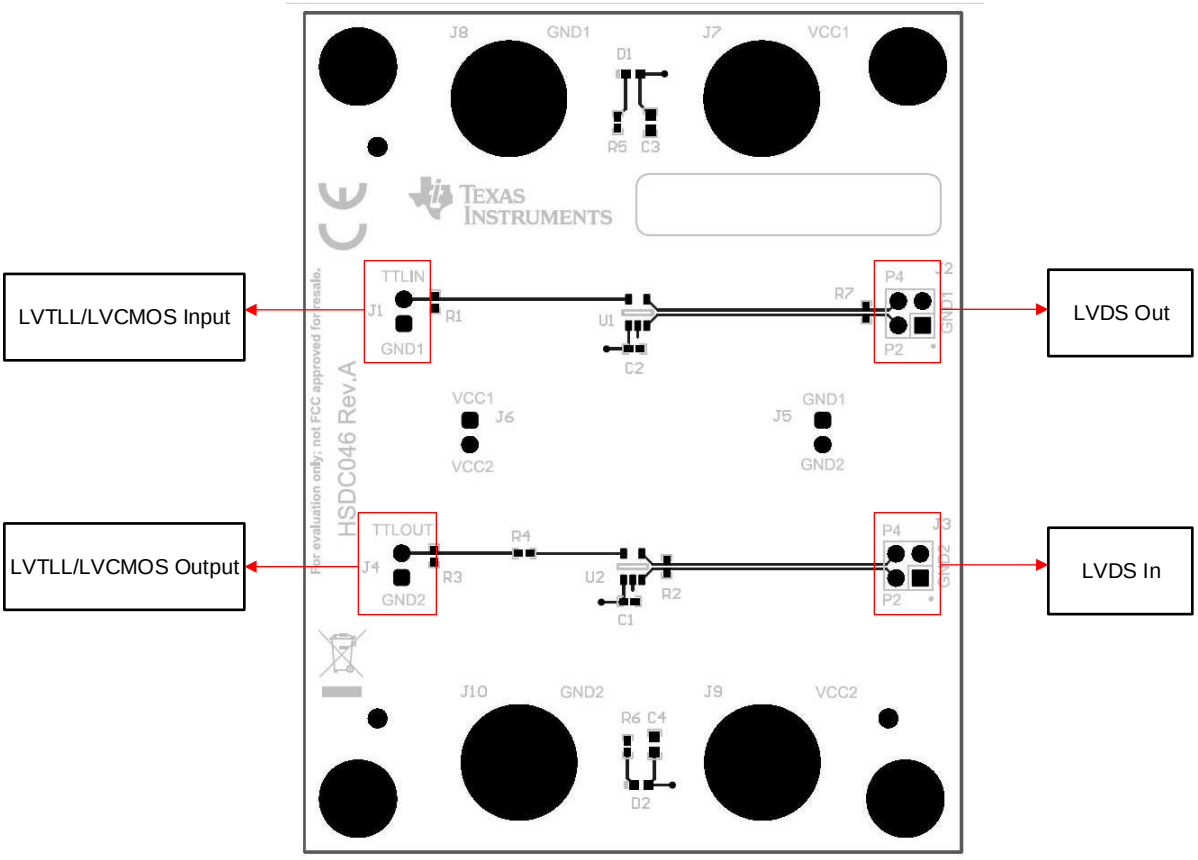


Figure 1. DSLVDS1001-1002EVM Input and Output Diagram

3.1 Hardware Description and Setup

3.1.1 Termination Resistor

By factory default, the DSLVDS1001-1002EVM comes with populated termination resistors R2 on the DSLVDS1002 inputs and unpopulated termination resistors R7 on the DSLVDS1001 outputs.

In order to measure LVDS signals properly, a 100-Ω termination resistor must be present across each differential pair at the point of measurement. However, if multiple 100-Ω termination resistors are placed across a differential pair between the transmitter and receiver, the signal becomes double terminated. Double termination should be avoided, since this reduces the output amplitude and noise margin.

Populate R7 with 100-Ω termination resistors

- if the DSLVDS1001 output is measured by a high-impedance differential probe.
- if the DSLVDS1001 output interfaces with an external load that does **not** have an appropriate 100-Ω differential termination.

Remove R7 (or keep R7 unpopulated)

- if the DSLVDS1001 output interfaces with a DSLVDS1002 input by connecting J4 to J1.
- if the DSLVDS1001 output interfaces with an external load that has an appropriate 100-Ω differential termination.

3.1.2 Hardware Setup

DSLVDS1001-1002EVM can be powered using a single power supply or two separate power supplies.

When using a single power supply, J5 and J6 should be connected with jumpers. When using two separate power supplies, J5 and J6 should be left open.

1. Connect a 3.3-V DC power supply (30 mA max) to the EVM. The LEDs D1 and D2 should turn on to specify that the board is powered.
2. Apply a high-speed 3.3-V LVTTL/LVCMOS signal to the DSLVDS1001 inputs on header J1.
3. The DSLVDS1001 LVDS output signals can be measured differentially on an oscilloscope by applying a Tektronix P6247 probe or equivalent differential probe at header J4 to measure the differential signal across the 100-Ω termination resistors R7, when R7 is populated. The expected output waveform is a ±350-mV LVDS signal.
4. Apply a high-speed ±350-mV (700-mV_{pp} differential) LVDS signal to the DSLVDS1002 inputs on header J3. If desired, LVDS output from DSLVDS1001 can be connected to LVDS input of DSLVDS1002. If this is done, make sure R7 is not populated to avoid double-termination.
5. The DSLVDS1002 LVTTL/LVCMOS output signals can be measured on an oscilloscope by applying a Tektronix P6247 probe or equivalent differential probe at header J4.

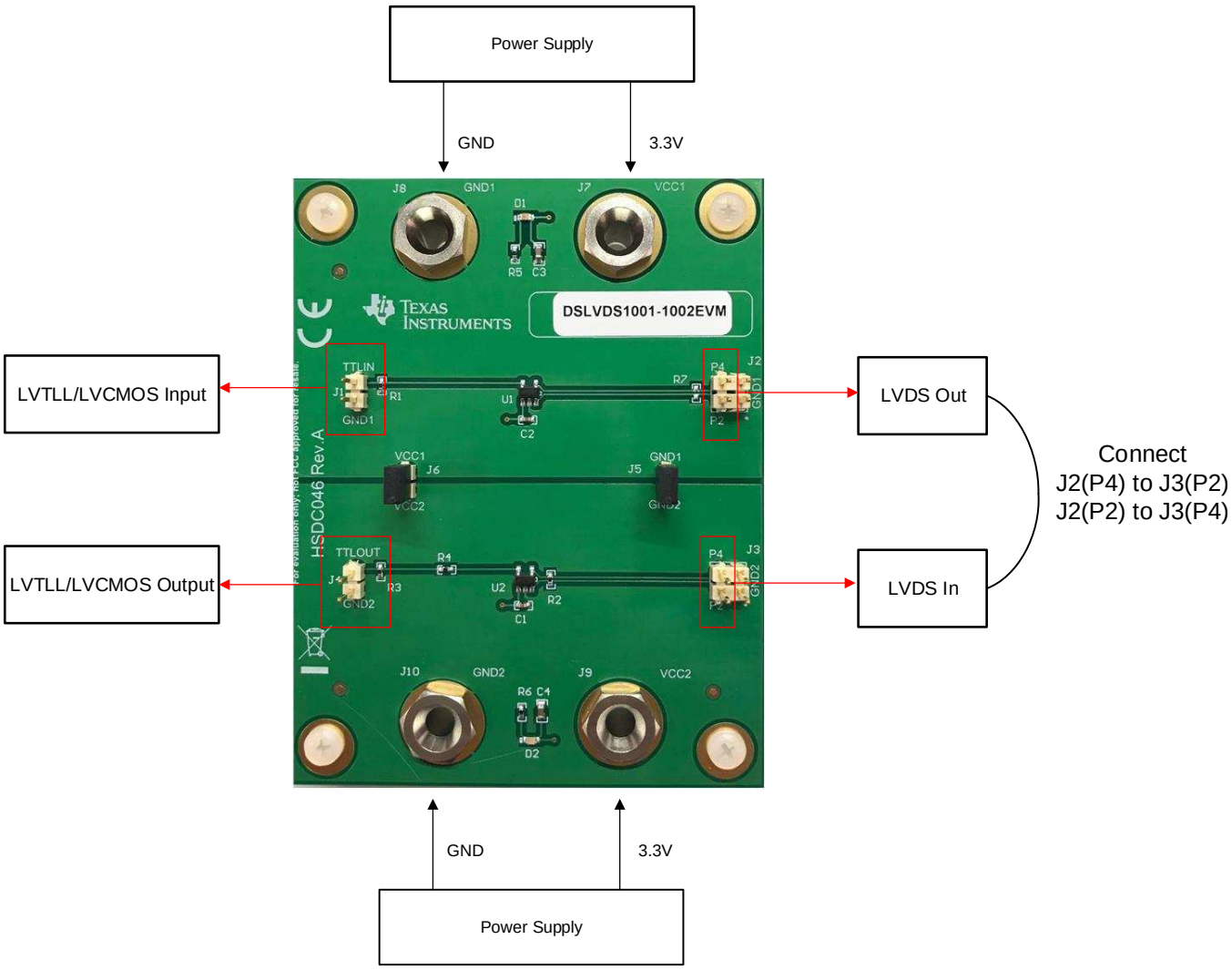


Figure 2. DSLVDS1001-1002EVM Setup Configuration

3.2 DSLVDS1001-1002EVM Performance Plots

The following plots show typical waveforms measured on the DSLVDS1001-1002EVM inputs and outputs using the hardware setup in Figure 2. For these measurements, the following parameters were used:

- Operating Frequency: 200 MHz (400 Mbps)
- DSLVDS1001 Input: 3.3 V LVCMOS square wave to J1
- DSLVDS1002 Input: LVDS signal to LVDS IN± from DSLVDS1001 output LVDS OUT1±. 100-Ω termination resistor R7 not populated
- DSLVDS1002 Output: Measured at TTLOUT

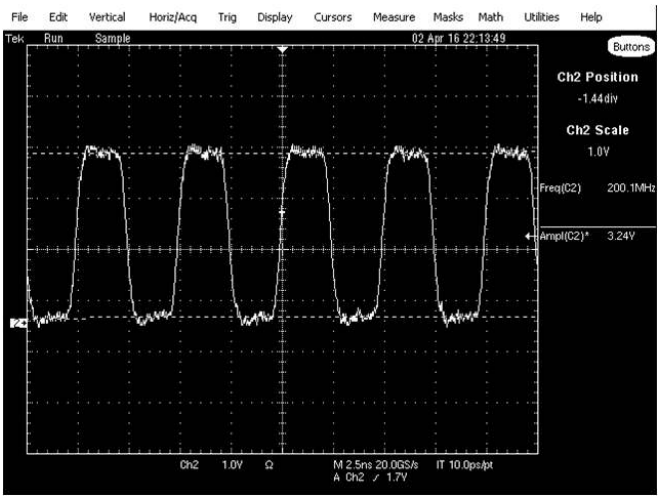


Figure 3. DSLVDS1001 3.3 V LVCMOS Input

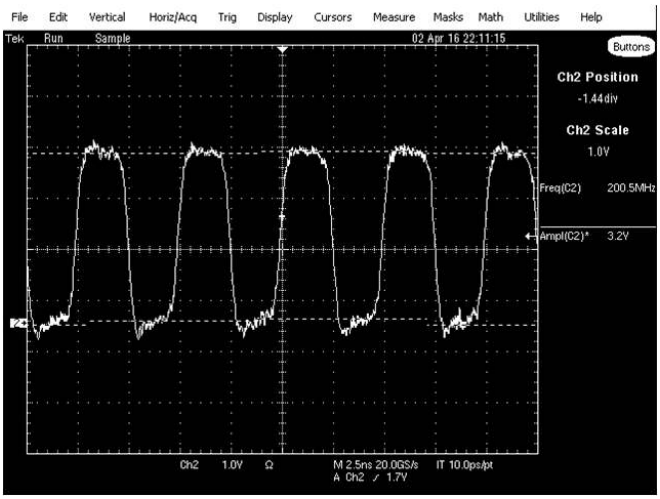


Figure 4. DSLVDS1002 LVCMOS Output

4 Board Layout

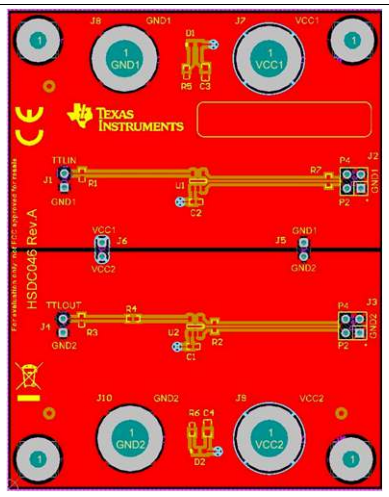


Figure 5. DSLVDS1001-1002EVM Top Layer

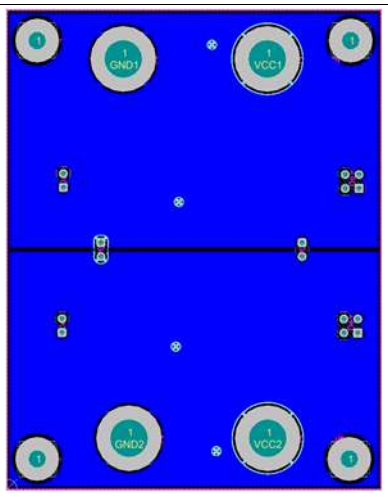
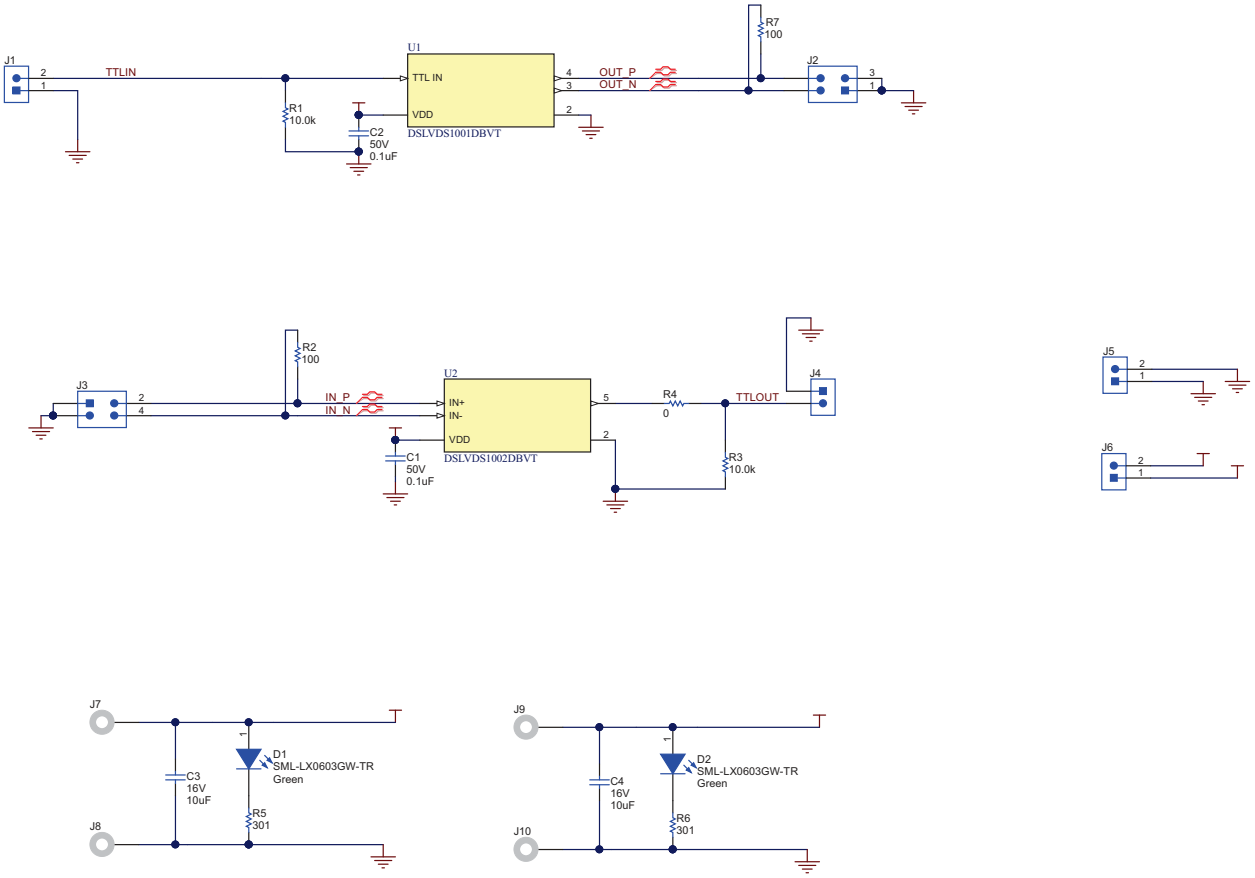


Figure 6. DSLVDS1001-1002EVM Bottom Layer

5 Schematic



6 Bill of Materials

Table 2. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
PCB	1		Printed Circuit Board		HSDC046	Any
C1, C2	2	0.1 µF	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0402	0402	C1005X7R1H104K050BB	TDK
C3, C4	2	10 µF	CAP, CERM, 10 µF, 16 V, +/- 20%, X5R, 0603	0603	EMK107BBJ106MA-T	Taiyo Yuden
D1, D2	2	Green	LED, Green, SMD	LED, GREEN, 0603	SML-LX0603GW-TR	Lumex
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1, J4, J5, J6	4		Header, 100 mil, 2 × 1, Gold, TH	2 × 1 Header	TSW-102-07-G-S	Samtec
J2, J3	2		Header, 100 mil, 2 × 2, Gold, TH	2 × 2 Header	TSW-102-07-G-D	Samtec
J7, J8, J9, J10	4		Standard Banana Jack, Uninsulated	Pomona_3267	3267	Pomona Electronics
LBL1	1			PCB Label 1.25 × 0.250 inch	THT-13-457-10	Brady
R1, R3	2	10.0 kΩ	RES, 10.0 kΩ, 1%, 0.063 W, 0402	0402	RC0402FR-0710KL	Yageo America
R2	1	100 Ω	RES, 100 Ω, 1%, 0.063 W, 0402	0402	RC0402FR-07100RL	Yageo America
R4	1	0 Ω	RES, 0 Ω, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GE0R00X	Panasonic
R5, R6	2	301 Ω	RES, 301 Ω, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402301RFKED	Vishay-Dale
SH-J1, SH-J2	2	1 × 2	Shunt, 100 mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
U1	1		Single High Speed Differential Driver, 5-pin SOT-23, Pb-Free	DBV0005A	DSLVDS1001DBVT	Texas Instruments
U2	1		3-V LVDS Single CMOS Differential Line Receiver, 5-pin SOT-23, Pb-Free	DBV0005A	DSLVDS1002DBVT	Texas Instruments
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
R7	0	100	RES, 100, 1%, 0.063 W, 0402	0402	RC0402FR-07100RL	Yageo America

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