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Evaluating the AD5686R 16-Bit, Quad Channel, Voltage Output DAC

FEATURES

Full featured evaluation board for the AD5686R
On-board references
Various link options
PC control in conjunction with the Analog Devices, Inc., SDP

EVALUATION KIT CONTENTS

EVAL-AD5686RSDZ board

HARDWARE REQUIRED

EVAL-SDP-CB1Z (SDP-B) board or EVAL-SDP-CS1Z (SDP-S) board, must be purchased separately

SOFTWARE REQUIRED

ACE evaluation software available for download from the EVAL-AD5686RSDZ product page

GENERAL DESCRIPTION

This user guide details the operation of the EVAL-AD5686RSDZ evaluation board for the AD5686R quad-channel, voltage output, digital-to-analog converter (DAC).

The EVAL-AD5686RSDZ evaluation board is designed to help users quickly prototype AD5686R circuits and reduce design time. The AD5686R operates from a single 2.7 V to 5.5 V supply. The AD5686R incorporates an internal 2.5 V reference to give an output voltage of 2.5 V or 5 V. The evaluation board also incorporates additional voltage references.

The EVAL-AD5686RSDZ evaluation board interfaces to the USB port of a PC via a system demonstration platform (SDP) board. The analysis control evaluation (ACE) software is available for download from the EVAL-AD5686RSDZ product page to use with the evaluation board to allow the user to program the AD5686R. A PMOD connection is also available to allow the connection of microcontrollers to the evaluation board without the SDP board. Note that when a microcontroller is used through the PMOD connection, the SDP board must be disconnected, and the user is unable to operate the ACE software.

The EVAL-AD5686RSDZ evaluation board is compatible with any Analog Devices SDP board, which can be purchased separately. A typical connection between the EVAL-AD5686RSDZ and the EVAL-SDP-CS1Z board (SDP-S controller board) is shown in Figure 1.

For full details, see the AD5686R data sheet, which must be consulted in conjunction with this user guide when using the evaluation board.

EVAL-AD5686RSDZ CONNECTED TO THE SDP-S BOARD

Figure 1.

TABLE OF CONTENTS

REVISION HISTORY

7/2017—Rev. A to Rev. B

Reorganized Layout ..... Universal
Added Evaluation Board Quick Start Procedures Section, Figure 2, and Figure 3; Renumbered Sequentially 3
Moved Installing the Software Section and Initial Setup Section 3
Changes to Installing the Software Section and Initial Setup Section 3
Added Block Diagram and Description Section, Figure 4, and Table 1; Renumbered Sequentially 4
Deleted Evaluation Board Software Section, Figure 2, Figure 3 Figure 4, and Figure 5 5
Added Memory Map Section, Figure 5, and Figure 6 5
Deleted Figure 6, Software Operation Section, Write to Input Register Section, Write to Input and DAC Register Section, Update DAC Register from Input Register Section, LDAC Control Section, GAIN Control Section, Reference Control Section and Power-Down Control Section 6
Moved Evaluation Board Hardware Section, Power Supplies Section, LDO Recommendation Section, Test Points Section, Voltage References Section, Link Options Section, Table 2, Table 3, and Table 4 6
Changes to Table 2 and Table 4 6
Deleted LDAC Mask Register Section and Full SPI Command Section 7
Moved Table 5 7

1/2016—Rev.0 to Rev. A

Changes to Title 1
Changes to Running the Software Section 5
Added Figure 5; Renumbered Sequentially 5
Changes to Figure 6 6
Added LDAC Mask Register Section 7
Changes to Figure 7 8
Changes to Figure 8 9
Changes to Figure 9 and Figure 10 10
Changes to Figure 11 11
Changes to Table 5 12

5/2015—Revision 0: Initial Version

EVALUATION BOARD QUICK START PROCEDURES

INSTALLING THE SOFTWARE

The EVAL-AD5686RSDZ evaluation board uses the ACE evaluation software, a desktop software application that allows the evaluation and control of multiple evaluation systems.

The ACE installer installs the necessary SDP drivers and the Microsoft® .NET Framework 4 by default. The ACE software is available for download from the EVAL-AD5686RSDZ product page and must be installed before connecting the SDP board to the USB port of the PC, to ensure that the SDP board is recognized with it connects to the PC. For full instructions on how to install and use this software, see the ACE software pages on the Analog Devices website.

After the installation is finished, the EVAL-AD5686RSDZ evaluation board plug in appears when the ACE software is opened.

INITIAL SETUP

To set up the evaluation board, take the following steps:

1. Connect the evaluation board to the SDP board, and then connect a USB cable between the SDP board and the PC.
2. Run the ACE application. The EVAL-AD5686RSDZ board plug-ins appear in the attached hardware section of the **Start** tab.
3. Double-click the board plug-in to open the board view seen in Figure 2.
4. Double-click the AD5686R chip to access the chip block diagram. This view provides a basic representation of functionality of the board. The main function blocks of the board are labeled in Figure 3.

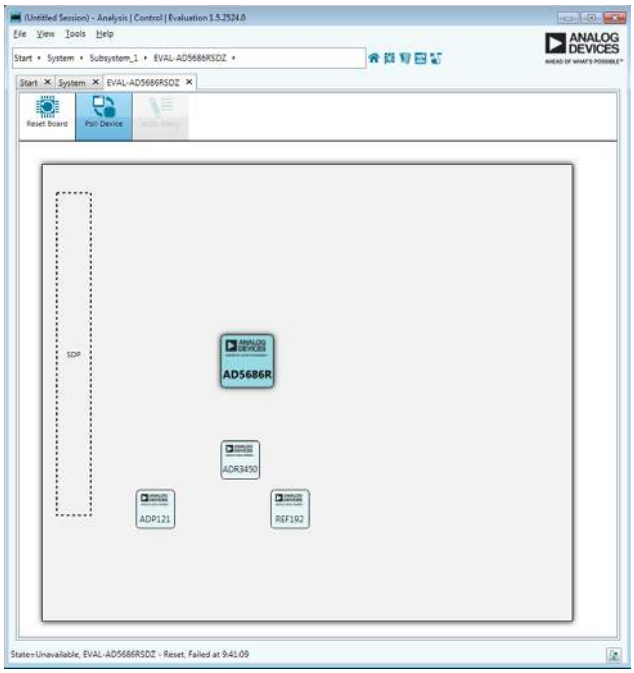

Figure 2. Board View of the EVAL-AD5686RSDZ

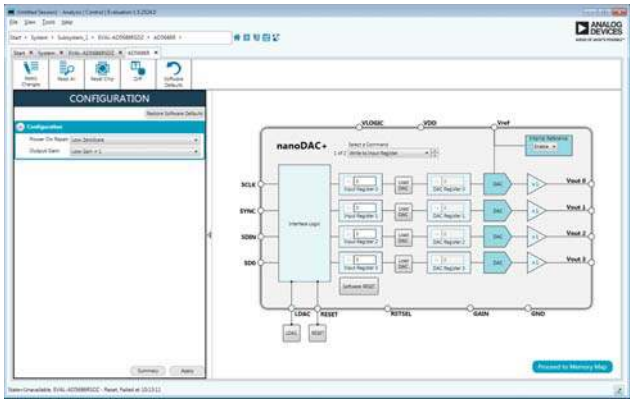

Figure 3. Chip Block Diagram View of the AD5686R

BLOCK DIAGRAM AND DESCRIPTION

The EVAL-AD5686RSDZ software is organized to appear similar to the functional block diagram shown in the AD5686R data sheet. Therefore, correlating the functions on the EVAL-AD5686RSDZ board with the description in the AD5686R data sheet is simplified.

A full description of each block, register, and its settings is given in the AD5686R data sheet.

Some of the blocks and their functions are described in this section as they pertain to the evaluation board. The block diagram is shown in Figure 4. Table 1 describes the functionality of each block.

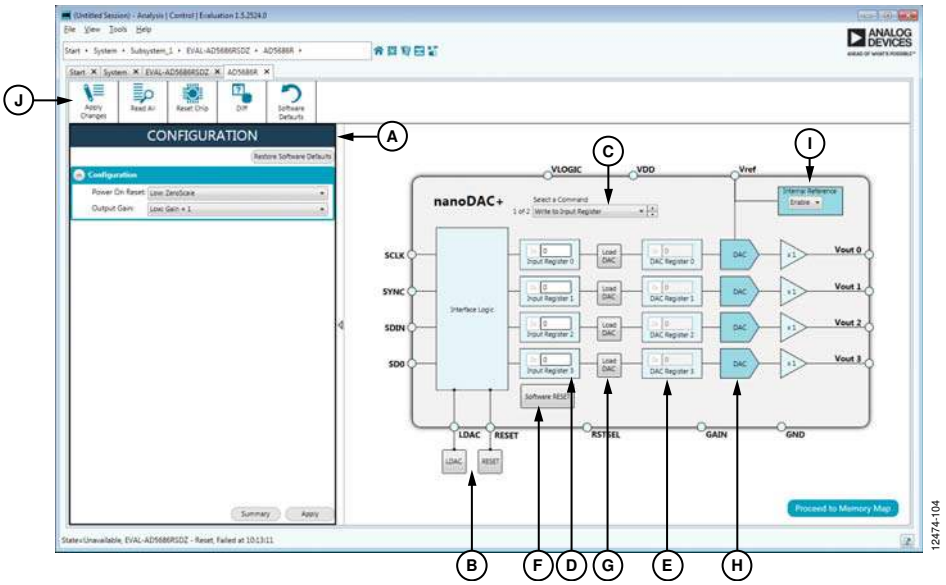

Figure 4. AD5686R Block Diagram with Labels

Table 1. Block Diagram Functions (See Figure 4 for Labels)

Label	Button/Function Name	Function
A	**CONFIGURATION** wizard	Used to set the initial configuration of the board. Select the reference gain case from the **Output Gain** dropdown box. A gain of 1 is the default. After setting up the initial configuration, click **Apply** to apply the values. These settings can be modified at any stage while evaluating the board.
B	**LDAC** and **RESET** (GPIO buttons)	Act as external GPIO pulses to the $\overline{\text{LDAC}}$ and $\overline{\text{RESET}}$ pins. The **LDAC** button transfers data from the input registers (D) to the DAC registers (E). The **RESET** button clears all data from the input registers and DAC registers. These buttons are live; therefore, there is no need to click **Apply Changes** (J).
C	**Select a Command**	The command option dropdown box selects how the data being transferred to the device affects the input and DAC registers. After a data value is entered in an input register (D), this menu determines the internal DAC registers affected by updating the input register (D). After a new value is written in the input register (D), the data can be transferred to the DAC input register or to the DAC input register and the DAC register simultaneously. If the data is transferred to both registers, the channel DAC register (E) reflects the new value.
D	**Input Register 0** to **Input Register 3**	16-bit data word to be transferred to the device. Click **Apply Changes** (J) to transfer this 16-bit data word to the device.
E	**DAC Register 0** to **DAC Register 3**	Displays the value that is currently present in the DAC register on the device. Update the DAC registers by selecting the appropriate command option or by toggling **LDAC** (B).
F	**Software RESET**	Returns the evaluation board and software to default values. This button is live; therefore, there is no need to click **Apply Changes**.
G	**Load DAC**	The user can individually control which channel loads the values from the input registers to the DAC registers.
H	**DAC**	DAC configuration options provide access to individual channel configuration options such as power-down options and hardware $\overline{\text{LDAC}}$ mask enable/disable settings.
I	**Internal Reference**	Select **Enable** from this setting to enable the on-chip reference for the board. If **Disable** is selected, an external reference must be applied. This control is only available on the AD5686R.
J	**Apply Changes**	Applies all modified values to the device. Note that if an evaluation board is not connected, values entered into the input registers are not transferred to the DAC registers.

MEMORY MAP

All registers are fully accessible from the **AD5686R Memory Map** tab, as shown in Figure 5. To navigate to this tab, click **Proceed to Memory Map**, shown in Figure 4. This tab allows registers to be edited at a bit level. The bits shaded in dark gray are read only bits and cannot be accessed from the ACE software. All other bits are toggled.

Clicking **Apply Changes** transfers data to the device. All changes in this tab correspond to the block diagram. For example, if the internal register bit is enabled, it displays as enabled on the block diagram. Any bits or registers that are shown in bold in the memory map tab are modified values that have not been transferred to the board (see Figure 6). Click **Apply Changes** to transfer the data to the evaluation board.

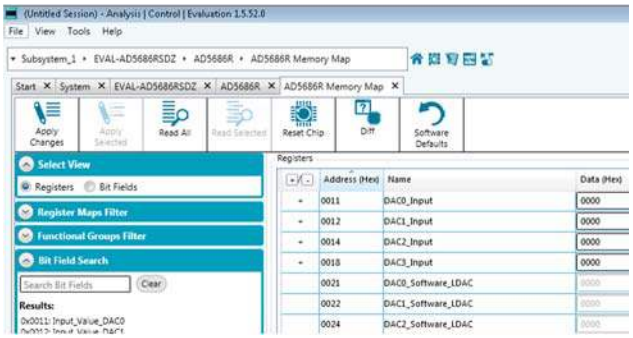

*Figure 5. **AD5686R Memory Map** Tab*

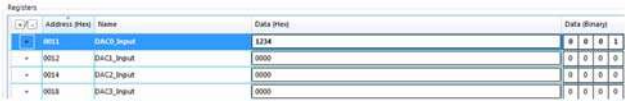

Figure 6. AD5686R Memory Map with Unapplied Changes in the DAC0_Input Register

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The EVAL-AD5686RSDZ evaluation board provides an on-board, 3.3 V regulator powered through the USB supply. If a different supply is required or if the board is controlled through the PMOD, an external supply must be provided via the EXTSUP connector. See Table 2 for more details.

Both AGND and DGND inputs are provided on the board. The AGND and DGND planes are connected at one location close to the AD5686R. To avoid ground loop problems, it is recommended that AGND and DGND not be connected elsewhere in the system.

All supplies are decoupled to ground with 10 µF tantalum and 0.1 µF ceramic capacitors.

LDO RECOMMENDATION

The ADP7118 low dropout (LDO) linear regulator (maximum V_{IN} = 20 V) is recommended to power the V_{DD} rail for maximal performance. A 4.7 Ω resistor in series with the input capacitor of the ADP7118 adds additional rejection at higher frequencies to reduce any power supply ripple artifacts below the noise floor. The ADP162 is recommended for powering the V_{LOGIC} rail.

TEST POINTS

The evaluation board has various test points for debugging and monitoring purposes. These test points are described in Table 5.

VOLTAGE REFERENCES

The AD5686R provides an internal voltage reference. The evaluation board provides external references with values of 2.5 V and 5 V. Note that using the ADR3450 requires the use of an external supply through the EXTSUP connector (see Table 4).

LINK OPTIONS

A number of link options are incorporated in the EVAL-AD5686RSDZ evaluation board and must be set for the required operating conditions before using the board. The functions of these link options are described in Table 4.

Table 3 lists the positions of the different links controlled by the PC via the USB port. An SDP board operating in single-supply mode is required.

Table 2. Power Supply Connectors

Connector	Label	External Voltage Supplies Description
EXTSUP, Pin 1	EXTSUP	External analog power supply from 2.7 V to 5.5 V, V_{DD}.
EXTSUP, Pin 2	EXTSUP	Analog ground.
EXTREF, Pin 1	EXTREF	External voltage reference, V_{LOGIC}. It is 3.3 V when the evaluation board is controlled through the SDP board. It is 1.8 V to 5.5 V when the evaluation board is controlled through an external connector.
EXTREF, Pin 2	EXTREF	Analog ground.

Table 3. Link Options Setup for SDP Control (Default)

Link	Option
PWRSEL	3.3 V
REF	Not connected
P1	Not connected

Table 4. Link Functions

Link	Description
PWRSEL	This link selects the DAC analog voltage source. There are three options, as follows. The 3.3V option selects the on-board voltage source from the ADP121. The USB_SUP option selects the USB supply from Pin 5 of the 120-pin connector of the SDP board. The EXT_SUP option selects an external supply voltage (EXTSUP connector).
REF	This link selects the reference source. There are four options, as follows. The not connected option uses the 2.5 V internal reference. The EXT_REF option selects an external reference source (EXTREF connector). The 2.5V option selects the on-board reference from the REF192. The 5V option selects the on-board reference from the ADR3450. This reference requires an external supply.
P1	The P1 link selects the DAC digital voltage source. There are two options, as follows. The connected option shorts V_{DD} and V_{LOGIC}. Use this option only when the SDP board is not connected. The not connected option opens the connection of V_{DD} and V_{LOGIC}. Use this option when using the SDP board.

Table 5. Test Point Descriptions

Test Point	Description
AGND	Analog ground.
DGND	Digital ground.
SCLK/A0	Serial clock input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz. This signal is named SCLK_A0 in Figure 7.
SDO/SDA	Serial data output. This output daisy-chains a number of AD5686R/AD5685R/AD5684R devices together, or it can be used for read back. The serial data is transferred on the rising edge of SCLK and is valid on the falling edge of the clock. This signal is named SDO_SDA in Figure 7.
SYNCB/SCL	Active low control input. This is the frame synchronization signal for the input data. When SYNCB goes low, data is transferred in on the falling edges of the next 24 clocks. This signal is named SYNCB_SCL in Figure 7.
SDIN/A1	Serial data input. This device has a 24-bit input shift register. Data is clocked into the register on the falling edge of the serial clock input. This signal is named SDIN_A1 in Figure 7.
VOUTA to VOUTD	Analog output voltage from DAC A to DAC D, respectively. The output amplifier has rail-to-rail operation.

EVALUATION BOARD SCHEMATICS AND ARTWORK

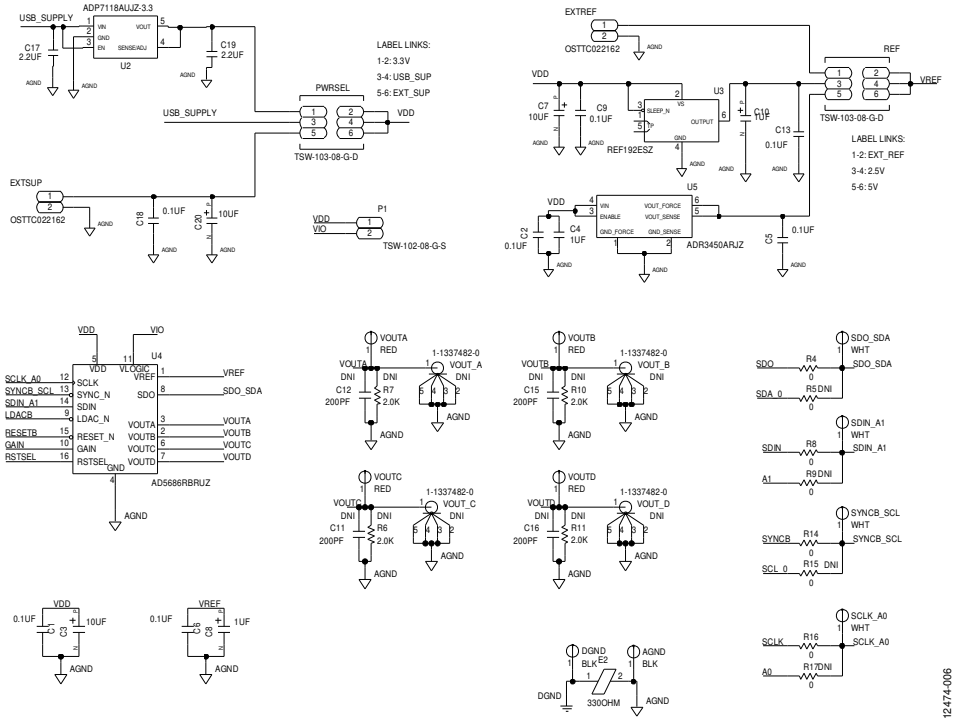

Figure 7. EVAL-AD5686RSDZ Schematic—Power Supply and Signal Routes

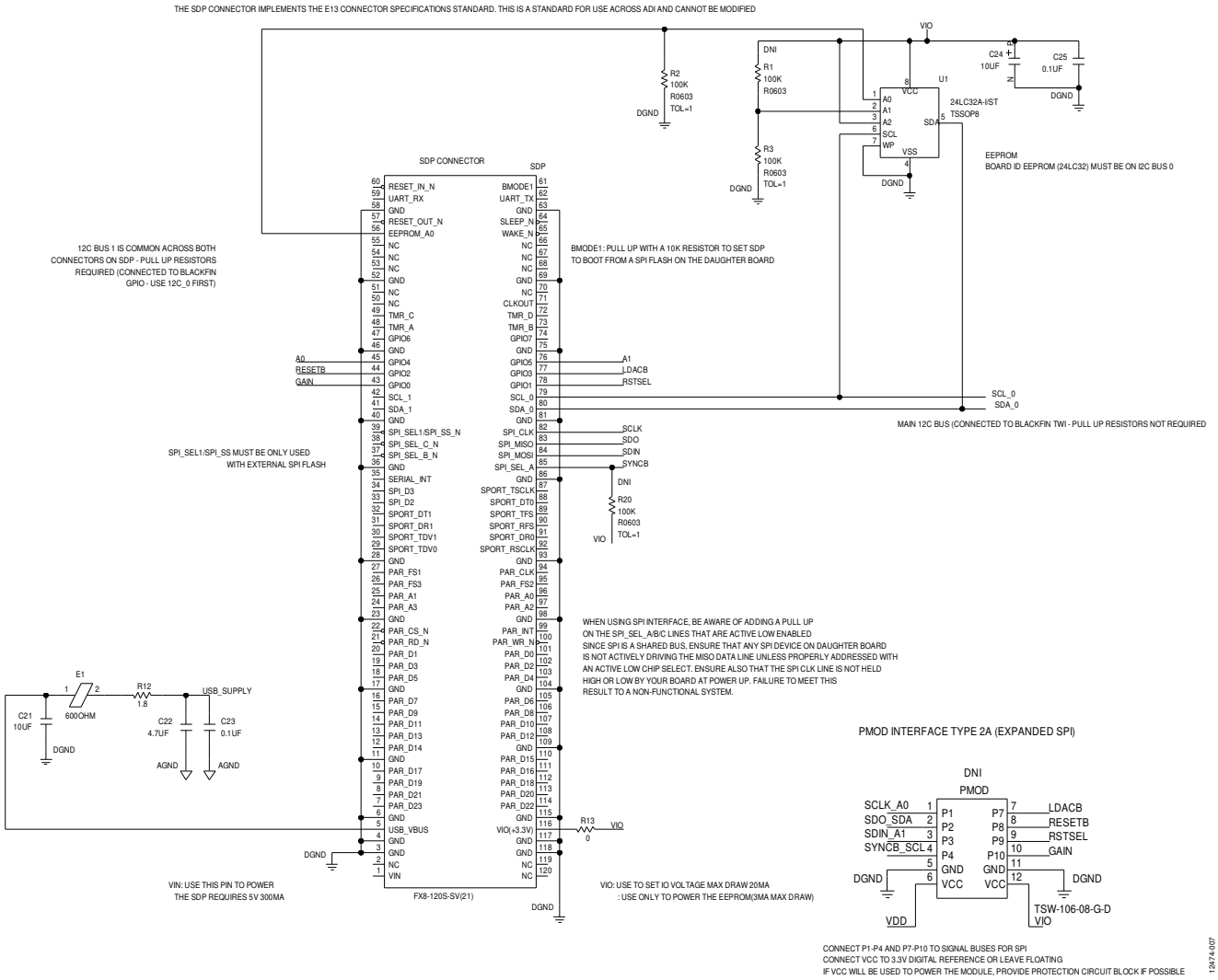

Figure 8. EVAL-AD5686RSDZ Schematic—SDP Connector

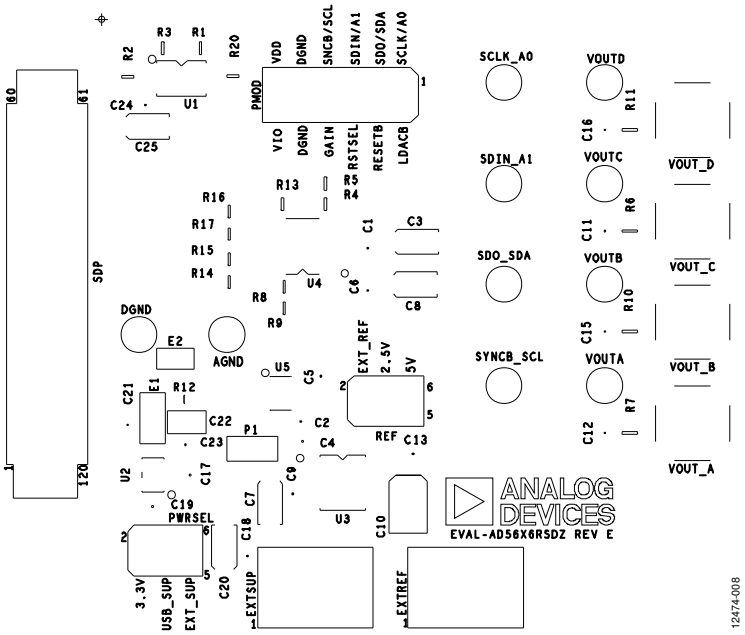

Figure 9. EVAL-AD5686RSDZ Component Placement

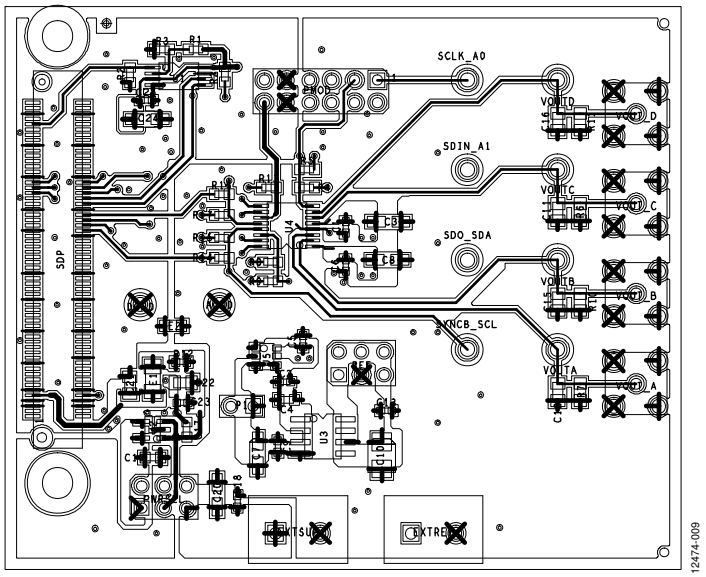

Figure 10. EVAL-AD5686RSDZ Top Side Routing

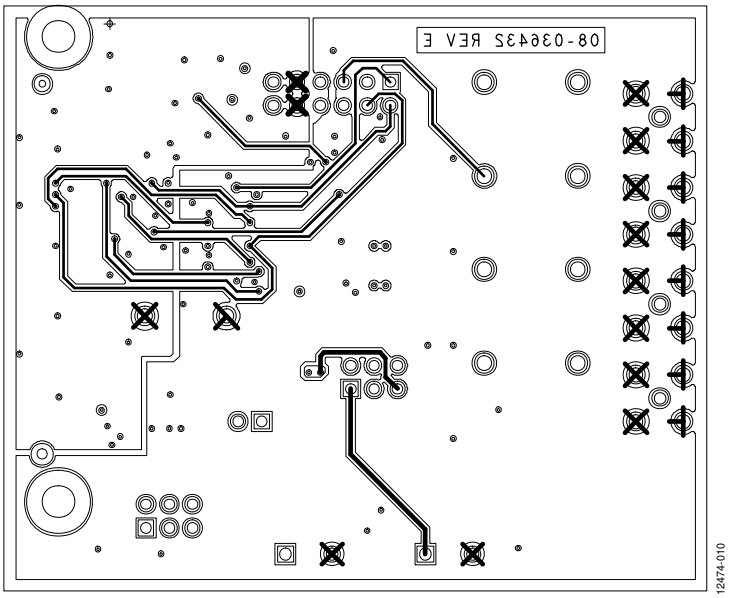

Figure 11. EVAL-AD5686RSDZ Bottom Side Routing

ORDERING INFORMATION

BILL OF MATERIALS

Table 6.

Quantity	Reference Designator	Description	Supplier/Part Number[1]
1	U1	32 kb, I²C serial EEPROM (24LC32)	FEC/1331330
1	U2	150 mA, low quiescent current, CMOS linear regulator	Analog Devices/ADP121
1	U3	2.5 V, precision micropower, low dropout, low voltage reference	Analog Devices/REF192
1	U4	Quad, 16-bit *nano*DAC+ with 2 ppm/°C on-chip reference and SPI interface	Analog Devices/AD5686R
1	U5	Micropower, high accuracy, 5.0 V voltage reference	Analog Devices/ADR3450
6	C1, C2, C5, C6, C18, C25	Capacitors, 0.1 µF, 16 V, 0402	Generic
3	C4, C17, C19	Capacitors, 1 µF, 25 V, X5R	Generic
3	C3, C20, C24	Capacitors, 10 µF, 10 V, tantalum	Generic
1	C8	Capacitor, 1 µF, 16 V, tantalum	Generic
1	C21	Capacitor, 10 µF, 25 V, X5R	Generic
1	C22	Capacitor, 4.7 µF, 25 V, X5R	Generic
1	C23	Capacitor, 0.1 µF, 25 V, X8R	Generic
1	E1	Ferrite bead, 600 Ω	Generic
1	E2	Ferrite bead, 330 Ω	Generic
2	EXTREF, EXTSUP	2-pin terminal blocks	Generic
1	P1	2-pin link/jumper	Generic
2	REF, PWRSEL	6-pin link/jumpers	Generic
1	R12	Resistor, 1.8 Ω, 5%, 1/10 W, thick film chip	Generic
1	R13	Resistor, 0 Ω, SMD	Generic
4	R4, R8, R14, R16	Resistors, 0 Ω, 5%, 1/16 W, 0603	Generic
2	R2, R3	Resistors, 100 kΩ, 1%, 1/10 W	Generic
1	SDP	120-pin female connector	FEC/ 1324660 or Digi-Key H1219-ND
2	AGND, DGND	Black test points	Generic
4	SCLK_A0, SDIN_A1, SDO_SDA, SYNCB_SCL	White test points	Generic
4	VOUTA to VOUTD	Red test points	Generic
19	PMOD, C11, C12, C15, C16, R1, R5 to R7, R9 to R11, R15, R17, R20, VOUT_A to VOUT_D	Do not insert/do not populate	Not inserted

[1] Generic indicates that any part with the specified value, size, and rating can be used.

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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