BLC2425M9LS250

Power LDMOS transistor

Rev. 3 — 20 December 2016

AMPLEON

Product data sheet

1. Product profile

1.1 General description

250 W LDMOS power transistor for Industrial, Scientific and Medical (ISM) applications at frequencies from 2400 MHz to 2500 MHz.

The BLC2425M9LS250 is designed for high-power CW applications and is assembled in a high performance plastic package.

Table 1. Typical performance

RF performance at V_{DS} = 32 V; I_{Dq} = 20 mA; T_{case} = 25 °C in a class-AB application circuit.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW	2450	32	250	18	61
CW pulsed [1]	2450	32	250	18.5	62

[1] t_p = 100 μs; δ = 10 %

1.2 Features and benefits

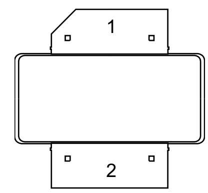
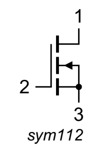
- High efficiency
- Excellent ruggedness
- Integrated ESD protection
- Designed for broadband operation (2400 MHz to 2500 MHz)
- Internally input and output matched
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for CW applications in the 2400 MHz to 2500 MHz frequency range such as ISM applications and heating.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
flange	source		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC2425M9LS250	-	air cavity plastic earless flanged package; 2 leads	SOT1270-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–6	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 250 W	0.290	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.7 mA	65.00	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 32 V; I_D = 20 mA	1.15	1.70	2.25	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	4.20	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	53.50	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	40.00	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 13.5 A	-	20.16	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 9.45 A	-	52.50	-	mΩ

Table 7. RF characteristics

Test signal: CW at 2450 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 20 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 250 W	16.3	18.5	-	dB
RL_{in}	input return loss	P_L = 250 W	-	−15	−10	dB
η_D	drain efficiency	P_L = 250 W	55	58.5	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLC2425M9LS250 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases with a time rate of 15 ms/degree under the following conditions: V_{DS} = 32 V; I_{Dq} = 20 mA; P_L = 250 W (CW); f = 2450 MHz; T_{case} = 25 °C.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data. Typical values unless otherwise specified. I_{Dq} = 20 mA; V_{DS} = 32 V.

f	Z_S [1]	Z_L [1]
(MHz)	(Ω)	(Ω)
2400	0.9 − 5.0j	1.9 − 0.4j
2450	1.0 − 5.4j	1.7 − 1.4j
2500	2.0 − 6.1j	1.7 − 1.1j

[1] Z_S and Z_L defined in Figure 1.

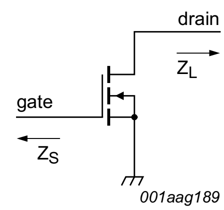
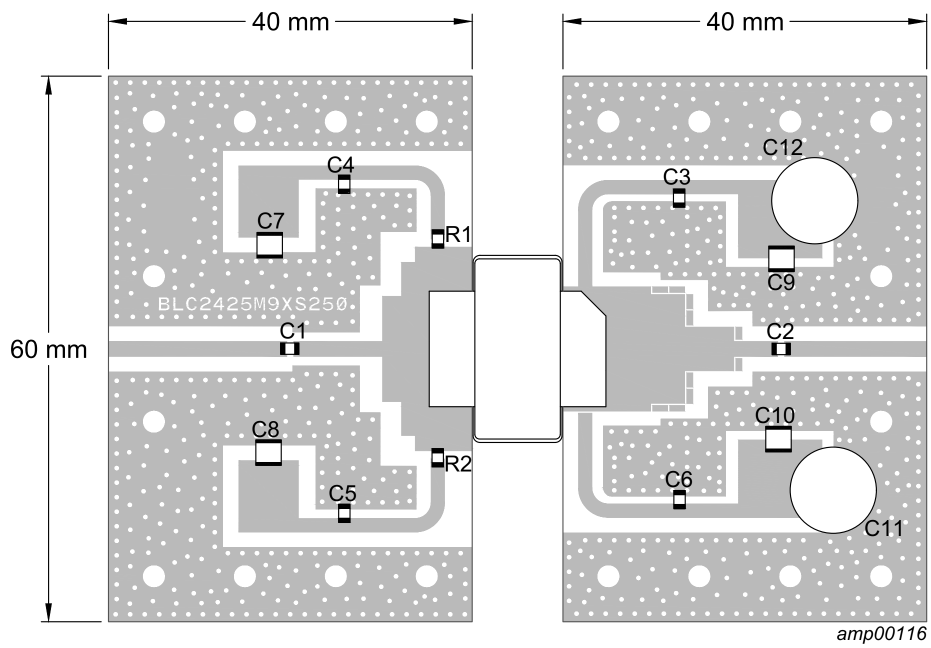


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers 6035HTC; thickness = 0.762 mm; thickness copper plating = 35 μm.

See Table 9 for a list of components.

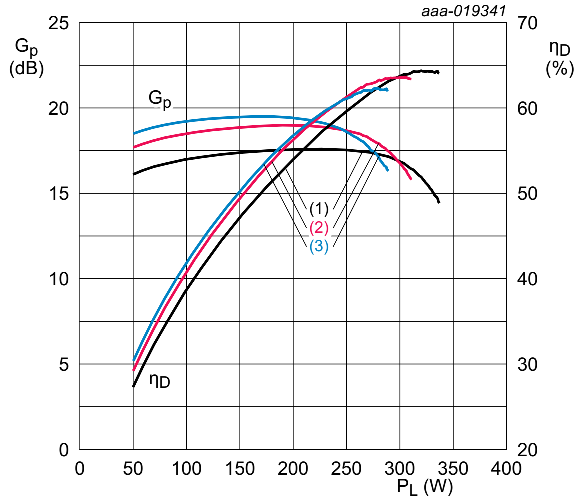
Fig 2. Component layout for production test circuit

Table 9. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C2, C3, C4, C5, C6	multilayer ceramic chip capacitor	15 pF	ATC100A150FW150XC
C7, C8, C9, C10	multilayer ceramic chip capacitor	1 μF	Murata
C11, C12	electrolytic capacitor	10 μF	
R1, R2	resistor	2.1 Ω	SMD 0805

7.4 Graphical data



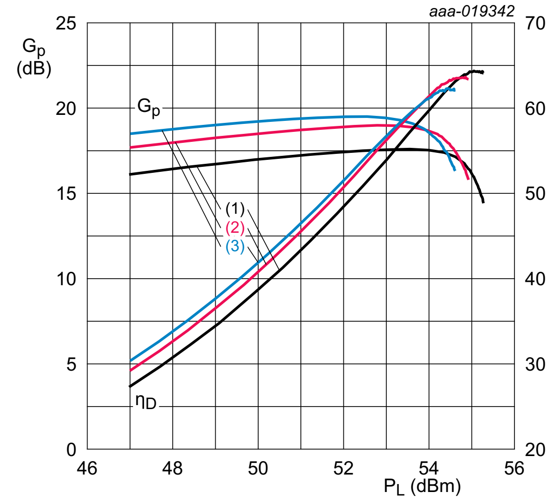
V_{DS} = 32 V; I_{Dq} = 20 mA.

(1) f = 2400 MHz

(2) f = 2450 MHz

(3) f = 2500 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



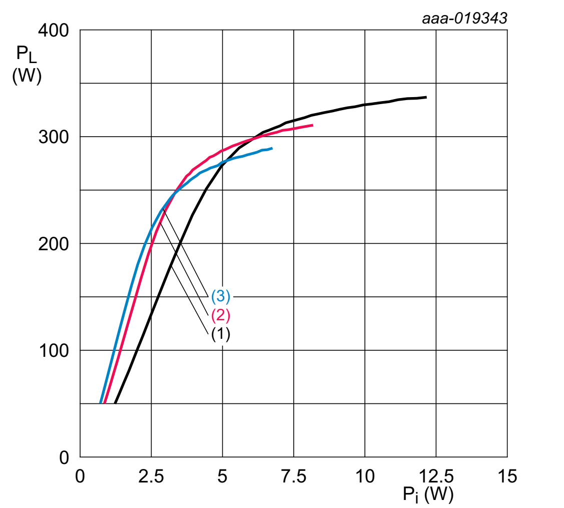
V_{DS} = 32 V; I_{Dq} = 20 mA.

(1) f = 2400 MHz

(2) f = 2450 MHz

(3) f = 2500 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values



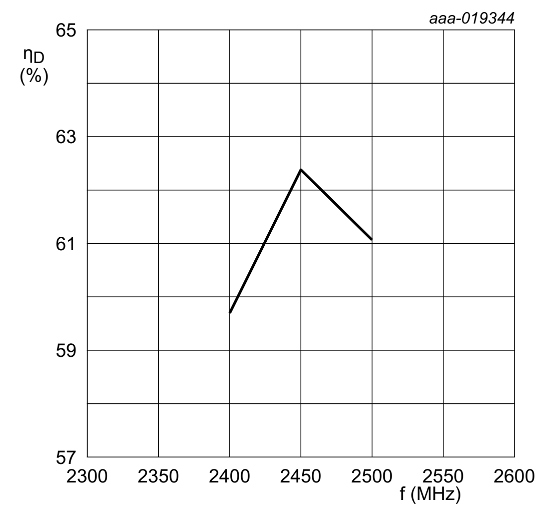
V_{DS} = 32 V; I_{Dq} = 20 mA.

(1) f = 2400 MHz

(2) f = 2450 MHz

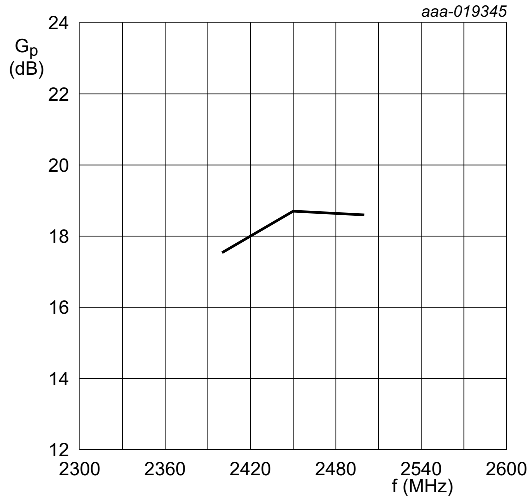
(3) f = 2500 MHz

Fig 5. Output power as a function of input power; typical values



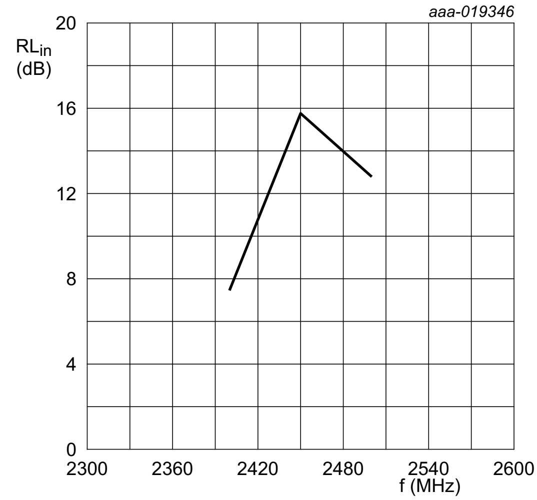
V_{DS} = 32 V; I_{Dq} = 20 mA; P_L = 250 W.

Fig 6. Drain efficiency as a function of frequency; typical values



V_{DS} = 32 V; I_{Dq} = 20 mA; P_L = 250 W.

Fig 7. Power gain as a function of frequency; typical values

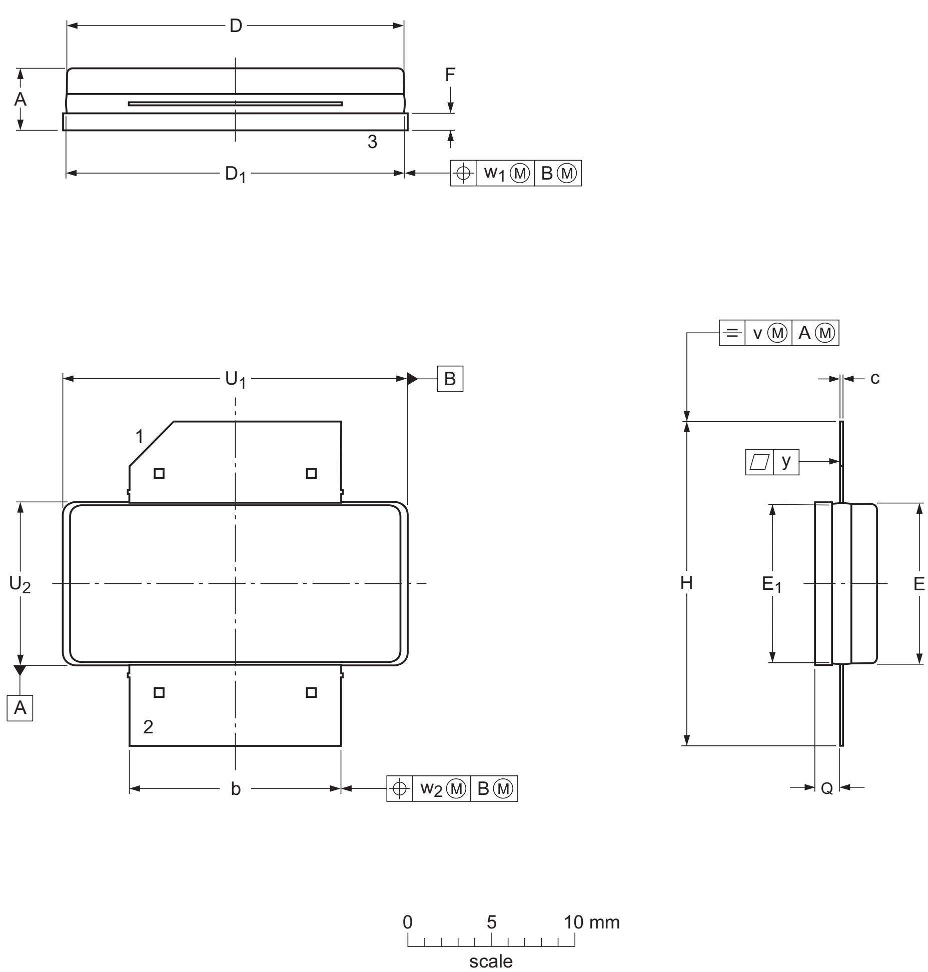


V_{DS} = 32 V; I_{Dq} = 20 mA; P_L = 250 W.

Fig 8. Input return loss as a function of frequency; typical values

8. Package outline

Air cavity plastic earless flanged package; 2 leads **SOT1270-1**



Dimensions

Unit		A	b	c	D	D_1	E	E_1	F	H	Q(1)	U_1	U_2	v	w_1	w_2	y
mm	max	4.01	12.80	0.18	20.42	20.37	9.80	9.75	1.14	19.53	1.68	20.70	9.91	0.50	0.50	0.50	0.10
	nom																
	min	3.40	12.60	0.13	20.12	20.17	9.50	9.55	0.94	19.33	1.45	20.50	9.70				

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1270-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1270-1						~~16-09-28~~ 16-11-15

Fig 9. Package outline SOT1270-1

9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C1 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1C [2]

[1] CDM classification C1 is granted to any part that passes after exposure to an ESD pulse of 250 V, but fails after exposure to an ESD pulse of 500 V.

[2] HBM classification 1C is granted to any part that passes after exposure to an ESD pulse of 1000 V, but fails after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC2425M9LS250 v.3	20161220	Product data sheet	-	BLC2425M9LS250 v.2
Modifications:	• Figure 9 on page 7: updated package outline drawing SOT1270-1 • Section 9 on page 8: updated Handling information			
BLC2425M9LS250 v.2	20161021	Product data sheet	-	BLC2425M9LS250 v.1
BLC2425M9LS250 v.1	20160928	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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