

## N-Channel Enhancement Mode Power MOSFET

### Description

The RM12N100LD uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### General Features

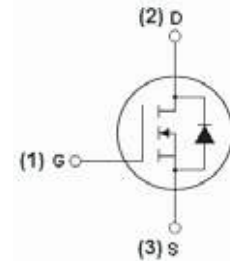
- $V_{DS} = 100V, I_D = 12A$   
 $R_{DS(ON)} < 112m\Omega @ V_{GS}=10V$   
 $R_{DS(ON)} < 120m\Omega @ V_{GS}=4.5V$
- Special process technology for high ESD capability
- High density cell design for ultra low  $R_{Dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Halogen-free
- P/N suffix V means AEC-Q101 qualified, e.g:RM12N100LDV

### Application

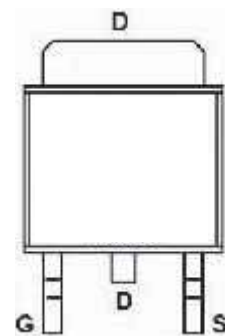
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

**100% UIS TESTED!**

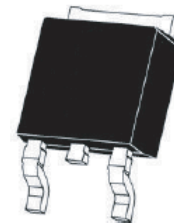
**100%  $\Delta V_{ds}$  TESTED!**



Schematic diagram



Marking and pin assignment



TO-252-2Ltop view

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
12N100	RM12N100LD	TO-252-2L	-	-	-

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current-Continuous	12	A
$I_D (100^\circ C)$	Drain Current-Continuous( $T_C=100^\circ C$ )	7.7	A
$I_{DM}$	Pulsed Drain Current	24	A
$P_D$	Maximum Power Dissipation	34.7	W
$E_{AS}$	Single pulse avalanche energy <sup>(Note 5)</sup>	256	mJ
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 To 150	$^\circ C$

## Thermal Characteristic

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	3.6	$^{\circ}C/W$
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## Electrical Characteristics ( $T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=80V, V_{GS}=0V$	-	-	1	$\mu A$
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	-	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=10A$	-	-	112	m $\Omega$
		$V_{GS}=4.5V, I_D=10A$	-	-	120	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=5V, I_D=10A$	-	13	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
$C_{iss}$	Input Capacitance	$V_{DS}=15V, V_{GS}=0V,$ $F=1.0MHz$	-	1535	-	PF
$C_{oss}$	Output Capacitance		-	60	-	PF
$C_{rSS}$	Reverse Transfer Capacitance		-	37	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=50V, R_L=5\Omega$ $V_{GS}=10V, R_{GEN}=3.3\Omega$	-	4.2	-	nS
$t_r$	Turn-on Rise Time		-	8.2	-	nS
$t_{d(off)}$	Turn-Off Delay Time		-	35.6	-	nS
$t_f$	Turn-Off Fall Time		-	9.6	-	nS
$Q_g$	Total Gate Charge	$V_{DS}=80V, I_D=10A,$ $V_{GS}=10V$	-	26.2	-	nC
$Q_{gs}$	Gate-Source Charge		-	4.6	-	nC
$Q_{gd}$	Gate-Drain Charge		-	5.1	-	nC
<b>Drain-Source Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage <sup>(Note 3)</sup>	$V_{GS}=0V, I_S=10A$	-	-	1.2	V
$I_S$	Diode Forward Current <sup>(Note 2)</sup>	-	-	-	12	A
$t_{rr}$	Reverse Recovery Time	$T_J=25^{\circ}C, I_F=10A$	-	37	-	nS
$Q_{rr}$	Reverse Recovery Charge	$di/dt=100A/\mu s$ <sup>(Note 3)</sup>	-	27.3	-	nC
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

### Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS Condition :  $T_J=25^{\circ}C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega, I_{AS}=32A$

## RATING AND CHARACTERISTICS CURVES (RM12N100LD)

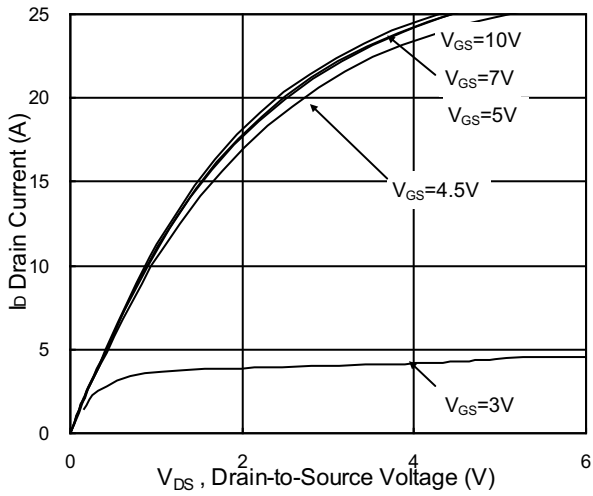


Fig.1 Typical Output Characteristics

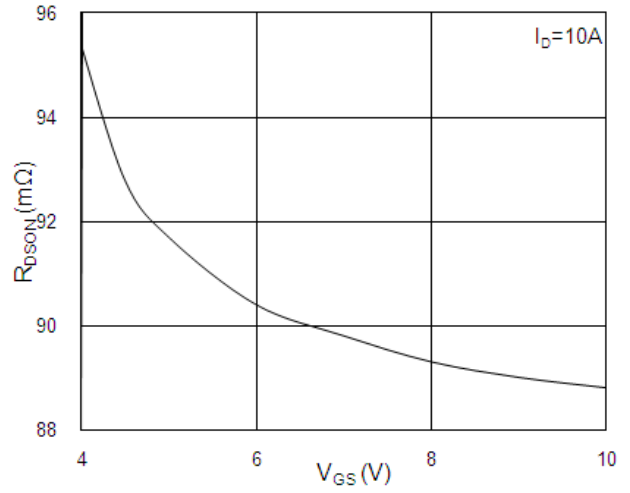


Fig.2 On-Resistance vs. Gate-Source

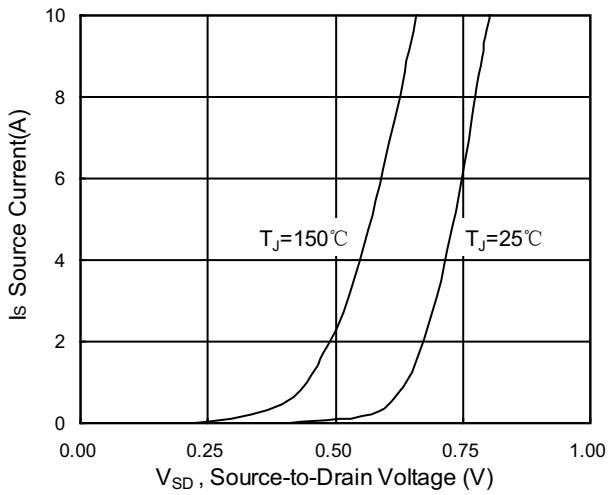


Fig.3 Forward Characteristics Of Reverse

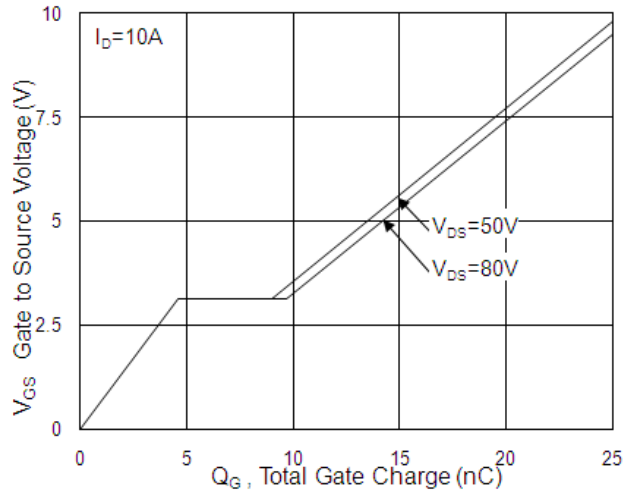


Fig.4 Gate-Charge Characteristics

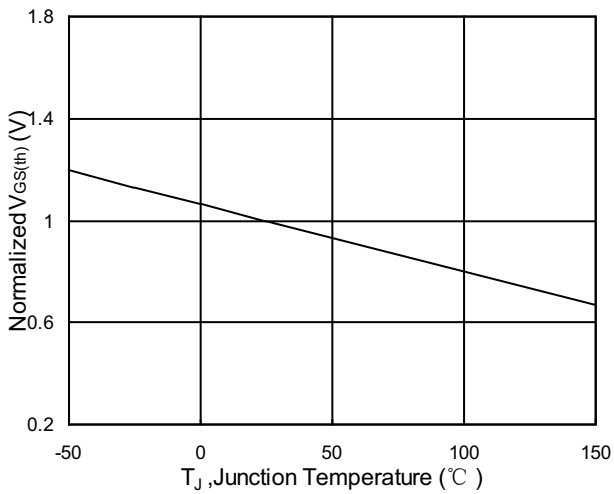


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$

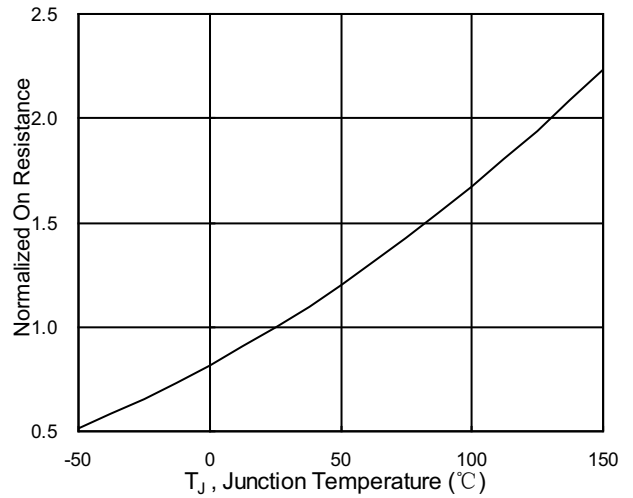


Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$

# RATING AND CHARACTERISTICS CURVES (RM12N100LD)

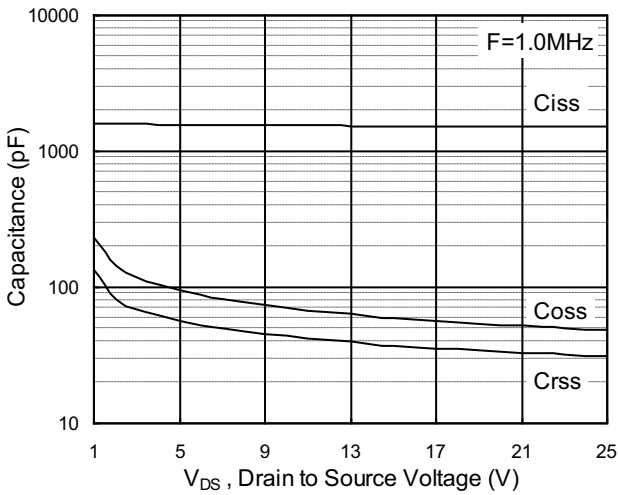


Fig.7 Capacitance

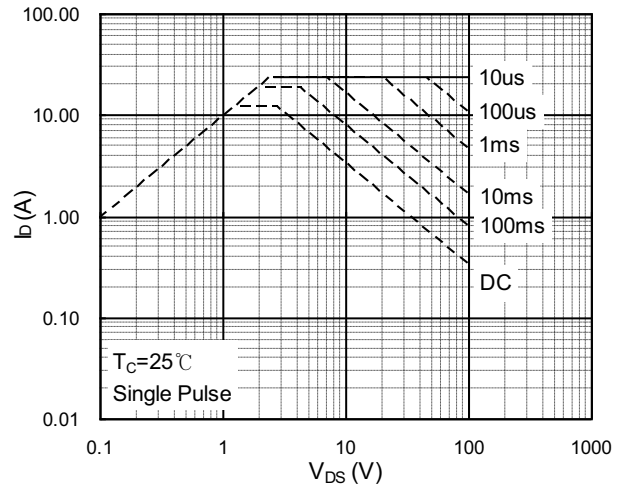


Fig.8 Safe Operating Area

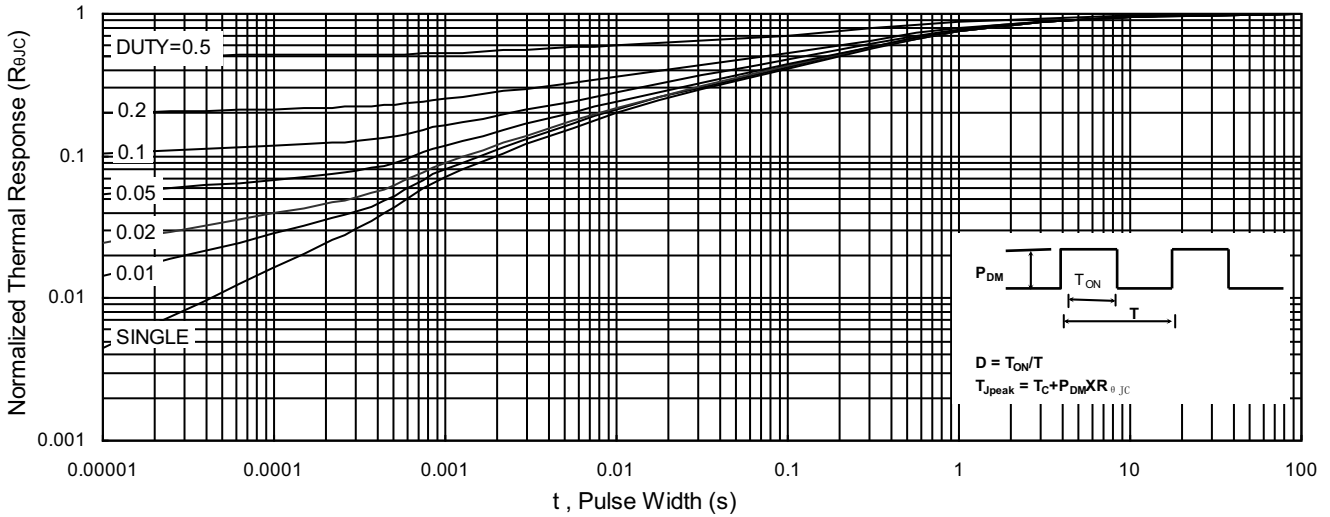


Fig.9 Normalized Maximum Transient Thermal Impedance

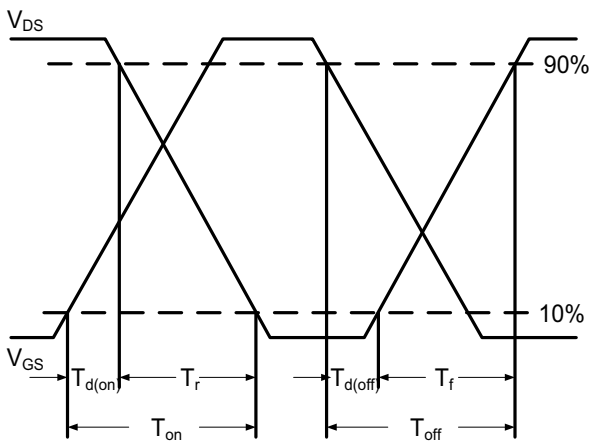


Fig.10 Switching Time Waveform

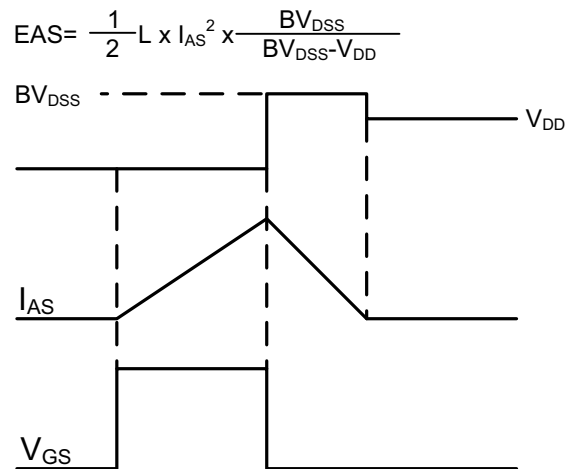
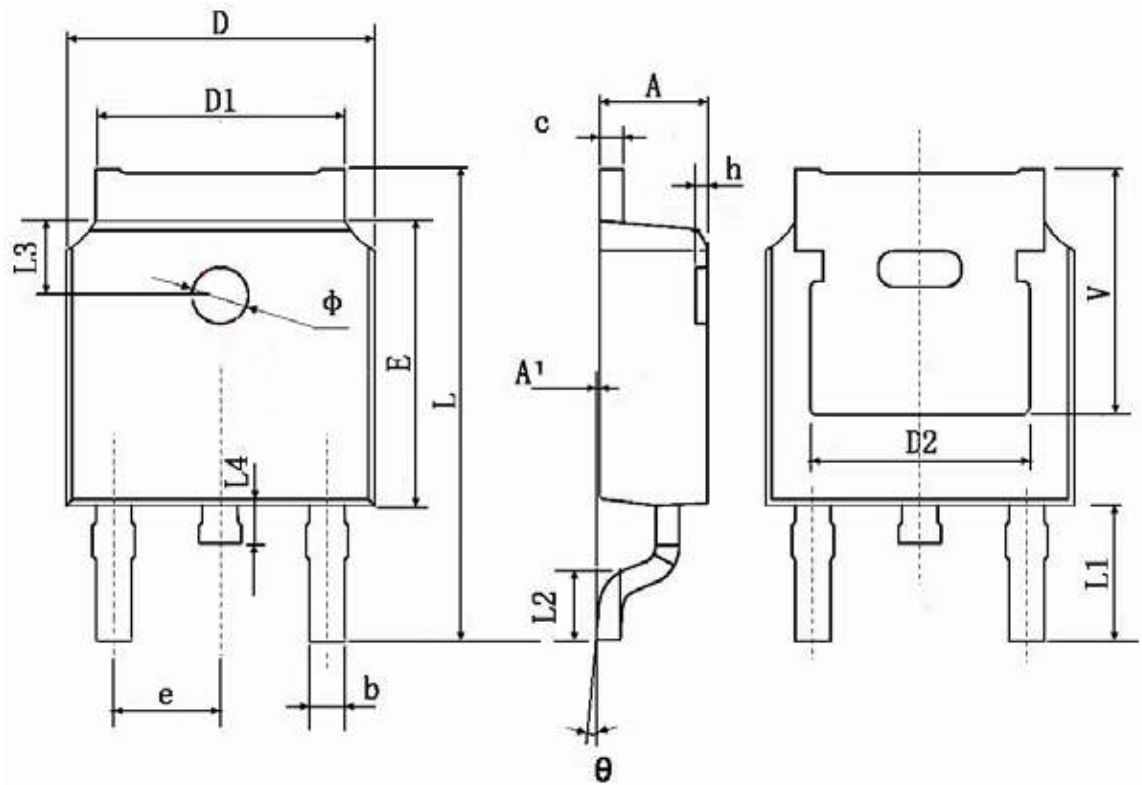


Fig.11 Unclamped Inductive Switching Waveform

## TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
$\Phi$	1.100	1.300	0.043	0.051
$\theta$	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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