



STD7NK30Z, STF7NK30Z STP7NK30Z

N-channel, 300 V, 0.80 Ω , 5 A TO-220, TO-220FP, DPAK
Zener-protected SuperMESH™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on) max}	I _D	P _w
STF7NK30Z	300 V	< 0.9 Ω	5 A	20 W
STP7NK30Z	300 V	< 0.9 Ω	5 A	50 W
STD7NK30Z	300 V	< 0.9 Ω	5 A	50 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability

Applications

- Switching application

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage Power MOSFETs including revolutionary MDmesh™ products

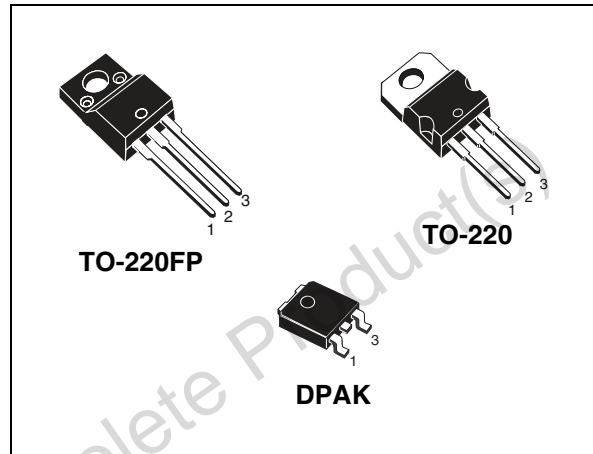


Figure 1. Internal schematic diagram

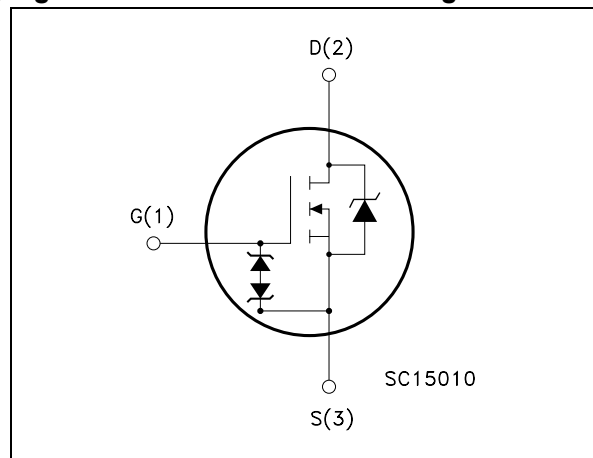


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD7NK30Z	D7NK30Z	DPAK	Tape and reel
STF7NK30Z	F7NK30Z	TO-220FP	Tube
STP7NK30Z	P7NK30Z	TO-220	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, DPAK	TO-220FP	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	300		V
V_{GS}	Gate- source voltage	± 30		V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	5	5 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3.2	3.2 ⁽¹⁾	A
I_{DM} ⁽²⁾	Drain current (pulsed)	20	20 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	50	20	W
	Derating factor	0.4	0.16	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100 pF, R=1.5 k Ω)	2800		V
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; $T_C=25\text{ }^\circ\text{C}$)		2500	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150		V

- Limited only by maximum temperature allowed
- Pulse width limited by safe operating area
- $I_{SD} \leq 5.7\text{ A}$, di/dt $\leq 200\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, DPAK	TO-220FP	
Rthj-case	Thermal resistance junction-case Max	2.50	6.25	V
Rthj-amb	Thermal resistance junction-ambient Max	62.5		V
T_l	Maximum lead temperature for soldering purpose	300		A

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	5	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	130	mJ

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	300			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = max rating V _{DS} = max rating @ 125 °C			1 50	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 50 μA	3	3.75	4.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 2.5 A		0.80	0.90	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 15 V, I _D = 2.5 A		2.5		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25 V, f = 1MHz, V _{GS} = 0		380 74 15		pF pF pF
C _{oss eq.} ⁽²⁾	Equivalent output capacitance	V _{GS} = 0, V _{DS} = 0 to 240 V		30		pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 240 V, I _D = 7 A, V _{GS} = 10 V <i>Figure 16</i>		13 4.5 7.6	17	nC nC nC

1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5%.

2. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 150\text{ V}$, $I_D = 3.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ <i>Figure 15</i>		11		ns
t_r	Rise time			25		ns
$t_{d(off)}$	Turn-off-delay time			20		ns
t_f	Fall time			10		ns
$t_{r(Voff)}$	Off-voltage rise time	$V_{DD} = 240\text{ V}$, $I_D = 7\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ <i>Figure 15</i>		8.5		ns
t_f	Fall time			8.5		ns
t_c	Cross-over time			20		ns

Table 8. Source Drain Diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
I_{SD}	Source-drain current				5	A	
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				20	A	
$V_{SD}^{(2)}$	Forward On voltage	$I_{SD} = 5\text{ A}$, $V_{GS} = 0$			1.6	V	
t_{rr}	Reverse recovery time	$I_{SD} = 7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 40\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ <i>Figure 20</i>		154		ns	
Q_{rr}	Reverse recovery charge				716		nC
I_{RRM}	Reverse recovery current				9.3		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

Table 9. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

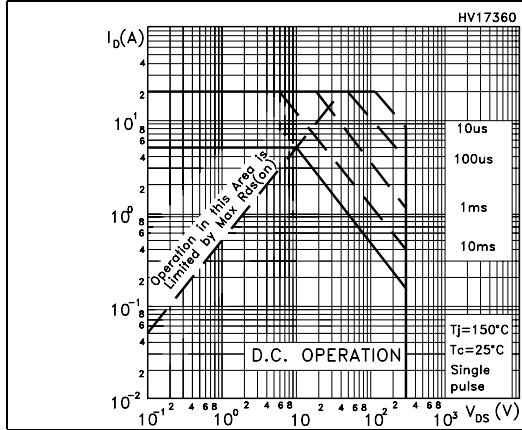


Figure 3. Thermal impedance for TO-220

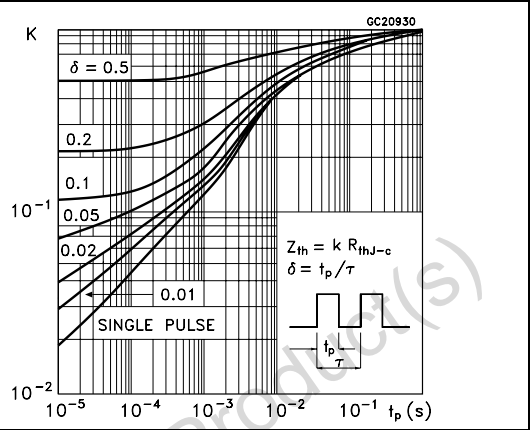


Figure 4. Safe operating area for TO-220FP

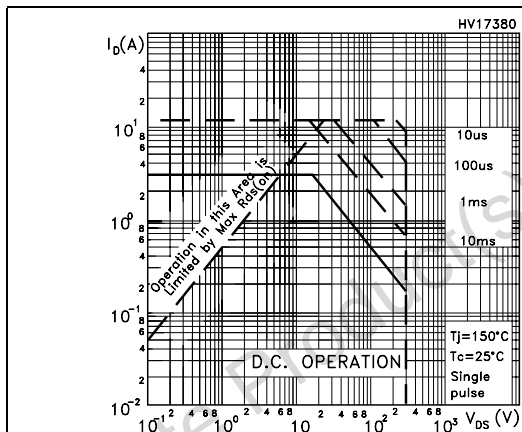


Figure 5. Thermal impedance for TO-220FP

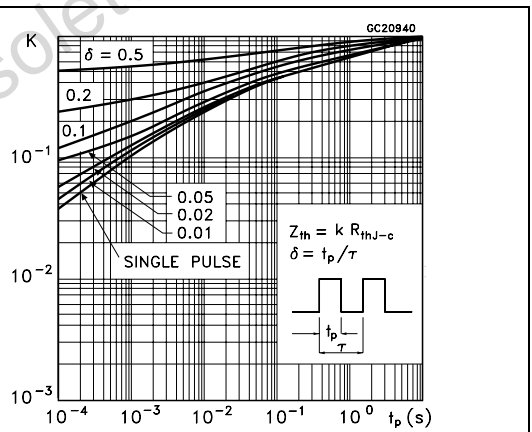


Figure 6. Output characteristics

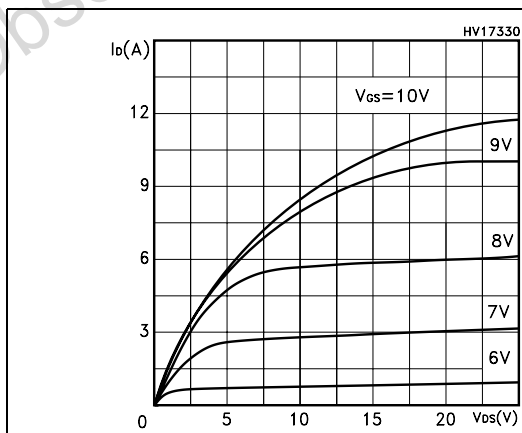


Figure 7. Transfer characteristics

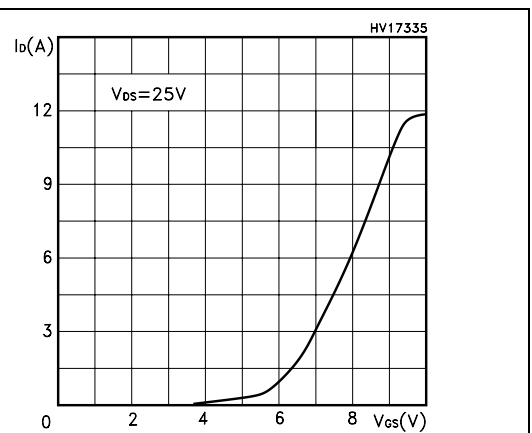


Figure 8. Static drain source on resistance

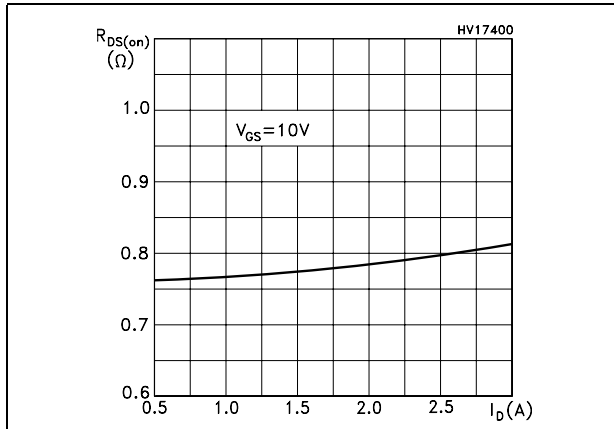


Figure 9. Normalized BV_{DSS} vs temperature

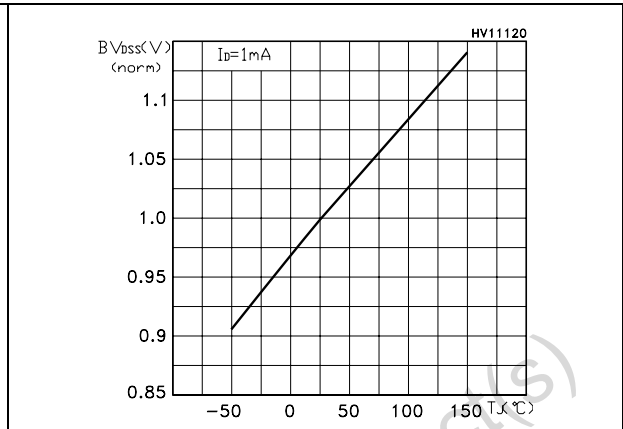


Figure 10. Gate charge vs gate-source voltage

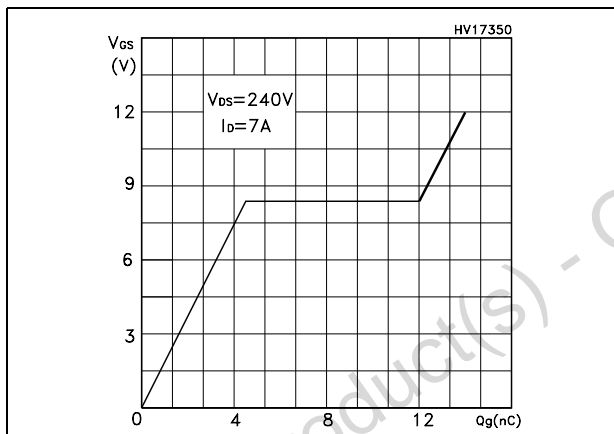


Figure 11. Capacitance variations

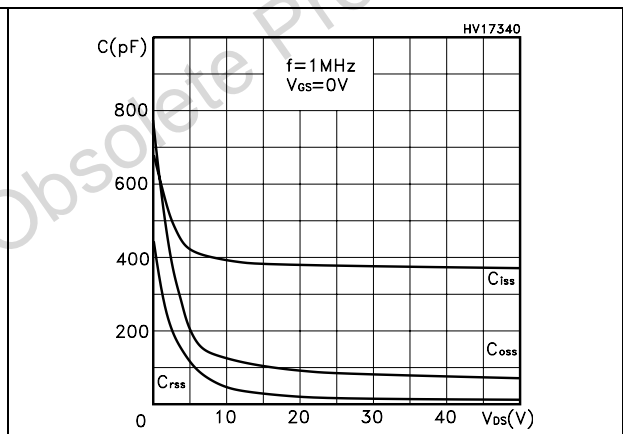


Figure 12. Normalized gate threshold voltage vs temperature

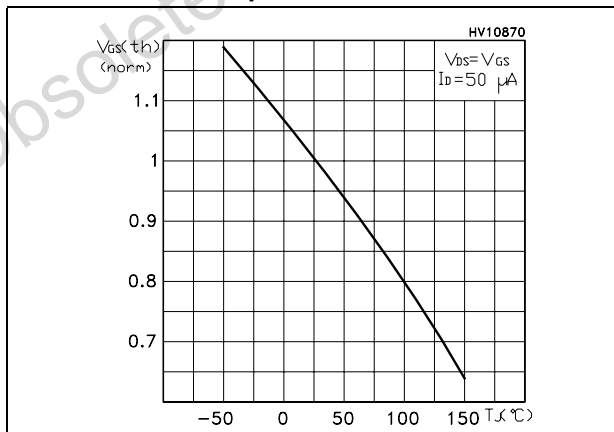


Figure 13. Normalized on resistance vs temperature

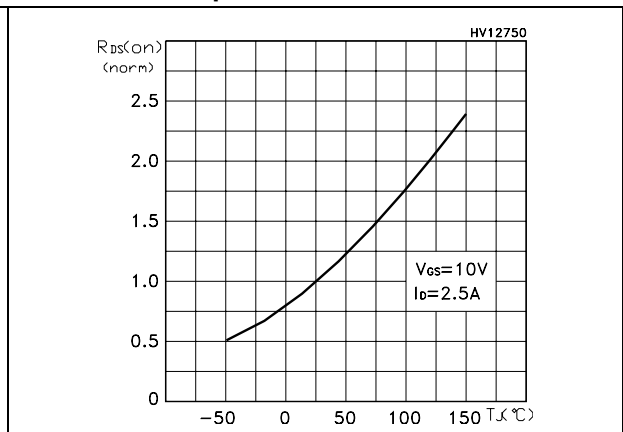
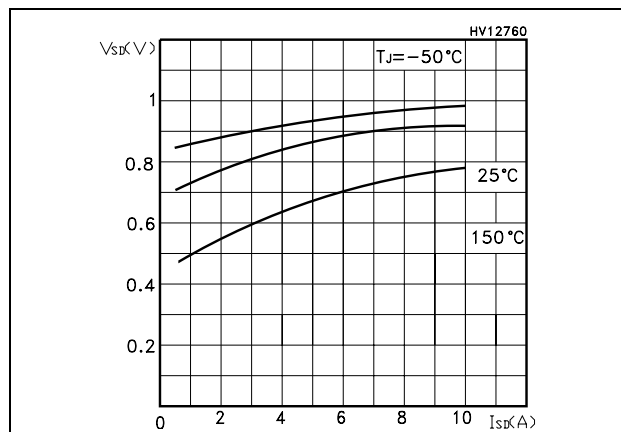


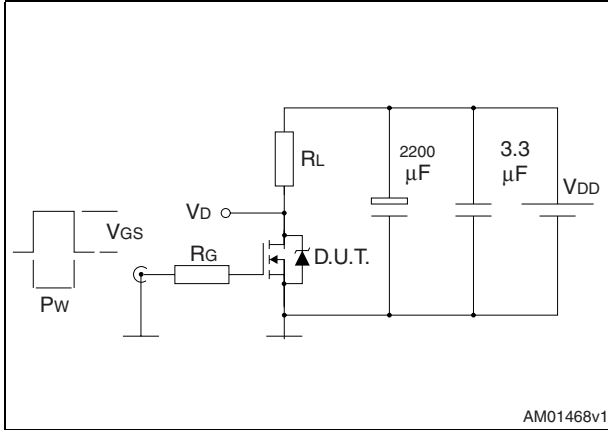
Figure 14. Source-drain diode forward characteristics



Obsolete Product(s) - Obsolete Product(s)

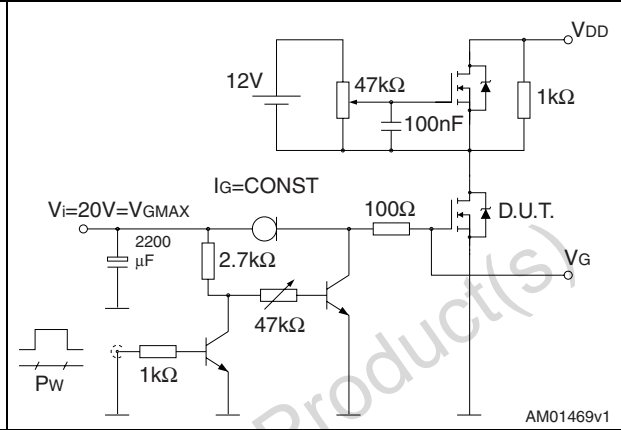
3 Test circuits

Figure 15. Switching times test circuit for resistive load



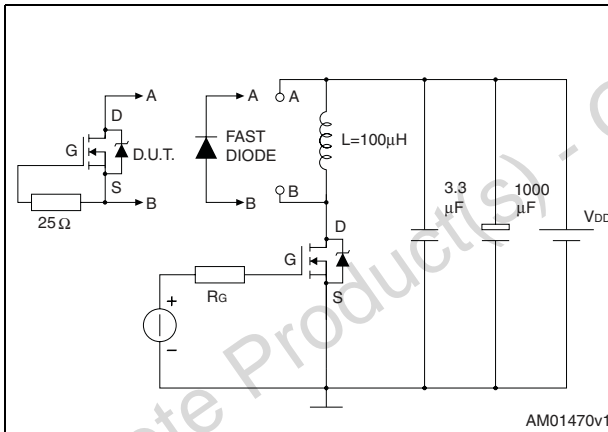
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Figure 16. Gate charge test circuit



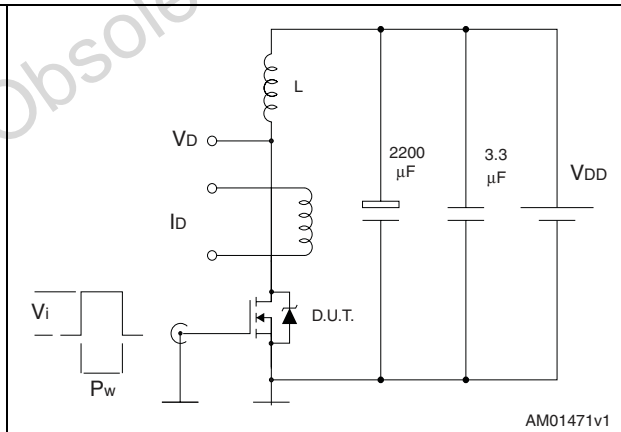
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Figure 17. Test circuit for inductive load switching and diode recovery times



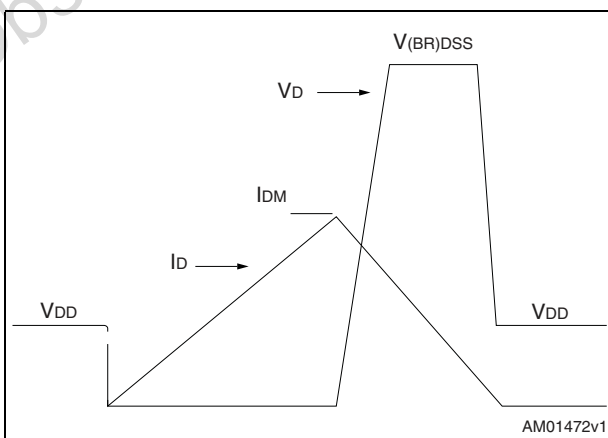
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Figure 18. Unclamped inductive load test circuit



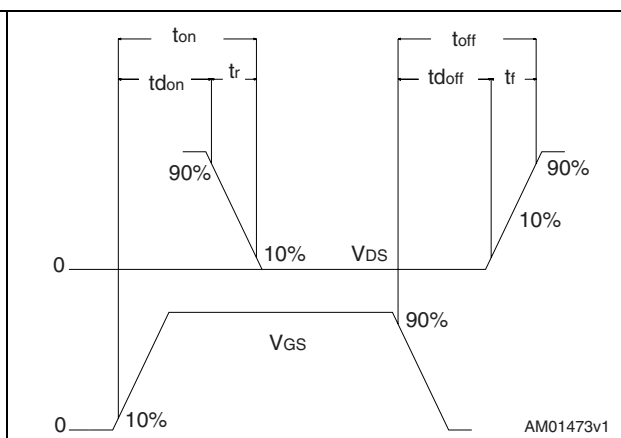
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Figure 19. Unclamped inductive waveform



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Figure 20. Switching time waveform



AM01473v1

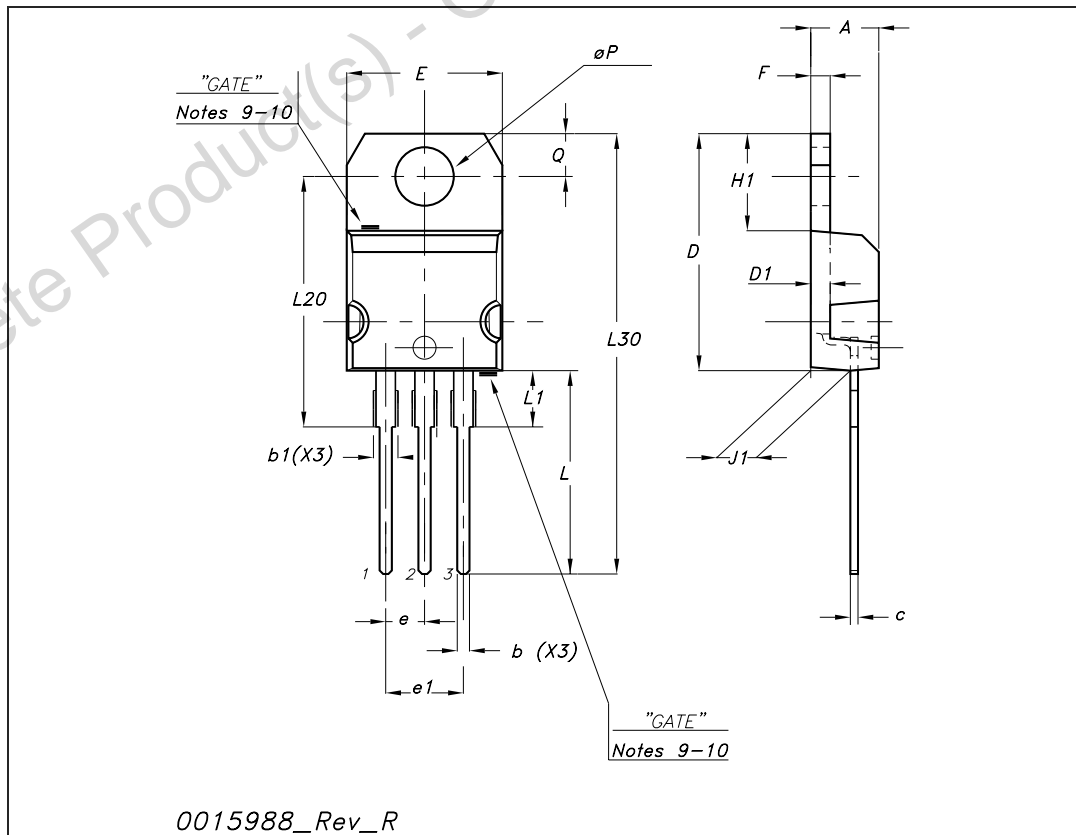
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Obsolete Product(s) - Obsolete Product(s)

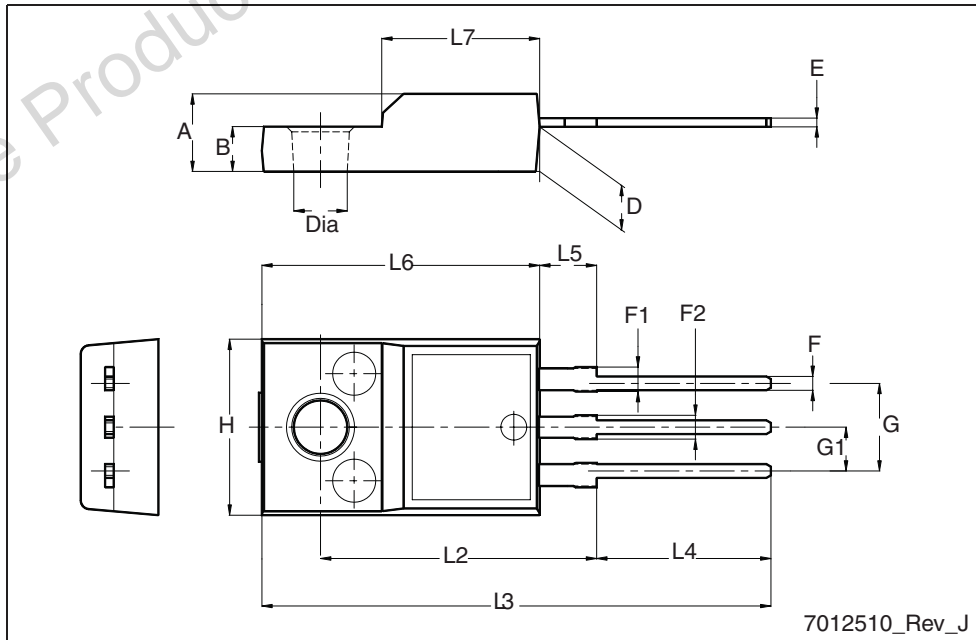
TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



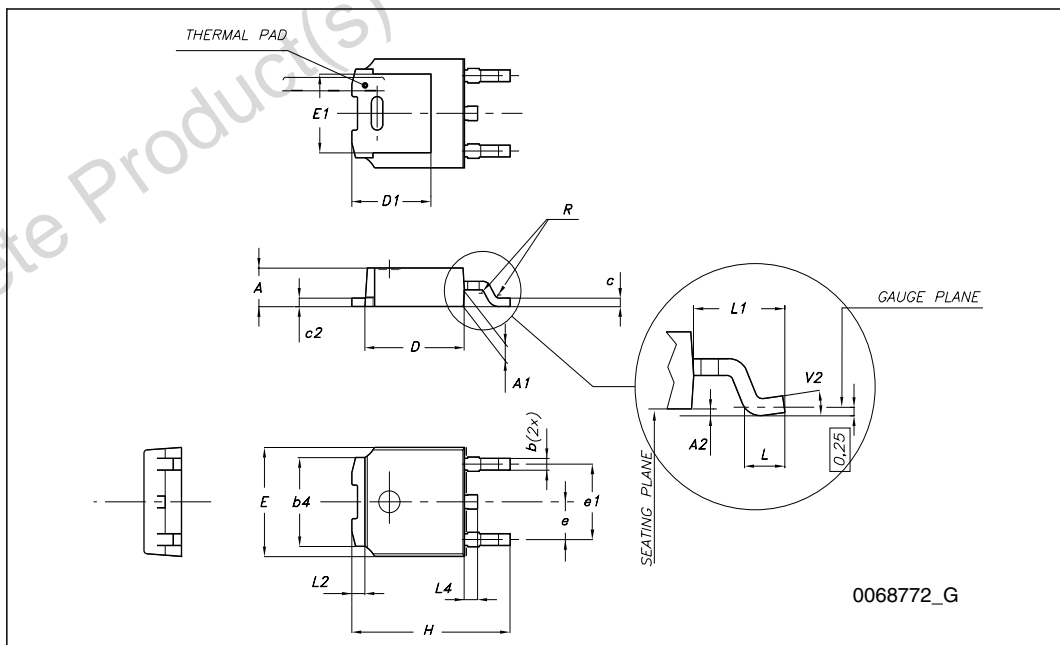
TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.5
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2



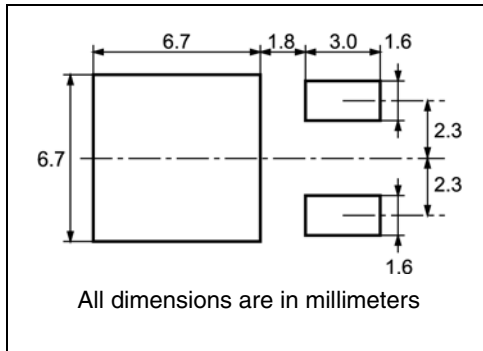
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°



5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

TOP COVER TAPE

10 pitches cumulative tolerance on tape +/- 0.2 mm

User Direction of Feed

Center line of cavity

For machine ref. only including draft and radii concentric around B0

TRL

FEED DIRECTION

Bending radius R min.

6 Revision history

Table 10. Revision history

Date	Revision	Changes
10-May-2005	1	New stylesheet
05-Sep-2005	2	Inserted Ecopack indication
04-Jan-2006	3	Some values changed on table 8.
22-Mar-2006	4	Inserted DPAK
05-Mar-2009	5	Section 4: Package mechanical data has been updated

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