

CD4030C Quad EXCLUSIVE-OR Gate

General Description

The CD4030C EXCLUSIVE-OR gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS} .

Features

- Wide supply voltage range: 3.0V to 15V
- Low power: 100 nW (typ.)
- Medium speed operation:
 $t_{PHL} = t_{PLH} = 40$ ns (typ.) at $C_L = 15$ pF, 10V supply
- High noise immunity 0.45 V_{CC} (typ.)

Applications

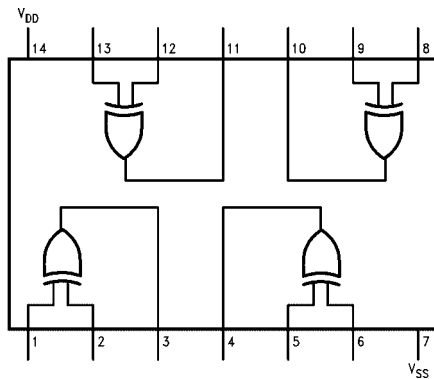
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- Remote metering
- Computers

Ordering Code:

Order Number	Package Number	Package Description
CD4030CSJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4030CN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram

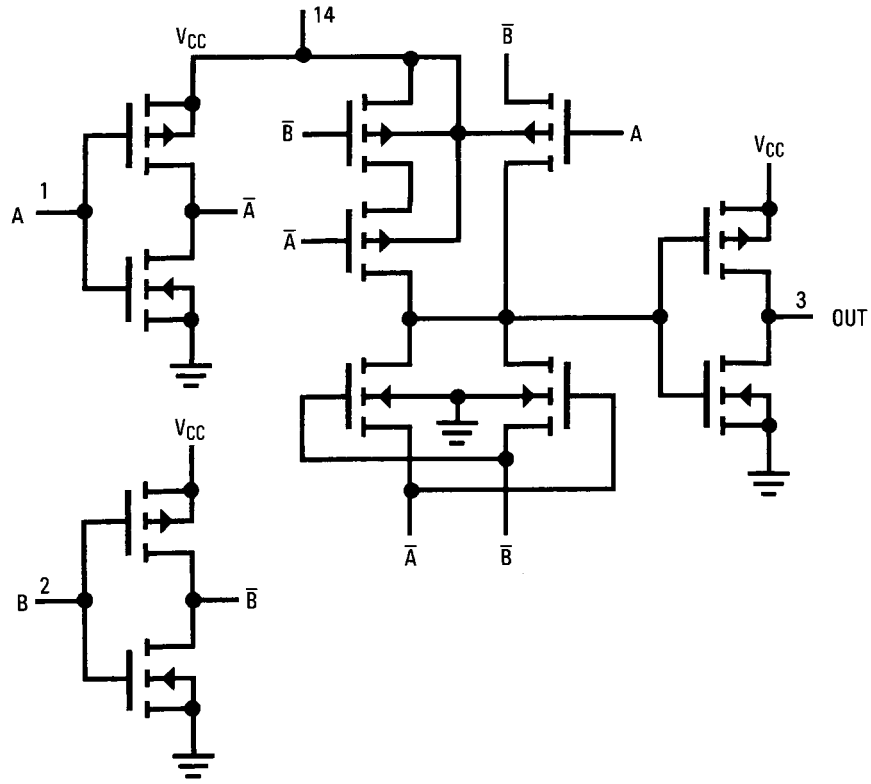


Truth Table

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

1 = HIGH Level
0 = LOW Level

Logic Diagram



Absolute Maximum Ratings(Note 1)

Voltage at Any Pin (Note 2)	$V_{SS} - 0.3V$ to $V_{SS} + 15.5V$
Operating Temperature Range	$-55^{\circ}C$ to $+125^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{DD} Range	$V_{SS} + 3.0V$ to $V_{SS} + 15V$
Lead Temperature (Soldering, 10 seconds)	260 $^{\circ}C$

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics tables provide conditions for actual device operation.

Note 2: This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

DC Electrical Characteristics

Symbol	Parameter	Conditions	$-55^{\circ}C$			$+25^{\circ}C$			$+125^{\circ}C$			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_L	Quiescent Device Current	$V_{DD} = 5.0V$			0.5		0.005	0.5			30	μA
		$V_{DD} = 10V$			1.0		0.01	1.0			60	
P_D	Quiescent Device Dissipation Package	$V_{DD} = 5.0V$			2.5		0.025	2.5			150	μW
		$V_{DD} = 10V$			10		0.1	10			600	
V_{OL}	Output Voltage LOW Level	$V_{DD} = 5.0V$			0.05		0	0.05			0.05	V
		$V_{DD} = 10V$			0.05		0	0.05			0.05	
V_{OH}	Output Voltage HIGH Level	$V_{DD} = 5.0V$	4.95			4.95	5.0		4.95			V
		$V_{DD} = 10V$	9.95			9.95	10		9.95			
V_{NL}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$	1.5			1.5	2.25		1.4			V
		$V_{DD} = 10V$	3.0			3.0	4.5		2.9			
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$	1.4			1.5	2.25		1.5			V
		$V_{DD} = 10V$	2.9			3.0	4.5		3.0			
I_{DN}	Output Drive Current N-Channel (Note 3)	$V_{DD} = 5.0V$	0.75			0.6	1.2		0.45			mA
		$V_{DD} = 10V$	1.5			1.2	2.4		0.9			
I_{DP}	Output Drive Current P-Channel (Note 3)	$V_{DD} = 5.0V$	-0.45			-0.3	-0.6		-0.21			mA
		$V_{DD} = 10V$	-0.95			-0.65	-1.3		-0.45			
I_I	Input Current	$V_I = 0V$ or $V_I = V_{DD}$					10					pA

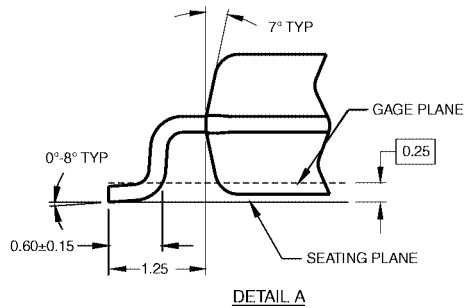
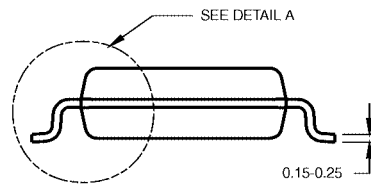
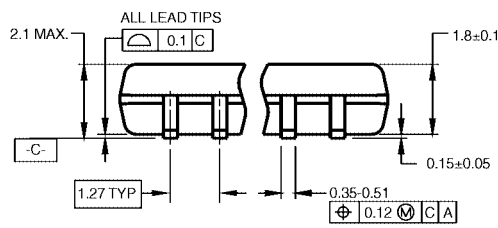
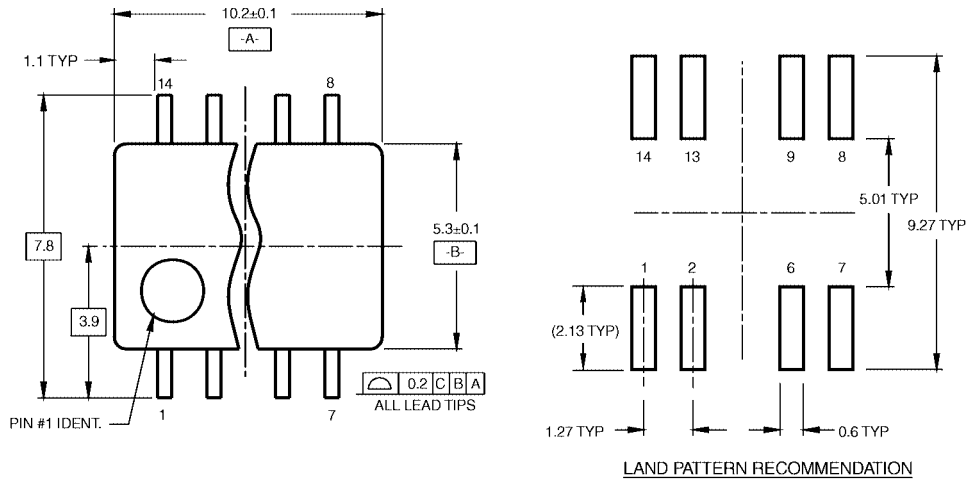
Note 3: I_{DN} and I_{DP} are tested one output at a time.

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
t_{PHL}	Propagation Delay Time	$V_{DD} = 5.0V$		100	300	ns
		$V_{DD} = 10V$		40	150	
t_{PLH}	Propagation Delay Time	$V_{DD} = 5.0V$		100	300	ns
		$V_{DD} = 10V$		40	150	
t_{THL}	Transition Time HIGH-to-LOW Level	$V_{DD} = 5.0V$		70	300	ns
		$V_{DD} = 10V$		25	150	
t_{TLH}	Transition Time LOW-to-HIGH Level	$V_{DD} = 5.0V$		80	300	ns
		$V_{DD} = 10V$		30	150	
C_I	Input Capacitance	$V_I = 0V$ or $V_I = V_{DD}$		5.0		pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

Physical Dimensions inches (millimeters) unless otherwise noted

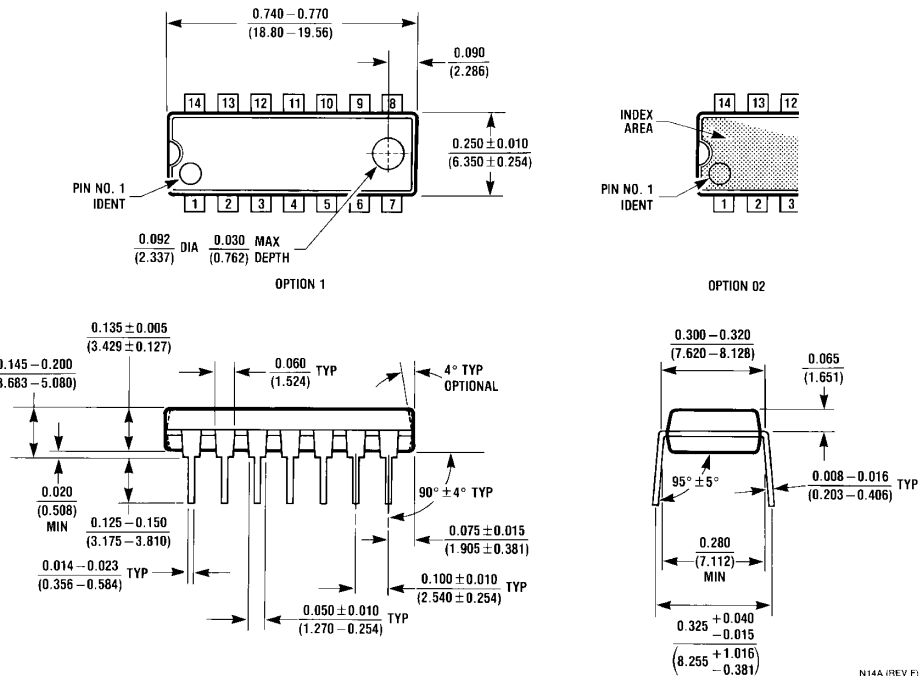


- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

N14A (REV F)

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