User's Guide
SLLU281A–November 2017–Revised March 2019

# TCAN4550 evaluation module

This user's guide describes the TCAN4550 evaluation module (EVM). This EVM helps designers evaluate device performance, support fast development, and analyze Controller Area Network with Flexible Data rate (CAN FD) systems using TCAN4550 CAN FD physical layer transceiver devices.

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## Trademarks

# 1 Introduction

This user's guide describes the TCAN4550 EVM. This EVM helps designers evaluate device performance, support fast development, and analyze CAN FD systems using TCAN4550 CAN FD physical layer transceiver devices.

## 1.1 Features

The features of the TCAN4550 EVM follow:

- CAN FD controller with integrated CAN transceiver
- Operates from a battery voltage input $V_{BAT}$ (6 V to 24 V)
- Polarity protected and EMC filtered supply voltage
- Dual-channel LDO
  - Selectable $V_{IO}$ (5-V, or 3.3-V) supply rails
  - General-purpose 5-V supply rail
  - Error monitoring and current-sense features
- CAN bus header and industry-standard DB-9 connector
- TVS diode pad (not populated)
- CAN bus transient signal injection/monitoring header
- CAN bus termination with disconnect headers
- Common-mode choke (bypassed with 0-Ω resistors by default)
- Status LEDs
- MCU interface header (SPI, GPIO, $V_{IO}$, and 5-V)
- Reset push-button switch
- Configuration DIP switches for support of multiple use pins
- Crystal oscillator (40 MHz)
- External clock input and output SMA connectors
- High-voltage Inhibit and Wake signal header
- WAKE push-button switch

## 1.2 Description

The TCAN4550 EVM provides the user with the ability to evaluate the TI TCAN4550 CAN FD Controller with integrated CAN transceiver devices. Any MCU or SPI controller with an I/O voltage of 3.3 V or 5 V may be connected to the EVM through a standard interface header. The EVM features a polarity-protected and EMC-filtered supply voltage that allows the EVM to operate from an external voltage from 6 V to 24 V. A dual-channel LDO creates a 5-V, general-purpose voltage rail to source the LEDs and supporting ICs, and a variable $V_{IO}$ voltage rail that can be set to 5 V or 3.3 V to match the MCU signal level requirements. The $V_{IO}$ or 5-V rail is also designed to source the supply voltage for the connected MCU to evaluate sleep mode and wake-up events.

# 2 EVM Features and Requirements

## 2.1 Power

### 2.1.1 EVM Supply Voltage

The TCAN4550 family of devices can operate across a wide recommended supply voltage range of 6 V to 24 V, with an absolute maximum voltage of 40 V. This makes the TCAN4550 device ideal for many different applications, including those in the automotive market. Typically, a wide array of tests must be performed throughout the qualification process specified in various standards, including reverse-polarity and EMC performance requirements. To accommodate these types of tests, a reverse-blocking diode and an EMC-filtering circuit have been added to the EVM based on a typical automotive ECU design to clean and protect the device voltage input supply $V_{SUP}$ from the external, unprotected battery voltage $V_{BAT\_EXT}$. The EVM uses a 30-V Zener diode as protection from excessive supply voltages.

Furthermore, it is common for a CAN node to receive power and CAN signals through a single wiring harness. The supply voltage of the EVM can be applied through pin 9 of the DB-9 connector consistent with the industry-standard pinout, or through header J9. Due to the reverse polarity blocking Schottky diode, a small voltage difference exists between the supplied voltage $V_{BAT}$ and the voltage at the TCAN4550 VSUP pin. This small voltage difference can be monitored on header J8. For lab environment tests that do not require the polarity protection, the power supply voltage can be applied directly to J8. Figure 1 shows the EVM supply voltage connectors.

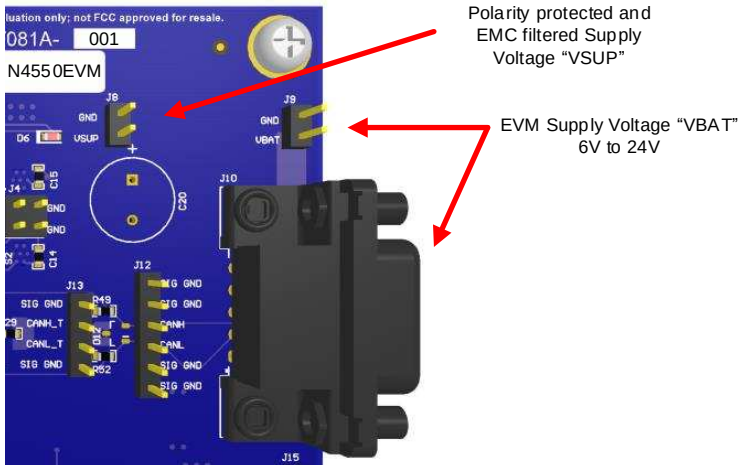


**Figure 1. EVM Supply Voltage Connectors**

### 2.1.2 TCAN4550

#### 2.1.2.1 VSUP Pin

The TCAN4550 is powered through the VSUP pin and supplies the internal regulators for the digital core, CAN transceiver, and optional VCCOUT. A 330-nF capacitor is required on the LDO Filter pin FLTR for proper operation as described in the data sheet and seen in the schematics.

#### 2.1.2.2 VIO Pin

The VIO pin provides the digital I/O voltage to match the MCU I/O voltage to prevent the need for level-shifting of signals across different MCUs. The VIO pin supports the SPI I/O pins, GPIO1 and GPO2 pins, as well as the oscillator block supporting the crystal oscillator or CLKIN pins.

#### 2.1.2.3 VCCOUT Pin

The TCAN4550 devices provide up to 70 mA of current on the VCCOUT pin from the 5-V internal LDO without impacting the CAN transceiver performance, except when in sleep mode and when the regulator is disabled. This voltage can be used to power an MCU or other supporting circuitry that is not needed during sleep mode. At least 10 µF of capacitance to ground is required on the VCCOUT pin, as described in the data sheet and seen in the schematic.

#### 2.1.2.4 GND Pin

The thermal pad and pin 13 of the TCAN4550 devices are ground and are connected to the ground plane of the EVM to support heat dissipation.

### 2.1.3 External LDO (TPS7B7702-Q1)

Although it is not required for all applications, the EVM included:

- a dual-channel LDO to provide the $V_{IO}$ voltage reference for TCAN4550
- a 5-V utility voltage to source the LEDs
- other devices on the EVM that have been added to enhance the evaluation of the TCAN4550 features.

The 5-V channel is configured to become enabled when the $V_{SUP}$ voltage is present, and the VIO channel is configured to become enabled through the TCAN4550 INH pin.

When the $V_{SUP}$ voltage is applied to the TCAN4550, the device enters standby mode and drives the INH pin to a high level ($V_{SUP}$ minus a diode drop) and monitors the VIO pin for a proper input voltage. If the $V_{IO}$ voltage fails to rise above the $UV_{IO}$ undervoltage threshold, or ever drops below this threshold during normal operation, for longer than the $t_{uv}$ undervoltage time, the TCAN4550 enters sleep mode and changes the INH pin to a high-impedance state. The Failsafe feature of the TCAN4550 can cause the device to enter Sleep Mode if the device is not configured for Normal mode or the PWRON flag is not cleared within four minutes of powering on or exiting Sleep Mode. This Hi-Z state disables the $V_{IO}$ channel of the LDO. If this occurs, a Local Wake Up (LWU) request is required through a voltage transition on the WAKE pin or through a request on the CAN bus.

The TPS7B7702-Q1 LDO has several features that are available through the J2 header, such as current sensing, current limiting and fault detection, and error reporting. See the TPS7B7702-Q1 data sheet for more information on those features. Figure 2 shows the external LDO features.

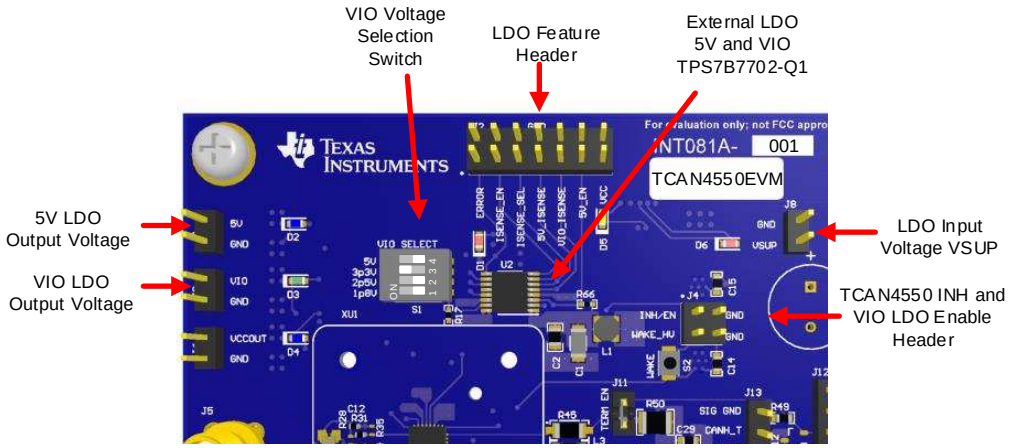


**Figure 2. External LDO Features**

### 2.1.4 $V_{IO}$ Voltage Selection Switch (S1)

The TPS7B7702-Q1 LDO is an adjustable LDO that uses a resistor divider between the output pin and a feedback pin to regulate the output voltage. Four different resistor divider options are provided on the EVM to allow $V_{IO}$ to be set to 5 V, 3.3 V, 2.5 V, and 1.8 V through the change of the DIP switch configuration on switch S1. The TCAN4550 only supports $V_{IO}$ levels of 5 V and 3.3 V. The 2.5 V and 1.8 V settings have been added to the board in case future versions of the TCAN4550 are developed with support for these common voltage levels. There is a common resistor between the output voltage pin, the feedback pin, and one side of all four DIP switch positions. A separate resistor has been placed between the other side of each DIP switch position and GND to create the voltage divider. Only one DIP switch at a time should be connected in the ON position (toward the silkscreen voltage labels). If more than one switch at a time is ON, the resistors to GND are in parallel and alter the voltage created by the resistor divider circuit and cause $V_{IO}$ to be regulated to a voltage other than one of the four standard options.

## 2.2 CAN

The following sections describe the features of the CAN. Figure 3 shows the CAN bus features.

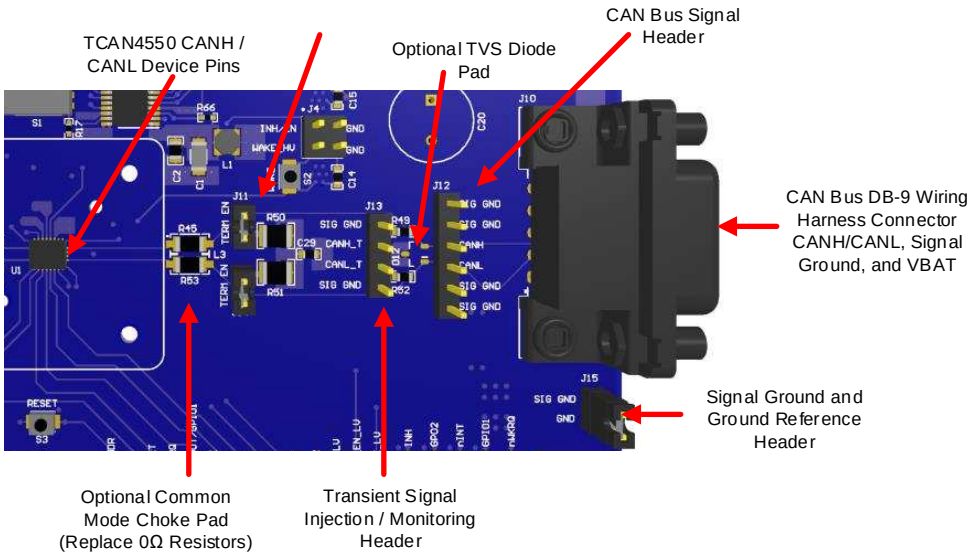


**Figure 3. CAN Bus Features**

### 2.2.1 CAN Bus DB-9 Connector (J10)

The CAN bus signals CANH and CANL are accessible through the DB-9 connector J10, which follows the industry-standard pin mapping. This mapping allows for easy integration into an existing system. The external supply voltage $V_{BAT}$, signal ground, and connector shield ground connections are also included in connector J10.

### 2.2.2 CAN Bus Signal Header (J12)

The CAN bus signals are also available on header J12. This may be more convenient in a lab environment or to attach scope probes to monitor the bus connected to the EVM through the DB-9 connector.

### 2.2.3 CAN Bus Signal Ground Reference

The EVM contains a separate GND plane that is used as the reference for the CAN signals called Signal GND. Potential differences between the GND nodes often exist in systems with a bus architecture resulting in common-mode offsets of the CAN signals. The TCAN4550 is designed to handle these differences. A DC voltage can be injected onto the Signal GND plane relative to the GND plane to simulate this offset and shift the common-mode of the CAN signals through header J15. By default, the Signal GND and GND planes are shorted together by placing a shunt on header J15.

### 2.2.4 TVS Diode (D12)

A TVS diode footprint has been added to the EVM if evaluation with additional ESD protection is required, but this is not populated by default nor required in all applications.

### 2.2.5 Transient Signal Injection/Monitoring Header (J13)

Many tests are commonly run on CAN transceivers that require some form of transient signal injection, or some form of additional bus loading. To accommodate these types of tests, header J13 and series resistors R49 and R52 have been added to the EVM. These components are not required for a final application and can be used or modified as desired during the evaluation.

### 2.2.6 Termination

The CAN standard requires termination of the CAN bus at each end with 120 Ω of resistance between the CANH and CANL pins. A common technique, also used on this EVM, is to implement a split termination using two 60-Ω resistors in series and a 4.7-nF capacitor to ground. The capacitor to ground provides a path for filtering common-mode noise out of the signals that can come from sources such as asymmetry between the CANH and CANL signals. Common-mode noise is a result of unequal lengths between the CANH and CANL wires, asymmetrical loading, or other sources. If the EVM is used in a lab environment or as one of the end nodes of the CAN bus, the termination can be enabled by placing shunts on jumpers J11 and J14 to connect the termination resistors to the CANH and CANL lines. However, if the EVM is used on a bus with existing termination resistors or does not require local termination, removing the shunts on J11 and J14 disconnects the local termination from the CANH and CANL lines. It is also possible to evaluate the TCAN4550 with one 120-Ω resistor by removing the two 60-Ω resistors, R50 and R51, and installing one 120-Ω resistor in their place using one pad of R50 and one pad of R51.

### 2.2.7 Common-Mode Choke

Many applications have system-level electromagnetic compatibility (EMC) requirements that may require the use of a common-mode choke on the CAN pins. A typical common-mode choke pad has been added to the EVM for the user to add their desired choke. However, by default, 0-Ω resistors have been placed across the choke pins to connect the CANH and CANL pins of the TCAN4550 device with the rest of the CAN bus connectors and features of the EVM. To add a choke to the EVM, simply remove resistors R45 and R53 from the EVM and install the choke in their place.

## 2.3 Clocking

Figure 4 shows the clocking features on the board.

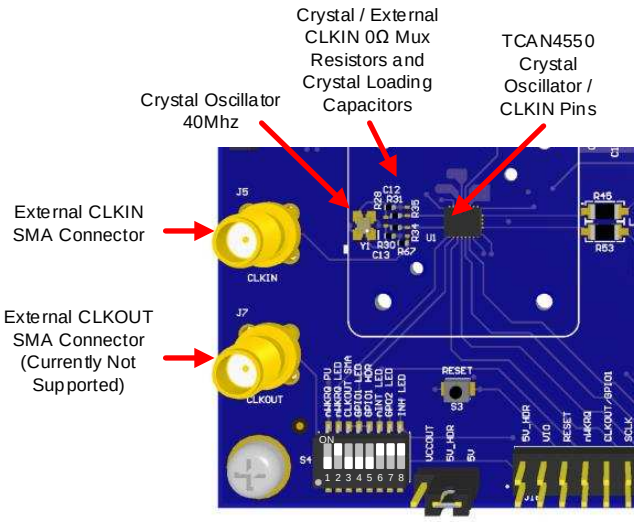


**Figure 4. Clocking Features**

### 2.3.1 Crystal/CLKIN

The TCAN4550 requires either a crystal oscillator, or a single-ended clock to run its digital core. A 40-MHz crystal oscillator is installed and connected to the OSC1/CLKIN and OSC2 pins by default and will be available whenever $V_{IO}$ is present. However, a simple configuration change of two 0-Ω resistors allows use of an external CLKIN through the SMA connector J5. To enable the external clock source, remove resistors R30 and R31 and install them in the locations for resistors R34 and R35. The installation of R30 and R31 serve the purpose of a MUX, and all four resistors should not be installed simultaneously.

### 2.3.2 CLKOUT, SMA (J7)

The TCAN4550 does not currently support a CLKOUT feature, but the SMA connector is on the EVM in case future version of the device are developed with a CLKOUT feature.

## 2.4 MCU Interface (SPI/GPIO)

Figure 5 shows the MCU interface.

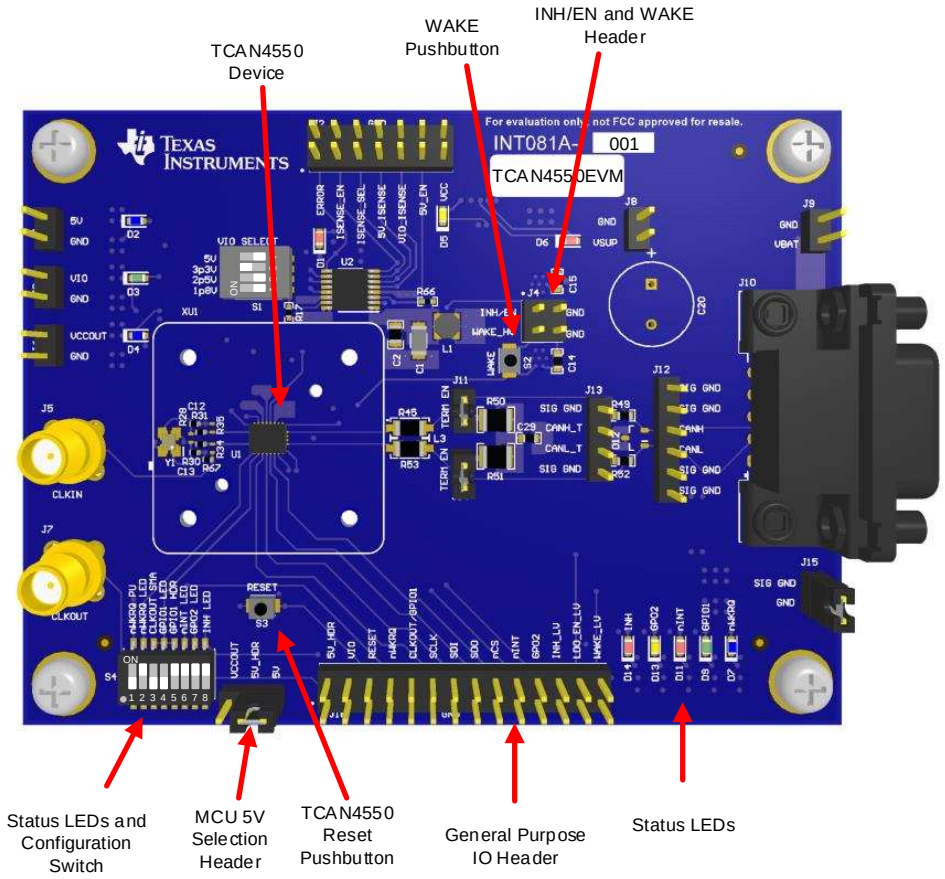


**Figure 5. MCU Interface (SPI/GPIO) Features**

### 2.4.1 General-Purpose I/O Header (J16)

The TCAN4550 requires a MCU or other SPI controller for configuration and operation. A specific MCU has not been included on the EVM to allow evaluation of the TCAN4550 device with any MCU board or SPI controller. All GPIO signals are available on a single header (J16), thus allowing a convenient connection to the MCU board through a ribbon cable or fly wires. A GND pin has been added next to each signal pin. These GND pins place a GND wire between each signal wire if a ribbon cable is used. Furthermore, 2-pin coax cables can be used for better signal integrity compared to unshielded fly wires, or for a convenient GND reference for scope probes and other test equipment. Both a 5-V reference and the $V_{IO}$ voltages are available on this header and can be used as the power supply for the MCU board and evaluate sleep and wake events used in integrated designs. The 5-V source can be configured to come from either the 5-V utility rail of the EVM, which is always present when VSUP is present, or from VCCOUT, which is present only when the TCAN4550 is not in sleep mode through the shunt position of header J17.

### 2.4.2 Status LEDs and Configuration Switch (S4)

Several TCAN4550 I/O pins have multiple functions that can be configured through the SPI registers, and a single multichannel DIP switch (S4) makes it easy to configure the EVM hardware to support the various I/O features. Most of the DIP switches are used to disconnect the traces to the LED circuits from the I/O signals to prevent stubs or extra loading on signals that might be sensitive to reflections and poor signal integrity. An example of when the LED should be disconnected is when the transceiver test mode is configured to use the GPIO1 pin for TXD and the GPO2 pin as RXD.

All I/O signals from the TCAN4550 device are connected directly to the general-purpose header J16, with the exception of the GPIO1 pin. The GPIO1 pin runs through switch positions 3, 4, and 5 of switch S4 to route the currently unsupported CLKOUT signal to the SMA connector (J7) and prevent creation of a stub by header J16 or status LED (D9).

All status LEDs on the EVM are sourced from the 5-V utility rail and buffered through a pair of transistors (CSD85301Q2). Because some of the signals where an LED is useful, such as nINT and nWKRQ, use negative logic, a second transistor has been added to invert the signals and allow the LED to be on when the IO pin voltage is in the active low state. All pullup resistors connected to the TCAN4550 side of the LED circuit are biased to the VIO rail to accommodate the desired I/O voltage of the MCU.

An LED has been added to each DC power rail on the EVM buffered through a transistor and sourced from the 5-V utility rail to not add to the current load of the individual rails more than the current needed for a 10-kΩ pullup resistor. For more precise current measurements on the VIO and VCCOUT rails, remove these resistors. Furthermore, to account for a large voltage range of VSUP, a large voltage divider is used on the gate of the FET that controls the VSUP LED (D6).

### 2.4.3 WAKE pin

The WAKE pin is considered a high-voltage input pin because it is referenced to the VSUP power rail and not the lower voltage VIO or VCC rail.

**CAUTION**

TI does not recommend connecting the WAKE signal directly to an MCU because the voltage rating of the IO pins is typically much lower than the $V_{SUP}$ voltage and damage to the MCU may occur.

A high-voltage FET (CSD18543Q3A) has been placed between the WAKE pin and GND and the gate of the FET is connected to pin 28 of the general-purpose header (J16). This allows the MCU to use a regular IO pin to cause a high-to-low transition on the WAKE pin to wake up the TCAN4550 device from sleep mode. The EVM also has a momentary push-button switch (S2) that can be used for a manual wake event from a high-to-low transition when pressed. However, by default, the WAKE pin is configured to be a bidirectional edge trigger and to recognize any direction transition as a wake event. This can be reconfigured as a rising only or falling only trigger as described in the data sheet, and pin 3 on header J4 that can be used to monitor or control the WAKE signal.

### 2.4.4 INH Pin and VIO Enable

The INH pin is considered a high-voltage output pin because it is referenced to the VSUP power rail and not the lower voltage VIO or VCCOUT rail. If the INH pin is used, it is typically connected to the enable pin of a regulator used to support the MCU and VIO rail. It outputs a voltage equal to VSUP, minus a diode drop, in all modes but sleep mode when the pin becomes high impedance. To ensure that a low voltage is applied to the enable pin of the regulator in sleep mode, a pulldown resistor is used to hold the line low when INH is high impedance.

The default configuration of the EVM has the INH pin of the TCAN4550 connected to the VIO enable pin. However, a 1-Ω resistor (R36) has been placed in series between these two pins and can be removed to isolate the enable and INH pins. If this is done, the 10-kΩ pullup resistor (R23) should be installed to provide a high-voltage reference for the VIO enable pin.

External control of the high-voltage LDO enable pin, or monitoring of the INH pin, can be done directly through pin 1 of header J4. A high-voltage FET (CSD18543Q3A) has been placed between the EN and GND pins with the gate of the FET connected to pin 26 of the general-purpose header (J16) to provide a low-voltage control option through the MCU. A low-voltage monitoring option of the INH pin is available through pin 24 of the general-purpose header (J16) and a status LED (D14). A voltage comparator (LMV331QDBVRQ1) is used to compare the INH voltage against a reference voltage generated with a voltage divider on the 5-V utility rail. The reference voltage divider is set to accommodate an INH signal with the maximum $V_{SUP}$ voltage tolerated without any modification to the EVM. The eighth switch in the configuration DIP switch (S4) disconnects the low-voltage enable signal from the status LED (D14).

The low-voltage control and monitoring options of the EVM, along with the wake request pin (nWKRQ) of the TCAN4550, allow an alternative approach to placing the node into sleep and waking it up again. If the system is in sleep mode, and a wake event occurs either through a local wake event on the WAKE pin or though activity on the CAN bus, the MCU can detect the INH pin going high through the INH_LV signal on pin 24 of the general-purpose header (J16). The MCU can then change the state of the VIO enable pin through the LDO_EN_LV signal on pin 28 of the general-purpose header (J16) to enable the $V_{IO}$ voltage rail for normal operation. However, this approach requires that the 5-V utility rail and the MCU remain on while TCAN4550 is in sleep mode to monitor for a wake event.

## *2.5 TCAN4550 Device*

By default, the EVM comes installed with the TCAN4550 device soldered to the board, but it can also be used with a socket from RS Tech Incorporated (PN: SK02-0020QFN-CS-02A).

## 3 Board Layout

Figure 6 and Figure 7 show the top and bottom, respectively, of the EVM.

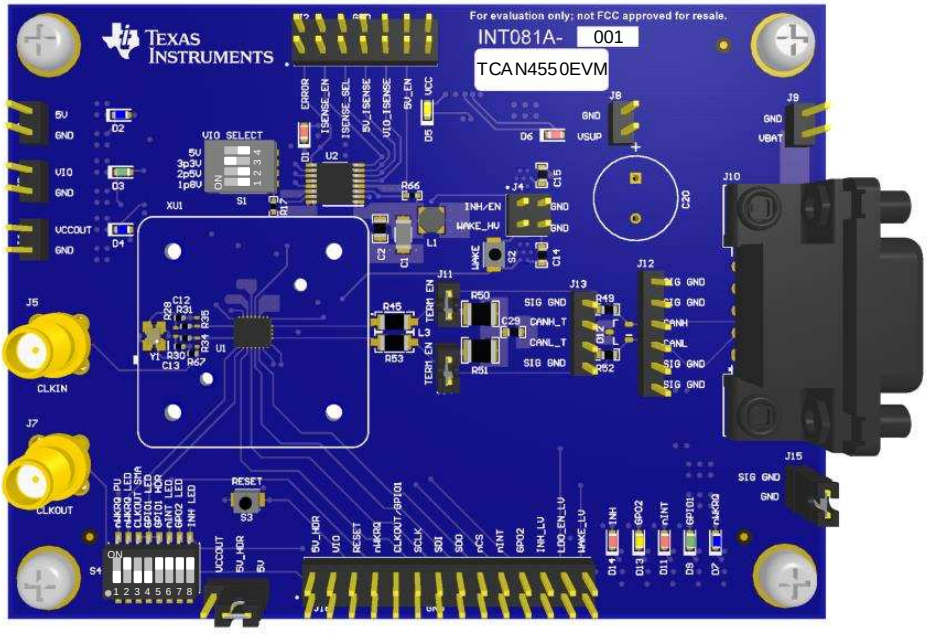


**Figure 6. EVM Top**

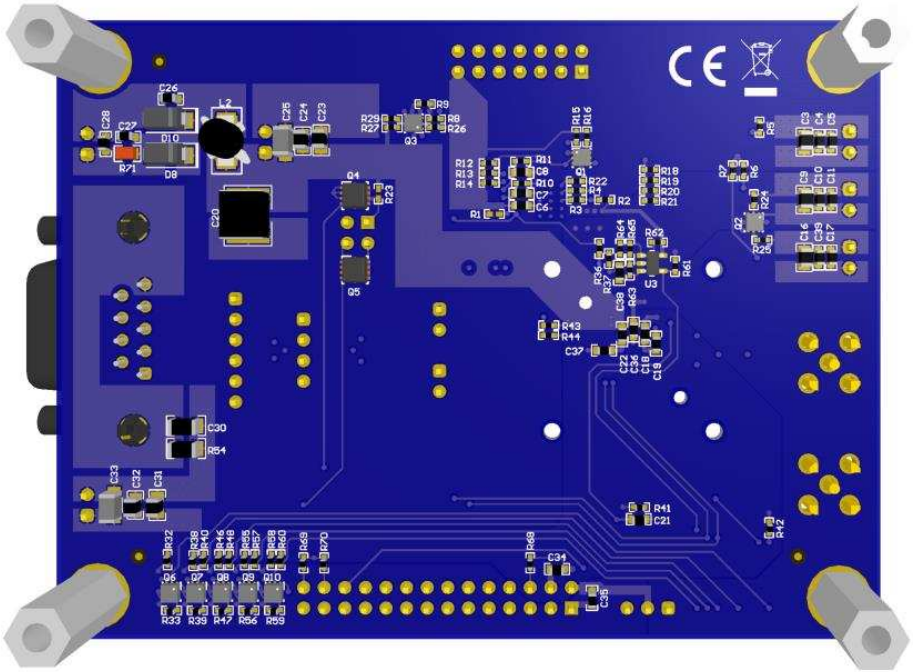

**Figure 7. EVM Bottom**

# 4 Schematic and Bill of Materials

## 4.1 Schematic

Figure 8 is a schematic diagram of the EVM.

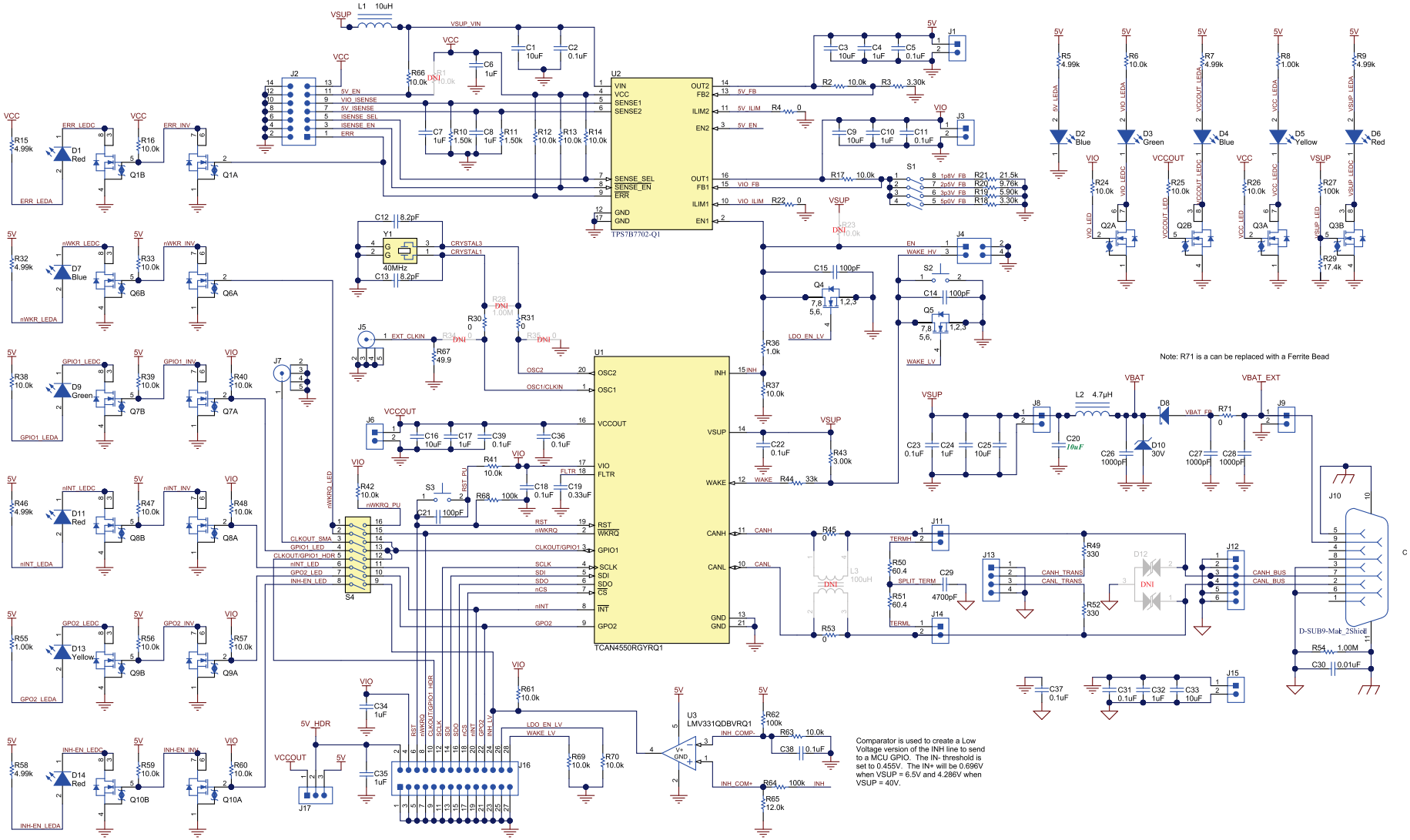


**Figure 8. EVM Schematic**

## 4.2 Bill of Materials

Table 1 lists the bill of materials (BOM).

**Table 1. Bill of Materials**

| Designator | Qty | Value | Description | Package Reference | Part Number | Manufacturer | Alternate Part Number[1] | Alternate Manufacturer[1] |
|---|---|---|---|---|---|---|---|---|
| !PCB1 | 1 | | Printed Circuit Board | | INT081 | Any | | |
| C1, C25, C33 | 3 | 10uF | CAP, CERM, 10 uF, 50 V, +/- 10%, X7R, 1206 | 1206 | CL31B106KBHNNNE | Samsung | | |
| C2, C23, C31 | 3 | 0.1uF | CAP, CERM, 0.1 uF, 50 V, +/- 5%, X7R, 0805 | 0805 | 08055C104JAT2A | AVX | | |
| C3, C9, C16 | 3 | 10uF | CAP, CERM, 10 uF, 16 V, +/- 10%, X7R, 0805 | 0805 | CL21B106KOQNNNE | Samsung Electro-Mechanics | | |
| C4, C6, C7, C8, C10, C17, C34, C35 | 8 | 1uF | CAP, CERM, 1 uF, 35 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603 | 0603 | CGA3E1X7R1V105K080AC | TDK | | |
| C12, C13 | 2 | 8.2pF | CAP, CERM, 8.2 pF, 25 V, +/- 5%, C0G/NP0, 0402 | 0402 | GRM1555C1E8R2CA01D | MuRata | | |
| C14, C15, C21 | 3 | 100pF | CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603 | 0603 | 06035A101JAT2A | AVX | | |
| C19 | 1 | 0.33uF | CAP, CERM, 0.33 uF, 16 V, +/- 10%, X7R, 0603 | 0603 | C0603C334K4RACTU | Kemet | | |
| C20 | 1 | 10uF | CAP, CERM, 10 uF, 50 V, +/- 10%, X7R, | | C5750X7R1H106K230KB | TDK | | |
| C24, C32 | 2 | 1uF | CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0805 | 0805 | 08055C105KAT2A | AVX | | |
| C26, C27, C28 | 3 | 1000pF | CAP, CERM, 1000 pF, 100 V, +/- 5%, X7R, 0603 | 0603 | 06031C102JAT2A | AVX | | |
| C29 | 1 | 4700pF | CAP, CERM, 4700 pF, 100 V, +/- 5%, X7R, 0603 | 0603 | 06031C472JAT2A | AVX | | |
| C30 | 1 | 0.01uF | CAP, CERM, 0.01 uF, 100 V, +/- 10%, X7R, 1206 | 1206 | 12061C103KAT2A | AVX | | |
| D1, D6, D11, D14 | 4 | Red | LED, Red, SMD | LED_0603 | 150060RS75000 | Wurth Elektronik | | |
| D2, D4, D7 | 3 | Blue | LED, Blue, SMD | LED_0603 | 150060BS75000 | Wurth Elektronik | | |
| D3, D9 | 2 | Green | LED, Green, SMD | LED_0603 | 150060GS75000 | Wurth Elektronik | | |
| D5, D13 | 2 | Yellow | LED, Yellow, SMD | LED_0603 | 150060YS75000 | Wurth Elektronik | | |
| D8 | 1 | 40V | Diode, Schottky, 40 V, 1 A, SMA | SMA | MBRA140T3G | ON Semiconductor | | |
| D10 | 1 | 30V | Diode, Zener, 30 V, 3 W, SMA | SMA | 3SMAJ5936B-TP | Micro Commercial Components | | |
| H1, H2, H3, H4 | 4 | | Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead | Screw | NY PMS 440 0025 PH | B& F Fastener Supply | | |
| H5, H6, H7, H8 | 4 | | Standoff, Hex, 0.5"L #4-40 Nylon | Standoff | 1902C | Keystone | | |
| J1, J3, J6, J8, J9, J11, J14, J15 | 8 | | Header, 100mil, 2x1, Gold, TH | 2x1 Header | TSW-102-07-G-S | Samtec | | |
| J2 | 1 | | Header, 100mil, 7x2, Gold, TH | 7x2 Header | TSW-107-07-G-D | Samtec | | |
| J4 | 1 | | Header, 100mil, 2x2, Gold, TH | 2x2 Header | TSW-102-07-G-D | Samtec | | |
| J5, J7 | 2 | | Connector, SMA, TH | SMA | 142-0701-201 | Cinch Connectivity | | |
| J10 | 1 | | D-Sub, 2.74mm, 9 Position, R/A, TH | D-Sub, 2.74mm, 9 Position, R/A, TH | 5747840-5 | TE Connectivity | | |
| J12 | 1 | | Header, 100mil, 6x1, Gold, TH | 6x1 Header | TSW-106-07-G-S | Samtec | | |
| J13 | 1 | | Header, 100mil, 4x1, Gold, TH | 4x1 Header | TSW-104-07-G-S | Samtec | | |
| J16 | 1 | | Header, 100mil, 14x2, Gold, TH | 14x2 Header | TSW-114-07-G-D | Samtec | | |
| J17 | 1 | | Header, 100mil, 3x1, Gold, TH | 3x1 Header | TSW-103-07-G-S | Samtec | | |
| L1 | 1 | 10uH | Inductor, Shielded Drum Core, Ferrite, 10 uH, 1 A, 0.17 ohm, SMD | Inductor, 2.8x2.8x2.8mm | 744025100 | Wurth Elektronik | | |

(1) Unless otherwise noted in the Alternate PartNumber and/or Alternate Manufacturer columns, all parts may be substituted with equivalents.

**Table 1. Bill of Materials (continued)**

| Designator | Qty | Value | Description | Package Reference | Part Number | Manufacturer | Alternate Part Number[1] | Alternate Manufacturer[1] |
|---|---|---|---|---|---|---|---|---|
| L2 | 1 | 4.7uH | Inductor, Wirewound, Ferrite, 4.7 µH, 1.65 A, 0.08 ohm, AEC-Q200 Grade 0, SMD | 6x6mm | B82462A4472M000 | TDK | | |
| LBL1 | 1 | | Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll | PCB Label 0.650 x 0.200 inch | THT-14-423-10 | Brady | | |
| Q1, Q2, Q3, Q6, Q7, Q8, Q9, Q10 | 8 | 20V | MOSFET, 2-CH, N-CH, 20 V, 6.7 A, DQK0006B (WSON-6) | DQK0006B | CSD85301Q2 | Texas Instruments | | None |
| Q4, Q5 | 2 | 60V | MOSFET, N-CH, 60 V, 35 A, DNH0008A (VSONP-8) | DNH0008A | CSD18543Q3A | Texas Instruments | | None |
| R2, R12, R13, R14, R16, R17, R24, R25, R26, R33, R37, R39, R40, R41, R42, R47, R48, R56, R57, R59, R60, R61, R63, R66, R69, R70 | 26 | 10.0k | RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | RMCF0402FT10K0 | Stackpole Electronics Inc | | |
| R3, R18 | 2 | 3.30k | RES, 3.30 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402 | 0402 | ERJ-2RKF3301X | Panasonic | | |
| R4, R22, R30, R31 | 4 | 0 | RES, 0, 5%, 0.063 W, 0402 | 0402 | RC0402JR-070RL | Yageo America | | |
| R5, R7, R9, R15, R32, R46, R58 | 7 | 4.99k | RES, 4.99 k, 1%, 0.063 W, 0402 | 0402 | RC0402FR-074K99L | Yageo America | | |
| R6, R38 | 2 | 10.0k | RES, 10.0 k, .1%, .0625 W, 0402 | 0402 | RT0402BRD0710KL | Yageo America | | |
| R8, R55 | 2 | 1.00k | RES, 1.00 k, 1%, 0.0625 W, 0402 | 0402 | RC0402FR-071KL | Yageo America | | |
| R10, R11 | 2 | 1.50k | RES, 1.50 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW04021K50FKED | Vishay-Dale | | |
| R19 | 1 | 5.90k | RES, 5.90 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW04025K90FKED | Vishay-Dale | | |
| R20 | 1 | 9.76k | RES, 9.76 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW04029K76FKED | Vishay-Dale | | |
| R21 | 1 | 21.5k | RES, 21.5 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW040221K5FKED | Vishay-Dale | | |
| R27, R62, R64, R68 | 4 | 100k | RES, 100 k, 1%, 0.0625 W, 0402 | 0402 | RC0402FR-07100KL | Yageo America | | |
| R29 | 1 | 17.4k | RES, 17.4 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW040217K4FKED | Vishay-Dale | | |
| R36 | 1 | 1.0k | RES, 1.0 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW04021K00JNED | Vishay-Dale | | |
| R43 | 1 | 3.00k | RES, 3.00 k, 1%, 0.0625 W, 0402 | 0402 | RC0402FR-073KL | Yageo America | | |
| R44 | 1 | 33k | RES, 33 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW040233K0JNED | Vishay-Dale | | |
| R45, R53 | 2 | 0 | RES, 0, 5%, 0.25 W, AEC-Q200 Grade 0, 1206 | 1206 | ERJ-8GEY0R00V | Panasonic | | |
| R49, R52 | 2 | 330 | RES, 330, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | 0603 | CRCW0603330RJNEA | Vishay-Dale | | |
| R50, R51 | 2 | 60.4 | RES, 60.4, 1%, 0.5 W, 1210 | 1210 | RC1210FR-0760R4L | Yageo | | |
| R54 | 1 | 1.00Meg | RES, 1.00 M, 1%, 0.25 W, AEC-Q200 Grade 0, 1206 | 1206 | ERJ-8ENF1004V | Panasonic | | |
| R65 | 1 | 12.0k | RES, 12.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW040212K0FKED | Vishay-Dale | | |
| R67 | 1 | 49.9 | RES, 49.9, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW040249R9FKED | Vishay-Dale | | |
| R71 | 1 | 0 | RES, 0, 1%, 0.5 W, 0805 | 0805 | 5106 | Keystone | | |
| S1 | 1 | | Switch, Slide, SPST 4 poles, SMT | SW, SMT Half Pitch 4SPST, 5.8x2.7x6.25 mm | 218-4LPST | CTS Electrocomponents | | |
| S2, S3 | 2 | | SWITCH TACTILE SPST-NO 0.05A 12V | 3x1.6x2.5mm | B3U-1000P | Omron Electronic Components | | |
| S4 | 1 | | Switch, 8SPST, 0.025 A, 24 VDC, SMD | 11.28x6.2mm | 1-1571983-1 | TE Connectivity | | |
| SH-J1, SH-J2, SH-J3, SH-J4 | 4 | | Shunt, 2.54mm, Gold, Black | Shunt, 2.54mm, Black | 60900213421 | Wurth Elektronik | | |
| U1 | 1 | | CAN-FD Controller with Integrated Transceiver, RGY0020A (VQFN-20) | RGY0020A | TCAN4550RGYRQ1 | Texas Instruments | TCAN4550RGYQ1 | Texas Instruments |

**Table 1. Bill of Materials (continued)**

| Designator | Qty | Value | Description | Package Reference | Part Number | Manufacturer | Alternate Part Number[1] | Alternate Manufacturer[1] |
|---|---|---|---|---|---|---|---|---|
| U2 | 1 | | Dual-Channel Antenna LDO With Current Sense, PWP0016J (TSSOP-16) | PWP0016J | TPS7B7702QPWPRQ1 | Texas Instruments | | Texas Instruments |
| U3 | 1 | | GENERAL-PURPOSE LOW-VOLTAGE COMPARATOR, DBV0005A (SOT-23-5) | DBV0005A | LMV331QDBVRQ1 | Texas Instruments | | Texas Instruments |
| Y1 | 1 | | Crystal, 40 MHz, 10 ppm, 8 pF, AEC-Q200 Grade 0, SMD | 2.0x0.45x1.6mm | NX2016SA-40M-STD-CZS-3 | NDK | | |
| D12 | 0 | 24V | Diode, TVS, Bi, 24 V, 70 Vc, AEC-Q101, SOT-23 | SOT-23 | PESD1CAN,215 | NXP Semiconductor | | |
| FID1, FID2, FID3, FID4, FID5, FID6 | 0 | | Fiducial mark. There is nothing to buy or mount. | N/A | N/A | N/A | | |
| L3 | 0 | 100uH | Inductor, Ferrite, 100 uH, 0.15 A, 2 ohm, SMD | SMD, 4-Leads, Body 4.7 x 3.7 mm | ACT45B-101-2P-TL003 | TDK | | |
| R1, R23 | 0 | 10.0k | RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | RMCF0402FT10K0 | Stackpole Electronics Inc | | |
| R28 | 0 | 1.00Meg | RES, 1.00 M, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW04021M00FKED | Vishay-Dale | | |
| R34, R35 | 0 | 0 | RES, 0, 5%, 0.063 W, 0402 | 0402 | RC0402JR-070RL | Yageo America | | |
| XU1 | 0 | | Socket, QFN-20, 0.5mm Pitch | Socket, QFN-20, 0.5mm Pitch | SK02-0020QFN-CS-02A | RS Tech Incorparated | | |

## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (November 2017) to A Revision | Page |
|---|---|
| • Changed the document From: *Advanced Information* To: *Production* data | 2 |

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