

## FEATURES

**Triaxial, digital gyroscope,  $\pm 450^\circ/\text{sec}$  dynamic range**

**$\pm 0.05^\circ$  orthogonal alignment error**

**$6^\circ/\text{hr}$  in-run bias stability**

**$0.3^\circ/\sqrt{\text{hr}}$  angular random walk**

**0.01% nonlinearity**

**Triaxial, digital accelerometer,  $\pm 5 g$**

**Triaxial, delta angle, and delta velocity outputs**

**Fast start-up time,  $\sim 500$  ms**

**Factory calibrated sensitivity, bias, and axial alignment**

**Calibration temperature range:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$**

**SPI-compatible serial interface**

**Embedded temperature sensor**

**Programmable operation and control**

**Automatic and manual bias correction controls**

**4 FIR filter banks, 120 configurable taps**

**Digital I/O: data-ready alarm indicator, external clock**

**Alarms for condition monitoring**

**Power-down/sleep mode for power management**

**Optional external sample clock input: up to 2.4 kHz**

**Single command self test**

**Single-supply operation: 3.0 V to 3.6 V**

**2000 g shock survivability**

**Operating temperature range:  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$**

## APPLICATIONS

Platform stabilization and control

Navigation

Personnel tracking

Instruments

Robotics

## GENERAL DESCRIPTION

The [ADIS16485](#) *iSensor*® device is a complete inertial system that includes a triaxial gyroscope and a triaxial accelerometer. Each inertial sensor in the [ADIS16485](#) combines industry-leading *iMEMS*® technology with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, alignment, and linear acceleration (gyroscope bias). As a result, each sensor has its own dynamic compensation formulas that provide accurate sensor measurements.

The [ADIS16485](#) provides a simple, cost-effective method for integrating accurate, multi-axis inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. The SPI and register structure provide a simple interface for data collection and configuration control.

The [ADIS16485](#) uses the same footprint and connector system as the [ADIS16375](#) and the [ADIS16488A](#), which greatly simplifies the upgrade process. It comes in a module that is approximately  $47\text{ mm} \times 44\text{ mm} \times 14\text{ mm}$  and has a standard connector interface.

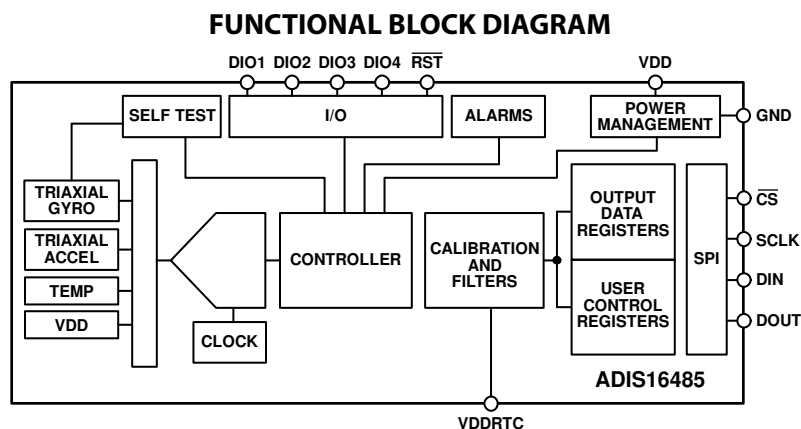


Figure 1.

Rev. H

[Document Feedback](#)

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**REVISION HISTORY****2/2019—Rev. G to Rev. H**

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| Added Endnote 3, Table 1; Renumbered Sequentially ..... | 5  |
| Added X-Ray Sensitivity Section .....                   | 31 |

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| Changes to Logic Inputs Parameter, Table 1 .....   | 4          |
| Added Endnote 4, Table 1; Renumbered Sequentially .....  | 5          |
| Changed PC-Based Evaluation, EVAL-ADIS Section Title to<br>PC-Based Evaluation, EVAL-ADIS2 Section Title ..... | 31         |
| Changes to PC-Based Evaluation, EVAL-ADIS2 Section .....   | 31         |

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|                            |    |
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| Changes to Figure 29 ..... | 31 |
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| Changes to Table 2 and Figure 2 .....                | 6  |
| Added Table 3; Renumbered Sequentially .....         | 6  |
| Change to Figure 4 .....                             | 7  |
| Change to Operating Temperature Range, Table 4 ..... | 8  |
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**5/2014—Rev. C to Rev. D**

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| Changes to Table 73, Table 74, and Table 75 ..... | 23 |
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|  |    |
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| Change to Features Section .....   | 1  |
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| Added Endnote 7; Renumbered Sequentially, and Changes to<br>Endnote 9, Table 1 .....                   | 5  |
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| Changes to Status/Alarm Indicators Section .....   | 17 |
| Deleted Prototype Interface Board Section, PC Evaluation with<br>EVAL_ADIS Section, Mechanical Design Tips Section, Figure 26,<br>Figure 27, Figure 30, and Figure 31; Renumbered Sequentially ..... | 27 |
| Added Mounting Tips Section and Figure 26; Renumbered<br>Sequentially .....  | 27 |
| Added Evaluation Tools Section, Power Supply Considerations<br>Section, Figure 29 and Figure 30; Renumbered Sequentially .....   | 28 |
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**12/2012—Rev. 0 to Rev. A**

|  |    |
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| Changes to Table 1 .....   | 3  |
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| Changes to Figure 8 .....  | 8  |
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**5/2012—Revision 0: Initial Version**

## SPECIFICATIONS

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ , angular rate =  $0^\circ/\text{sec}$ , dynamic range =  $\pm 450^\circ/\text{sec} \pm 1\text{ g}$ , 300 mbar to 1100 mbar, unless otherwise noted.

Table 1.

| Parameter  | Test Conditions/Comments  | Min       | Typ                    | Max       | Unit                                     |
|--|---|-----------|------------------------|-----------|--|
| <b>GYROSCOPES</b>                                      |   |           |                        |           |  |
| Dynamic Range  |   | $\pm 450$ |                        | $\pm 480$ | $^\circ/\text{sec}$                      |
| Sensitivity  | $x\_GYRO\_OUT$ and $x\_GYRO\_LOW$ (32-bit)                        |           | $3.052 \times 10^{-7}$ |           | $^\circ/\text{sec}/\text{LSB}$           |
| Repeatability <sup>1</sup>                             | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$               |           |                        | $\pm 1$   | %  |
| Sensitivity Temperature Coefficient                    | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , $1\sigma$   |           | $\pm 35$               |           | $\text{ppm}/^\circ\text{C}$              |
| Misalignment   | Axis-to-axis  |           | $\pm 0.05$             |           | Degrees                                  |
|  | Axis-to-frame (package)   |           | $\pm 1.0$              |           | Degrees                                  |
| Nonlinearity   | Best fit straight line, $FS = 450^\circ/\text{sec}$               |           | 0.01                   |           | % of FS                                  |
| Bias Repeatability <sup>1,2</sup>                      | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , $1\sigma$   |           | $\pm 0.2$              |           | $^\circ/\text{sec}$                      |
| In-Run Bias Stability                                  | $1\sigma$   |           | 6.25                   |           | $^\circ/\text{hr}$                       |
| Angular Random Walk                                    | $1\sigma$   |           | 0.3                    |           | $^\circ/\sqrt{\text{hr}}$                |
| Bias Temperature Coefficient                           | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , $1\sigma$   |           | $\pm 0.0025$           |           | $^\circ/\text{sec}/^\circ\text{C}$       |
| Linear Acceleration Effect on Bias                     | Any axis, $1\sigma$ (CONFIG[7] = 1)                               |           | 0.009                  |           | $^\circ/\text{sec}/\text{g}$             |
| Output Noise   | No filtering  |           | 0.16                   |           | $^\circ/\text{sec rms}$                  |
| Rate Noise Density                                     | $f = 25\text{ Hz}$ , no filtering                                 |           | 0.0066                 |           | $^\circ/\text{sec}/\sqrt{\text{Hz rms}}$ |
| 3 dB Bandwidth   |   |           | 330                    |           | Hz                                       |
| Sensor Resonant Frequency                              |   |           | 18                     |           | kHz                                      |
| <b>ACCELEROMETERS</b>                                  |   |           |                        |           |  |
| Dynamic Range  | Each axis   | $\pm 5$   |                        |           | $g$                                      |
| Sensitivity  | $x\_ACCL\_OUT$ and $x\_ACCL\_LOW$ (32-bit)                        |           | $3.815 \times 10^{-9}$ |           | $g/\text{LSB}$                           |
| Repeatability <sup>1,3</sup>                           | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$               |           |                        | $\pm 0.5$ | %  |
| Sensitivity Temperature Coefficient                    | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , $1\sigma$   |           | $\pm 10$               |           | $\text{ppm}/^\circ\text{C}$              |
| Misalignment   | Axis-to-axis  |           | $\pm 0.035$            |           | Degrees                                  |
|  | Axis-to-frame (package)   |           | $\pm 1.0$              |           | Degrees                                  |
| Nonlinearity   | Best-fit straight line, $\pm 5\text{ g}$                          |           | 0.1                    |           | % of FS                                  |
| Bias Repeatability <sup>1,2</sup>                      | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , $1\sigma$   |           | $\pm 3$                |           | $mg$                                     |
| In-Run Bias Stability                                  | $1\sigma$   |           | 32                     |           | $\mu g$                                  |
| Velocity Random Walk                                   | $1\sigma$   |           | 0.023                  |           | $\text{m}/\text{sec}/\sqrt{\text{hr}}$   |
| Bias Temperature Coefficient                           | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$               |           | $\pm 0.03$             |           | $mg/^\circ\text{C}$                      |
| Output Noise   | No filtering  |           | 1.25                   |           | $mg\text{ rms}$                          |
| Noise Density  | $f = 25\text{ Hz}$ , no filtering                                 |           | 0.055                  |           | $mg/\sqrt{\text{Hz rms}}$                |
| 3 dB Bandwidth   |   |           | 330                    |           | Hz                                       |
| Sensor Resonant Frequency                              |   |           | 5.5                    |           | kHz                                      |
| <b>TEMPERATURE SENSOR</b>                              |   |           |                        |           |  |
| Scale Factor   | Output = $0x0000$ at $25^\circ\text{C}$ ( $\pm 5^\circ\text{C}$ ) |           | 0.00565                |           | $^\circ\text{C}/\text{LSB}$              |
| <b>LOGIC INPUTS<sup>4</sup></b>                        |   |           |                        |           |  |
| Input High Voltage, $V_{IH}$                           |   | 2.0       |                        |           | V  |
| Input Low Voltage, $V_{IL}$                            |   |           |                        | 0.8       | V  |
| $\overline{CS}$ Wake-Up Pulse Width                    |   | 20        |                        |           | $\mu\text{s}$                            |
| Logic 1 Input Current, $I_{IH}$                        | $V_{IH} = 3.3\text{ V}$   |           |                        | 10        | $\mu\text{A}$                            |
| Logic 0 Input Current, $I_{IL}$                        | $V_{IL} = 0\text{ V}$   |           |                        |           | $\mu\text{A}$                            |
| All Pins Except $\overline{RST}$ and $\overline{CS}$   |   |           |                        | 10        | $\mu\text{A}$                            |
| $\overline{RST}$ and $\overline{CS}$ Pins <sup>5</sup> |   |           | 0.33                   |           | $\text{mA}$                              |
| Input Capacitance, $C_{IN}$                            |   |           | 10                     |           | $\text{pF}$                              |
| <b>DIGITAL OUTPUTS</b>                                 |   |           |                        |           |  |
| Output High Voltage, $V_{OH}$                          | $I_{SOURCE} = 0.5\text{ mA}$                                      | 2.4       |                        |           | V  |
| Output Low Voltage, $V_{OL}$                           | $I_{SINK} = 2.0\text{ mA}$  |           |                        | 0.4       | V  |

| Parameter  | Test Conditions/Comments   | Min           | Typ  | Max | Unit                             |
|--|--|---------------|--|-----|----------------------------------|
| FLASH MEMORY<br>Data Retention <sup>7</sup>  | Endurance <sup>6</sup><br>T <sub>J</sub> = 85°C  | 100,000<br>20 |  |     | Cycles<br>Years                  |
| FUNCTIONAL TIMES <sup>8</sup><br>Power-On, Start-Up Time<br>Reset Recovery Time <sup>9</sup><br>Sleep Mode Recovery Time<br>Flash Memory Update Time<br>Flash Memory Test Time<br>Automatic Self Test Time | Time until data is available<br><br><br><br><br>Using internal clock, 100 SPS  |               | 400 ± 160<br>400 ± 160<br>500<br>900<br>66<br>12 |     | ms<br>ms<br>µs<br>ms<br>ms<br>ms |
| CONVERSION RATE<br>Initial Clock Accuracy<br>Temperature Coefficient<br>Sync Input Clock <sup>10</sup>   |  |               | 2.46<br>0.02<br>40                               |     | kSPS<br>%<br>ppm/°C<br>kHz       |
| POWER SUPPLY, VDD<br>Power Supply Current <sup>11</sup>  | Operating voltage range<br>Normal mode, VDD = 3.3 V, $\mu \pm \sigma$<br>Sleep mode, VDD = 3.3 V<br>Power-down mode, VDD = 3.3 V | 3.0           |  | 3.6 | V<br>mA<br>mA<br>µA              |
| POWER SUPPLY, VDDRTC<br>Real-Time Clock Supply Current   | Operating voltage range<br>Normal mode, VDDRTC = 3.3 V   | 3.0           |  | 3.6 | V<br>µA                          |

<sup>1</sup> The repeatability specifications represent analytical projections that are based off of the following drift contributions and conditions: temperature hysteresis (−40°C to +85°C), electronics drift (high temperature operating life test: +110°C, 500 hours), drift from temperature cycling (JEDEC22, Method A104-C, Method N, 500 cycles, −40°C to +85°C), rate random walk (10 year projection), and broadband noise

<sup>2</sup> Bias repeatability describes a long-term behavior over a variety of conditions. Short-term repeatability is related to the in-run bias stability and noise density specifications.

<sup>3</sup> X-ray exposure may degrade this performance metric.

<sup>4</sup> The digital I/O signals use a 3.3 V system.

<sup>5</sup>  $\overline{RST}$  and  $\overline{CS}$  pins are connected to the VDD pin through 10 kΩ pull-up resistors.

<sup>6</sup> Endurance is qualified as per JEDEC Standard 22, Method A117, and measured at −40°C, +25°C, +85°C, and +125°C.

<sup>7</sup> The data retention specification assumes a junction temperature (T<sub>J</sub>) of 85°C as per JEDEC Standard 22, Method A117. Data retention lifetime decreases with T<sub>J</sub>.

<sup>8</sup> These times do not include thermal settling and internal filter response times, which can affect overall accuracy.

<sup>9</sup> The  $\overline{RST}$  line must be in a low state for at least 10 µs to assure a proper reset initiation and recovery.

<sup>10</sup> The device functions at clock rates below 0.7 kHz but at reduced performance levels.

<sup>11</sup> Supply current transients can reach 600 mA during start-up and reset recovery.

**TIMING SPECIFICATIONS**

T<sub>A</sub> = 25°C, VDD = 3.3 V, unless otherwise noted.

**Table 2.**

| Parameter                         | Description                                    | Min <sup>1</sup> | Normal Mode |                  | Unit |
|-----------------------------------|--|------------------|-------------|------------------|------|
|                                   |  |                  | Typ         | Max <sup>1</sup> |      |
| f <sub>SCLK</sub>                 | Serial clock                                   | 0.01             |             | 15               | MHz  |
| t <sub>STALL</sub> <sup>2</sup>   | Stall period between data communication cycles | 2                |             |                  | μs   |
| t <sub>CLS</sub>                  | Serial clock low period                        | 31               |             |                  | ns   |
| t <sub>CHS</sub>                  | Serial clock high period                       | 31               |             |                  | ns   |
| t <sub>CS</sub>                   | Chip select to clock edge                      | 32               |             |                  | ns   |
| t <sub>DAV</sub>                  | DOUT valid after SCLK edge                     |                  |             | 10               | ns   |
| t <sub>DSU</sub>                  | DIN setup time before SCLK rising edge         | 2                |             |                  | ns   |
| t <sub>DHD</sub>                  | DIN hold time after SCLK rising edge           | 2                |             |                  | ns   |
| t <sub>DR</sub> , t <sub>DF</sub> | DOUT rise/fall times, ≤100 pF loading          |                  | 3           | 8                | ns   |
| t <sub>DSOE</sub>                 | CS assertion to data out active                | 0                |             | 11               | ns   |
| t <sub>HD</sub>                   | SCLK edge to data out invalid                  | 0                |             |                  | ns   |
| t <sub>SFS</sub>                  | Last SCLK edge to CS deassertion               | 32               |             |                  | ns   |
| t <sub>DSHI</sub>                 | CS deassertion to data out high impedance      | 0                |             | 9                | ns   |
| t <sub>1</sub>                    | Input sync pulse width                         | 5                |             |                  | μs   |
| t <sub>2</sub>                    | Input sync to data invalid                     |                  | 510         |                  | μs   |
| t <sub>3</sub>                    | Input sync period                              | 417              |             |                  | μs   |

<sup>1</sup> Guaranteed by design and characterization, but not tested in production.

<sup>2</sup> See Table 3 for exceptions to the stall time rating.

**Table 3. Register Specific Stall Times**

| Register    | Function                         | Minimum Stall Time (μs) |
|-------------|----------------------------------|-------------------------|
| FNCTIO_CTRL | Configure DIOx functions         | 60                      |
| FLTR_BNK0   | Enable/select FIR filter banks   | 320                     |
| FLTR_BNK1   | Enable/select FIR filter banks   | 320                     |
| NULL_CFG    | Configure autonull bias function | 10                      |
| GLOB_CMD[1] | Self test                        | 12,000                  |
| GLOB_CMD[2] | Memory test                      | 50,000                  |
| GLOB_CMD[3] | Flash memory update              | 375,000                 |
| GLOB_CMD[6] | Flash memory test                | 75,000                  |
| GLOB_CMD[7] | Software reset                   | 12,000                  |

Timing Diagrams

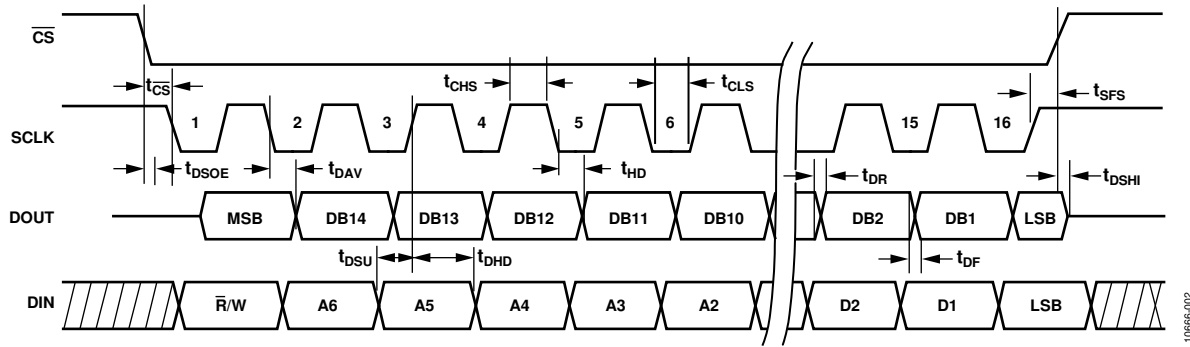


Figure 2. SPI Timing and Sequence

10666-002

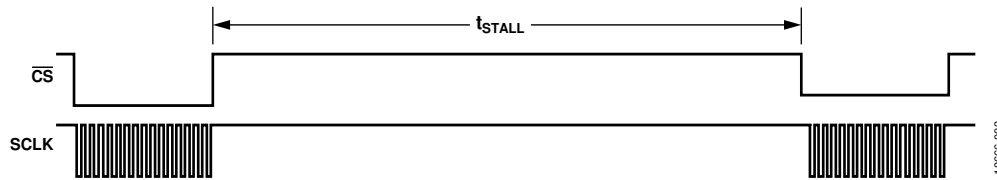


Figure 3. Stall Time and Data Rate

10666-003

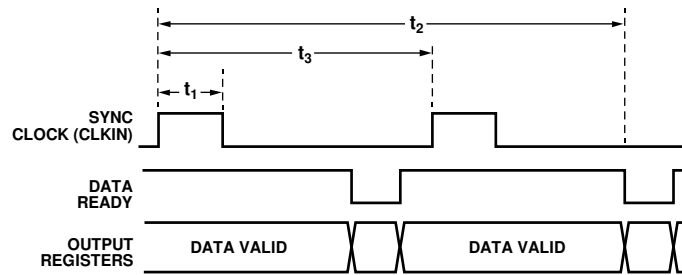


Figure 4. Input Clock Timing Diagram

10666-004

## ABSOLUTE MAXIMUM RATINGS

Table 4.

| Parameter                     | Rating                       |
|-------------------------------|------------------------------|
| Acceleration                  |                              |
| Any Axis, Unpowered           | 2000 <i>g</i>                |
| Any Axis, Powered             | 2000 <i>g</i>                |
| VDD to GND                    | -0.3 V to +3.6 V             |
| Digital Input Voltage to GND  | -0.3 V to VDD + 0.2 V        |
| Digital Output Voltage to GND | -0.3 V to VDD + 0.2 V        |
| Operating Temperature Range   | -40°C to +105°C              |
| Storage Temperature Range     | -65°C to +150°C <sup>1</sup> |

<sup>1</sup> Extended exposure to temperatures that are lower than -40°C or higher than +105°C can adversely affect the accuracy of the factory calibration.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 5. Package Characteristics

| Package Type             | $\theta_{JA}$ | $\theta_{JC}$ | Device Weight |
|--------------------------|---------------|---------------|---------------|
| 24-Lead Module (ML-24-6) | 22.8°C/W      | 10.1°C/W      | 48 <i>g</i>   |

### ESD CAUTION

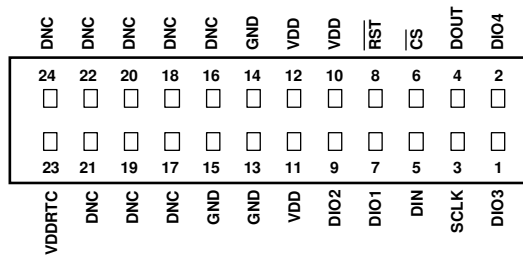


**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

ADIS16485  
TOP VIEW  
(Not to Scale)

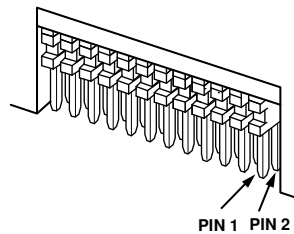
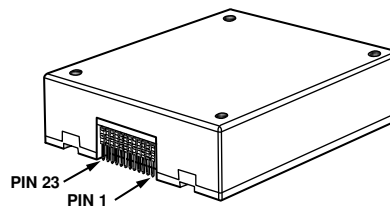


**NOTES**

1. THIS REPRESENTATION DISPLAYS THE TOP VIEW PINOUT FOR THE MATING SOCKET CONNECTOR.
2. THE ACTUAL CONNECTOR PINS ARE NOT VISIBLE FROM THE TOP VIEW.
3. MATING CONNECTOR: SAMTEC CLM-112-02 OR EQUIVALENT.
4. DNC = DO NOT CONNECT.

10686-005

Figure 5. Mating Connector Pin Assignments



10686-106

Figure 6. Axial Orientation (Top Side Facing Up)

Table 6. Pin Function Descriptions

| Pin No.      | Mnemonic          | Type           | Description  |
|--------------|-------------------|----------------|--|
| 1            | DIO3              | Input/output   | Configurable Digital Input/Output.                   |
| 2            | DIO4              | Input/output   | Configurable Digital Input/Output.                   |
| 3            | SCLK              | Input          | SPI Serial Clock.                                    |
| 4            | DOUT              | Output         | SPI Data Output. Clocks output on SCLK falling edge. |
| 5            | DIN               | Input          | SPI Data Input. Clocks input on SCLK rising edge.    |
| 6            | $\overline{CS}$   | Input          | SPI Chip Select.                                     |
| 7            | $\overline{DIO1}$ | Input/output   | Configurable Digital Input/Output.                   |
| 8            | $\overline{RST}$  | Input          | Reset.   |
| 9            | DIO2              | Input/output   | Configurable Digital Input/Output.                   |
| 10, 11, 12   | VDD               | Supply         | Power Supply.  |
| 13, 14, 15   | GND               | Supply         | Power Ground.  |
| 16 to 22, 24 | DNC               | Not applicable | Do Not Connect to These Pins.                        |
| 23           | VDDRTC            | Supply         | Real-Time Clock Power Supply.                        |

TYPICAL PERFORMANCE CHARACTERISTICS

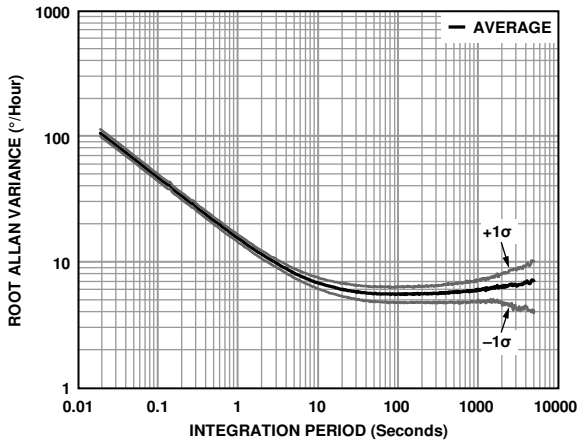


Figure 7. Gyroscope Allan Variance, 25°C

10666-007

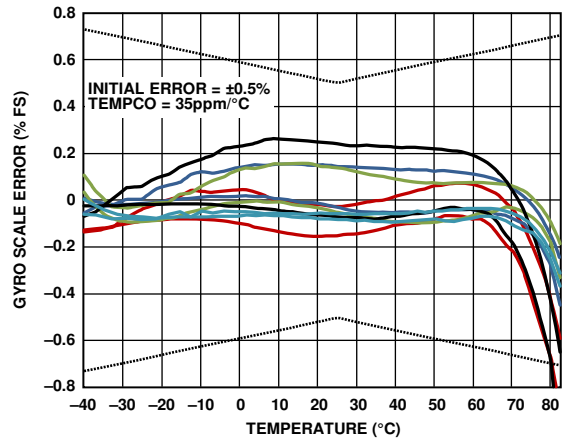


Figure 9. Gyroscope Scale (Sensitivity) Error and Hysteresis vs. Temperature

10666-009

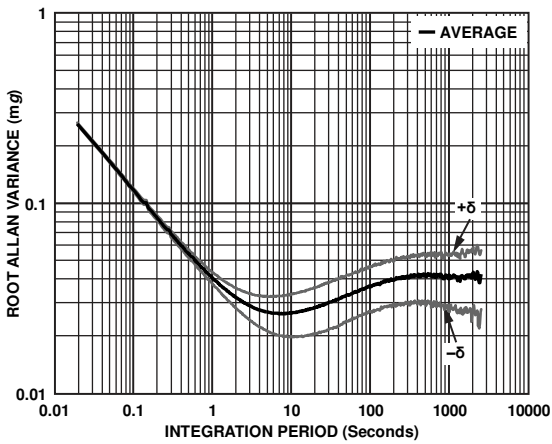


Figure 8. Accelerometer Allan Variance, 25°C

10666-008

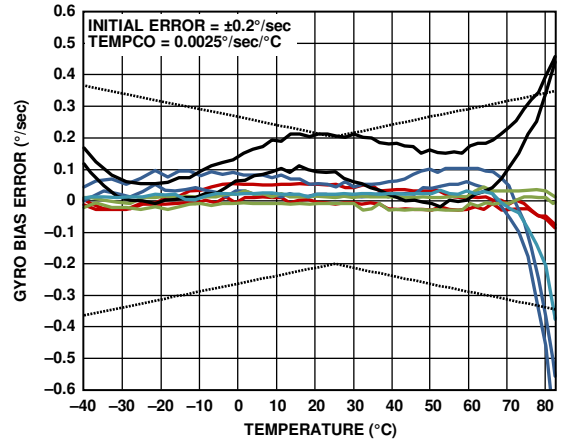


Figure 10. Gyroscope Bias Error and Hysteresis vs. Temperature

10666-010

## BASIC OPERATION

The ADIS16485 is an autonomous sensor system that starts up on its own when it has a valid power supply. After running through its initialization process, it begins sampling, processing, and loading calibrated sensor data into the output registers, which are accessible using the SPI port. The SPI port typically connects to a compatible port on an embedded processor, using the connection diagram in Figure 11. The four SPI signals facilitate synchronous, serial data communication. Connect  $\overline{RST}$  (Pin 8, see Table 6) to VDD or leave  $\overline{RST}$  open for normal operation. The factory default configuration provides users with a data-ready signal on the DIO2 pin, which pulses high when new data is available in the output data registers.

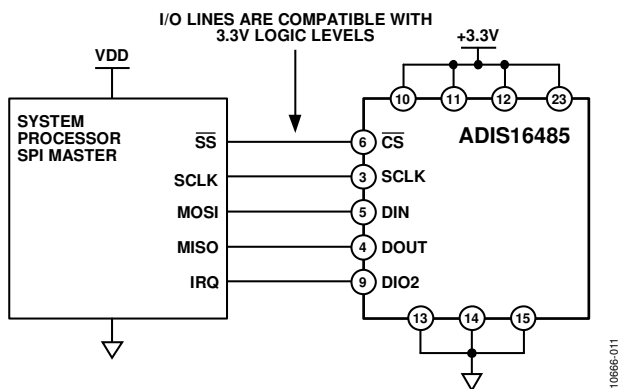


Figure 11. Electrical Connection Diagram

Table 7. Generic Master Processor Pin Names and Functions

| Mnemonic | Function                   |
|----------|----------------------------|
| SS       | Slave select               |
| IRQ      | Interrupt request          |
| MOSI     | Master output, slave input |
| MISO     | Master input, slave output |
| SCLK     | Serial clock               |

Embedded processors typically use control registers to configure their serial ports for communicating with SPI slave devices such as the ADIS16485. Table 8 provides a list of settings, which describe the SPI protocol of the ADIS16485. The initialization routine of the master processor typically establishes these settings using firmware commands to write them into its serial control registers.

Table 8. Generic Master Processor SPI Settings

| Processor Setting | Description                               |
|-------------------|---|
| Master            | ADIS16485 operates as slave               |
| SCLK ≤ 15 MHz     | Maximum serial clock rate                 |
| SPI Mode 3        | CPOL = 1 (polarity), and CPHA = 1 (phase) |
| MSB-First Mode    | Bit sequence                              |
| 16-Bit Mode       | Shift register/data length                |

## REGISTER STRUCTURE

The register structure and SPI port provide a bridge between the sensor processing system and an external, master processor. It contains both output data and control registers. The output data registers include the latest sensor data, a real-time clock, error flags, alarm flags, and identification data. The control registers include sample rate, filtering, input/output, alarms, calibration, and diagnostic configuration options. All communication between the ADIS16485 and an external processor involves either reading or writing to one of the user registers.

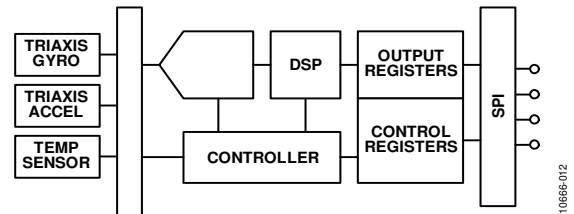


Figure 12. Basic Operation

The register structure uses a paged addressing scheme that is composed of 13 pages, with each one containing 64 register locations. Each register is 16 bits wide, with each byte having its own unique address within the memory map of that page. The SPI port has access to one page at a time, using the bit sequence in Figure 17. Select the page to activate for SPI access by writing its code to the PAGE\_ID register. Read the PAGE\_ID register to determine which page is currently active. Table 9 displays the PAGE\_ID contents for each page, together with their basic functions. The PAGE\_ID register is located at Address 0x00 on every page.

Table 9. User Register Page Assignments

| Page | PAGE_ID | Function   |
|------|---------|--|
| 0    | 0x00    | Output data, clock, identification                   |
| 1    | 0x01    | Reserved   |
| 2    | 0x02    | Calibration  |
| 3    | 0x03    | Control: sample rate, filtering, I/O, alarms         |
| 4    | 0x04    | Serial number  |
| 5    | 0x05    | FIR Filter Bank A Coefficient 0 to Coefficient 59    |
| 6    | 0x06    | FIR Filter Bank A, Coefficient 60 to Coefficient 119 |
| 7    | 0x07    | FIR Filter Bank B, Coefficient 0 to Coefficient 59   |
| 8    | 0x08    | FIR Filter Bank B, Coefficient 60 to Coefficient 119 |
| 9    | 0x09    | FIR Filter Bank C, Coefficient 0 to Coefficient 59   |
| 10   | 0x0A    | FIR Filter Bank C, Coefficient 60 to Coefficient 119 |
| 11   | 0x0B    | FIR Filter Bank D, Coefficient 0 to Coefficient 59   |
| 12   | 0x0C    | FIR Filter Bank D, Coefficient 60 to Coefficient 119 |

**SPI COMMUNICATION**

The SPI port supports full duplex communication, as shown in Figure 17, which enables external processors to write to DIN while reading DOUT, when the previous command was a read request. Figure 17 provides a guideline for the bit coding on both DIN and DOUT.

**DEVICE CONFIGURATION**

The SPI provides write access to the control registers, one byte at a time, using the bit assignments shown in Figure 17. Each register has 16 bits, where Bits[7:0] represent the lower address (listed in Table 10) and Bits[15:8] represent the upper address. Write to the lower byte of a register first, followed by a write to its upper byte. The only register that changes with a single write to its lower byte is the PAGE\_ID register. For a write command, the first bit in the DIN sequence is set to 1. Address Bits[A6:A0] represent the target address, and Data Command Bits[DC7:DC0] represent the data being written to the location. Figure 13 provides an example of writing 0x03 to Address 0x00 (PAGE\_ID [7:0]), using DIN = 0x8003. This write command activates the control page for SPI access.

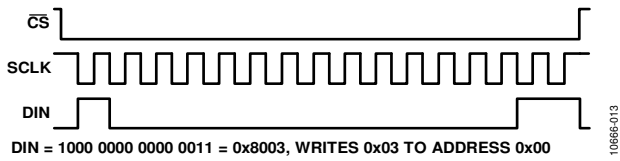


Figure 13. SPI Sequence for Activating the Control Page (DIN = 0x8003)

**Dual Memory Structure**

Writing configuration data to a control register updates its SRAM contents, which are volatile. After optimizing each relevant control register setting in a system, use the manual flash update command, which is located in GLOB\_CMD[3] on Page 3 of the register map. Activate the manual flash update command by turning to Page 3 (DIN = 0x8003) and setting GLOB\_CMD[3] = 1 (DIN = 0x8208, then DIN = 0x8300). Make sure that the power supply is within specification for the entire 375 ms processing time for a flash memory update. Table 10 provides a memory map for all of the user registers, which includes a column of flash backup information. A yes in this column indicates that a register has a mirror location in flash and, when backed up properly, automatically restores itself during startup or after a reset. Figure 14 provides a diagram of the dual memory structure used to manage operation and store critical user settings.

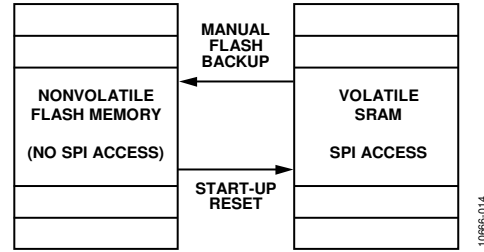


Figure 14. SRAM and Flash Memory Diagram

**READING SENSOR DATA**

The ADIS16485 automatically starts up and activates Page 0 for data register access. Write 0x00 to the PAGE\_ID register (DIN = 0x8000) to activate Page 0 for data access after accessing any other page. A single register read requires two 16-bit SPI cycles. The first cycle requests the contents of a register using the bit assignments in Figure 17, and then the register contents follow DOUT during the second sequence. The first bit in a DIN command is zero, followed by either the upper or the lower address for the register. The last eight bits are don't care, but the SPI requires the full set of 16 SCLKs to receive the request. Figure 15 includes two register reads in succession, which starts with DIN = 0x1A00 to request the contents of the Z\_GYRO\_OUT register and follows with 0x1800 to request the contents of the Z\_GYRO\_LOW register.



Figure 15. SPI Read Example

Figure 16 provides an example of the four SPI signals when reading PROD\_ID in a repeating pattern. This is a good pattern to use for troubleshooting the SPI interface setup and communications because the contents of PROD\_ID are predefined and stable.

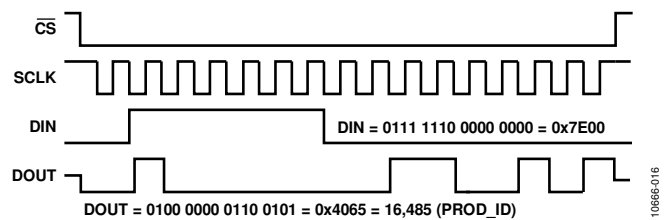
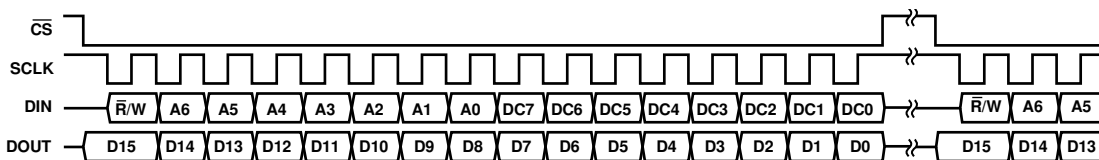


Figure 16. SPI Read Example, Second 16-Bit Sequence



**NOTES**

1. DOUT BITS ARE PRODUCED ONLY WHEN THE PREVIOUS 16-BIT DIN SEQUENCE STARTS WITH R/W = 0.
2. WHEN CS IS HIGH, DOUT IS IN A THREE-STATE, HIGH IMPEDANCE MODE, WHICH ALLOWS MULTIFUNCTIONAL USE OF THE LINE FOR OTHER DEVICES.

Figure 17. SPI Communication Bit Sequence

## USER REGISTERS

Table 10. User Register Memory Map (N/A Means Not Applicable)

| Name          | R/W | Flash | PAGE_ID | Address      | Default | Register Description                        | Format   |
|---------------|-----|-------|---------|--------------|---------|---|----------|
| PAGE_ID       | R/W | No    | 0x00    | 0x00         | 0x00    | Page identifier                             | N/A      |
| Reserved      | N/A | N/A   | 0x00    | 0x02 to 0x06 | N/A     | Reserved                                    | N/A      |
| SYS_E_FLAG    | R   | No    | 0x00    | 0x08         | 0x0000  | Output, system error flags                  | Table 41 |
| DIAG_STS      | R   | No    | 0x00    | 0x0A         | 0x0000  | Output, self test error flags               | Table 42 |
| ALM_STS       | R   | No    | 0x00    | 0x0C         | 0x0000  | Output, alarm error flags                   | Table 43 |
| TEMP_OUT      | R   | No    | 0x00    | 0x0E         | N/A     | Output, temperature                         | Table 39 |
| X_GYRO_LOW    | R   | No    | 0x00    | 0x10         | N/A     | Output, x-axis gyroscope, low word          | Table 15 |
| X_GYRO_OUT    | R   | No    | 0x00    | 0x12         | N/A     | Output, x-axis gyroscope, high word         | Table 11 |
| Y_GYRO_LOW    | R   | No    | 0x00    | 0x14         | N/A     | Output, y-axis gyroscope, low word          | Table 16 |
| Y_GYRO_OUT    | R   | No    | 0x00    | 0x16         | N/A     | Output, y-axis gyroscope, high word         | Table 12 |
| Z_GYRO_LOW    | R   | No    | 0x00    | 0x18         | N/A     | Output, z-axis gyroscope, low word          | Table 17 |
| Z_GYRO_OUT    | R   | No    | 0x00    | 0x1A         | N/A     | Output, z-axis gyroscope, high word         | Table 13 |
| X_ACCL_LOW    | R   | No    | 0x00    | 0x1C         | N/A     | Output, x-axis accelerometer, low word      | Table 22 |
| X_ACCL_OUT    | R   | No    | 0x00    | 0x1E         | N/A     | Output, x-axis accelerometer, high word     | Table 18 |
| Y_ACCL_LOW    | R   | No    | 0x00    | 0x20         | N/A     | Output, y-axis accelerometer, low word      | Table 23 |
| Y_ACCL_OUT    | R   | No    | 0x00    | 0x22         | N/A     | Output, y-axis accelerometer, high word     | Table 19 |
| Z_ACCL_LOW    | R   | No    | 0x00    | 0x24         | N/A     | Output, z-axis accelerometer, low word      | Table 24 |
| Z_ACCL_OUT    | R   | No    | 0x00    | 0x26         | N/A     | Output, z-axis accelerometer, high word     | Table 20 |
| Reserved      | N/A | N/A   | 0x00    | 0x28 to 0x3E | N/A     | Reserved                                    | N/A      |
| X_DELTANG_LOW | R   | No    | 0x00    | 0x40         | N/A     | Output, x-axis delta angle, low word        | Table 29 |
| X_DELTANG_OUT | R   | No    | 0x00    | 0x42         | N/A     | Output, x-axis delta angle, high word       | Table 25 |
| Y_DELTANG_LOW | R   | No    | 0x00    | 0x44         | N/A     | Output, y-axis delta angle, low word        | Table 30 |
| Y_DELTANG_OUT | R   | No    | 0x00    | 0x46         | N/A     | Output, y-axis delta angle, high word       | Table 26 |
| Z_DELTANG_LOW | R   | No    | 0x00    | 0x48         | N/A     | Output, z-axis delta angle, low word        | Table 31 |
| Z_DELTANG_OUT | R   | No    | 0x00    | 0x4A         | N/A     | Output, z-axis delta angle, high word       | Table 27 |
| X_DELTVEL_LOW | R   | No    | 0x00    | 0x4C         | N/A     | Output, x-axis delta velocity, low word     | Table 36 |
| X_DELTVEL_OUT | R   | No    | 0x00    | 0x4E         | N/A     | Output, x-axis delta velocity, high word    | Table 32 |
| Y_DELTVEL_LOW | R   | No    | 0x00    | 0x50         | N/A     | Output, y-axis delta velocity, low word     | Table 37 |
| Y_DELTVEL_OUT | R   | No    | 0x00    | 0x52         | N/A     | Output, y-axis delta velocity, high word    | Table 33 |
| Z_DELTVEL_LOW | R   | No    | 0x00    | 0x54         | N/A     | Output, z-axis delta velocity, low word     | Table 38 |
| Z_DELTVEL_OUT | R   | No    | 0x00    | 0x56         | N/A     | Output, z-axis delta velocity, high word    | Table 34 |
| Reserved      | N/A | N/A   | 0x00    | 0x58 to 0x76 | N/A     | Reserved                                    | N/A      |
| TIME_MS_OUT   | R   | Yes   | 0x00    | 0x78         | N/A     | Factory configuration time: minutes/seconds | Table 96 |
| TIME_DH_OUT   | R   | Yes   | 0x00    | 0x7A         | N/A     | Factory configuration date/time: day/hour   | Table 97 |
| TIME_YM_OUT   | R   | Yes   | 0x00    | 0x7C         | N/A     | Factory configuration date: year/month      | Table 98 |
| PROD_ID       | R   | Yes   | 0x00    | 0x7E         | 0x4065  | Output, product identification (16,485)     | Table 47 |
| Reserved      | N/A | N/A   | 0x01    | 0x00 to 0x7E | N/A     | Reserved                                    | N/A      |
| PAGE_ID       | R/W | No    | 0x02    | 0x00         | 0x00    | Page identifier                             | N/A      |
| Reserved      | N/A | N/A   | 0x02    | 0x02         | N/A     | Reserved                                    | N/A      |
| X_GYRO_SCALE  | R/W | Yes   | 0x02    | 0x04         | 0x0000  | Calibration, scale, x-axis gyroscope        | Table 64 |
| Y_GYRO_SCALE  | R/W | Yes   | 0x02    | 0x06         | 0x0000  | Calibration, scale, y-axis gyroscope        | Table 65 |
| Z_GYRO_SCALE  | R/W | Yes   | 0x02    | 0x08         | 0x0000  | Calibration, scale, z-axis gyroscope        | Table 66 |
| X_ACCL_SCALE  | R/W | Yes   | 0x02    | 0x0A         | 0x0000  | Calibration, scale, x-axis accelerometer    | Table 74 |
| Y_ACCL_SCALE  | R/W | Yes   | 0x02    | 0x0C         | 0x0000  | Calibration, scale, y-axis accelerometer    | Table 75 |
| Z_ACCL_SCALE  | R/W | Yes   | 0x02    | 0x0E         | 0x0000  | Calibration, scale, z-axis accelerometer    | Table 76 |

| Name         | R/W | Flash | PAGE_ID | Address      | Default             | Register Description                                  | Format   |
|--------------|-----|-------|---------|--------------|---------------------|---|----------|
| XG_BIAS_LOW  | R/W | Yes   | 0x02    | 0x10         | 0x0000              | Calibration, offset, gyroscope, x-axis, low word      | Table 60 |
| XG_BIAS_HIGH | R/W | Yes   | 0x02    | 0x12         | 0x0000              | Calibration, offset, gyroscope, x-axis, high word     | Table 57 |
| YG_BIAS_LOW  | R/W | Yes   | 0x02    | 0x14         | 0x0000              | Calibration, offset, gyroscope, y-axis, low word      | Table 61 |
| YG_BIAS_HIGH | R/W | Yes   | 0x02    | 0x16         | 0x0000              | Calibration, offset, gyroscope, y-axis, high word     | Table 58 |
| ZG_BIAS_LOW  | R/W | Yes   | 0x02    | 0x18         | 0x0000              | Calibration, offset, gyroscope, z-axis, low word      | Table 62 |
| ZG_BIAS_HIGH | R/W | Yes   | 0x02    | 0x1A         | 0x0000              | Calibration, offset, gyroscope, z-axis, high word     | Table 59 |
| XA_BIAS_LOW  | R/W | Yes   | 0x02    | 0x1C         | 0x0000              | Calibration, offset, accelerometer, x-axis, low word  | Table 71 |
| XA_BIAS_HIGH | R/W | Yes   | 0x02    | 0x1E         | 0x0000              | Calibration, offset, accelerometer, x-axis, high word | Table 68 |
| YA_BIAS_LOW  | R/W | Yes   | 0x02    | 0x20         | 0x0000              | Calibration, offset, accelerometer, y-axis, low word  | Table 72 |
| YA_BIAS_HIGH | R/W | Yes   | 0x02    | 0x22         | 0x0000              | Calibration, offset, accelerometer, y-axis, high word | Table 69 |
| ZA_BIAS_LOW  | R/W | Yes   | 0x02    | 0x24         | 0x0000              | Calibration, offset, accelerometer, z-axis, low word  | Table 73 |
| ZA_BIAS_HIGH | R/W | Yes   | 0x02    | 0x26         | 0x0000              | Calibration, offset, accelerometer, z-axis, high word | Table 70 |
| Reserved     | N/A | N/A   | 0x02    | 0x28 to 0x72 | N/A                 | Reserved  | N/A      |
| USER_SCR_1   | R/W | Yes   | 0x02    | 0x74         | 0x0000              | User Scratch Register 1                               | Table 92 |
| USER_SCR_2   | R/W | Yes   | 0x02    | 0x76         | 0x0000              | User Scratch Register 2                               | Table 93 |
| USER_SCR_3   | R/W | Yes   | 0x02    | 0x78         | 0x0000              | User Scratch Register 3                               | Table 94 |
| USER_SCR_4   | R/W | Yes   | 0x02    | 0x7A         | 0x0000              | User Scratch Register 4                               | Table 95 |
| FLSHCNT_LOW  | R   | Yes   | 0x02    | 0x7C         | N/A                 | Diagnostic, flash memory count, low word              | Table 87 |
| FLSHCNT_HIGH | R   | Yes   | 0x02    | 0x7E         | N/A                 | Diagnostic, flash memory count, high word             | Table 88 |
| PAGE_ID      | R/W | No    | 0x03    | 0x00         | 0x0000              | Page identifier                                       | N/A      |
| GLOB_CMD     | W   | No    | 0x03    | 0x02         | N/A                 | Control, global commands                              | Table 86 |
| Reserved     | N/A | N/A   | 0x03    | 0x04         | N/A                 | Reserved  | N/A      |
| FNCTIO_CTRL  | R/W | Yes   | 0x03    | 0x06         | 0x000D              | Control, I/O pins, functional definitions             | Table 89 |
| GPIO_CTRL    | R/W | Yes   | 0x03    | 0x08         | 0x00X0 <sup>1</sup> | Control, I/O pins, general purpose                    | Table 90 |
| CONFIG       | R/W | Yes   | 0x03    | 0x0A         | 0x00C0              | Control, clock, and miscellaneous correction          | Table 67 |
| DEC_RATE     | R/W | Yes   | 0x03    | 0x0C         | 0x0000              | Control, output sample rate decimation                | Table 49 |
| NULL_CNFG    | R/W | Yes   | 0x03    | 0x0E         | 0x070A              | Control, automatic bias correction configuration      | Table 63 |
| SLP_CNT      | R/W | No    | 0x03    | 0x10         | N/A                 | Control, power-down/sleep mode                        | Table 91 |
| Reserved     | N/A | N/A   | 0x03    | 0x12 to 0x14 | N/A                 | Reserved  | N/A      |
| FILTR_BNK_0  | R/W | Yes   | 0x03    | 0x16         | 0x0000              | Filter selection                                      | Table 50 |
| FILTR_BNK_1  | R/W | Yes   | 0x03    | 0x18         | 0x0000              | Filter selection                                      | Table 51 |
| Reserved     | N/A | N/A   | 0x03    | 0x1A to 0x1E | N/A                 | Reserved  | N/A      |
| ALM_CNFG_0   | R/W | Yes   | 0x03    | 0x20         | 0x0000              | Alarm configuration                                   | Table 83 |
| ALM_CNFG_1   | R/W | Yes   | 0x03    | 0x22         | 0x0000              | Alarm configuration                                   | Table 84 |
| Reserved     | N/A | N/A   | 0x03    | 0x24 to 0x26 | N/A                 | Reserved  | N/A      |
| XG_ALM_MAGN  | R/W | Yes   | 0x03    | 0x28         | 0x0000              | Alarm, x-axis gyroscope threshold setting             | Table 77 |
| YG_ALM_MAGN  | R/W | Yes   | 0x03    | 0x2A         | 0x0000              | Alarm, y-axis gyroscope threshold setting             | Table 78 |
| ZG_ALM_MAGN  | R/W | Yes   | 0x03    | 0x2C         | 0x0000              | Alarm, z-axis gyroscope threshold setting             | Table 79 |
| XA_ALM_MAGN  | R/W | Yes   | 0x03    | 0x2E         | 0x0000              | Alarm, x-axis accelerometer threshold                 | Table 80 |
| YA_ALM_MAGN  | R/W | Yes   | 0x03    | 0x30         | 0x0000              | Alarm, y-axis accelerometer threshold                 | Table 81 |
| ZA_ALM_MAGN  | R/W | Yes   | 0x03    | 0x32         | 0x0000              | Alarm, z-axis accelerometer threshold                 | Table 82 |
| Reserved     | N/A | N/A   | 0x03    | 0x34 to 0x76 | N/A                 | Reserved  | N/A      |
| FIRM_REV     | R   | Yes   | 0x03    | 0x78         | N/A                 | Firmware revision                                     | Table 44 |
| FIRM_DM      | R   | Yes   | 0x03    | 0x7A         | N/A                 | Firmware programming date: day/month                  | Table 45 |
| FIRM_Y       | R   | Yes   | 0x03    | 0x7C         | N/A                 | Firmware programming date: year                       | Table 46 |
| Reserved     | N/A | N/A   | 0x03    | 0x7E         | N/A                 | Reserved  | N/A      |
| Reserved     | N/A | N/A   | 0x04    | 0x00 to 0x18 | N/A                 | Reserved  | N/A      |
| SERIAL_NUM   | R   | Yes   | 0x04    | 0x20         | N/A                 | Serial number   | Table 48 |
| Reserved     | N/A | N/A   | 0x04    | 0x22 to 0x7F | N/A                 | Reserved  | N/A      |

| Name          | R/W | Flash | PAGE_ID | Address      | Default | Register Description                           | Format   |
|---------------|-----|-------|---------|--------------|---------|--|----------|
| PAGE_ID       | R/W | No    | 0x05    | 0x00         | 0x0000  | Page identifier                                | N/A      |
| FIR_COEF_Axxx | R/W | Yes   | 0x05    | 0x02 to 0x7E | N/A     | FIR Filter Bank A, Coefficients 0 through 119  | Table 52 |
| PAGE_ID       | R/W | No    | 0x06    | 0x00         | 0x0000  | Page identifier                                | N/A      |
| FIR_COEF_Axxx | R/W | Yes   | 0x06    | 0x02 to 0x7E | N/A     | FIR Filter Bank A, Coefficients 60 through 119 | Table 52 |
| PAGE_ID       | R/W | No    | 0x07    | 0x00         | 0x0000  | Page identifier                                | N/A      |
| FIR_COEF_Bxxx | R/W | Yes   | 0x07    | 0x02 to 0x7E | N/A     | FIR Filter Bank B, Coefficients 0 through 119  | Table 53 |
| PAGE_ID       | R/W | No    | 0x08    | 0x00         | 0x0000  | Page identifier                                | N/A      |
| FIR_COEF_Bxxx | R/W | Yes   | 0x08    | 0x02 to 0x7E | N/A     | FIR Filter Bank B, Coefficients 60 through 119 | Table 53 |
| PAGE_ID       | R/W | No    | 0x09    | 0x00         | 0x0000  | Page identifier                                | N/A      |
| FIR_COEF_Cxxx | R/W | Yes   | 0x09    | 0x02 to 0x7E | N/A     | FIR Filter Bank C, Coefficients 0 through 119  | Table 54 |
| PAGE_ID       | R/W | No    | 0x0A    | 0x00         | 0x0000  | Page identifier                                | N/A      |
| FIR_COEF_Cxxx | R/W | Yes   | 0x0A    | 0x02 to 0x7E | N/A     | FIR Filter Bank C, Coefficients 60 through 119 | Table 54 |
| PAGE_ID       | R/W | No    | 0x0B    | 0x00         | 0x0000  | Page identifier                                | N/A      |
| FIR_COEF_Dxxx | R/W | Yes   | 0x0B    | 0x02 to 0x7E | N/A     | FIR Filter Bank D, Coefficients 0 through 119  | Table 55 |
| PAGE_ID       | R/W | No    | 0x0C    | 0x00         | 0x0000  | Page identifier                                | N/A      |
| FIR_COEF_Dxxx | R/W | Yes   | 0x0C    | 0x02 to 0x7E | N/A     | FIR Filter Bank D, Coefficients 60 through 119 | Table 55 |

<sup>1</sup> The GPIO\_CTRL[7:4] bits reflect the logic levels on the DIOx lines and do not have a default setting.

## OUTPUT DATA REGISTERS

After the ADIS16485 completes its start-up process, the PAGE\_ID register contains 0x0000, which sets Page 0 as the active page for SPI access. Page 0 contains the output data, real-time clock, status, and product identification registers.

### INERTIAL SENSOR DATA FORMAT

The gyroscope, accelerometer, delta angle, and delta velocity output data registers use a 32-bit, twos complement format. Each output uses two registers to support this resolution. Figure 18 provides an example of how each register contributes to each inertial measurement. In this case, X\_GYRO\_OUT is the most significant word (upper 16 bits), and X\_GYRO\_LOW is the least significant word (lower 16 bits). In many cases, using the most significant word registers alone provide sufficient resolution for preserving key performance metrics.

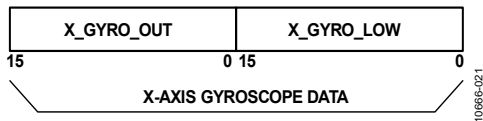


Figure 18. Gyroscope Output Format Example, DEC\_RATE > 0

The arrows in Figure 19 describe the direction of the motion, which produces a positive output response in each output register of the sensor. The accelerometers respond to both dynamic and static forces associated with acceleration, including gravity. When lying perfectly flat, as shown in Figure 19, the z-axis accelerometer output is 1 g, and the x and y accelerometers are 0 g.

### ROTATION RATE (GYROSCOPE)

The registers that use the x\_GYRO\_OUT format are the primary registers for the gyroscope measurements (see Table 11, Table 12, and Table 13). When processing data from these registers, use a 16-bit, twos complement data format. Table 14 provides x\_GYRO\_OUT digital coding examples.

Table 11. X\_GYRO\_OUT (Page 0, Base Address = 0x12)

| Bits   | Description   |
|--------|---|
| [15:0] | X-axis gyroscope data; twos complement, $\pm 450^\circ/\text{sec}$ range, $0^\circ/\text{sec} = 0x0000$ , 1 LSB = $0.02^\circ/\text{sec}$ |

Table 12. Y\_GYRO\_OUT (Page 0, Base Address = 0x16)

| Bits   | Description   |
|--------|---|
| [15:0] | Y-axis gyroscope data; twos complement, $\pm 450^\circ/\text{sec}$ range, $0^\circ/\text{sec} = 0x0000$ , 1 LSB = $0.02^\circ/\text{sec}$ |

Table 13. Z\_GYRO\_OUT (Page 0, Base Address = 0x1A)

| Bits   | Description   |
|--------|---|
| [15:0] | Z-axis gyroscope data; twos complement, $\pm 450^\circ/\text{sec}$ range, $0^\circ/\text{sec} = 0x0000$ , 1 LSB = $0.02^\circ/\text{sec}$ |

Table 14. X\_GYRO\_OUT Data Format Examples

| Rotation Rate | Decimal | Hex    | Binary              |
|---------------|---------|--------|---------------------|
| +450°/sec     | +22,500 | 0x57E4 | 0101 0111 1110 0100 |
| +0.04°/sec    | +2      | 0x0002 | 0000 0000 0000 0010 |
| +0.02°/sec    | +1      | 0x0001 | 0000 0000 0000 0001 |
| 0°/sec        | 0       | 0x0000 | 0000 0000 0000 0000 |
| -0.02°/sec    | -1      | 0xFFFF | 1111 1111 1111 1111 |
| -0.04°/sec    | -2      | 0xFFFE | 1111 1111 1111 1110 |
| -450°/sec     | -22,500 | 0xA81C | 1010 1000 0001 1100 |

The registers that use the x\_GYRO\_LOW naming format provide additional resolution for the gyroscope measurements (see Table 15, Table 16, and Table 17). The MSB has a weight of  $0.01^\circ/\text{sec}$ , and each subsequent bit has  $\frac{1}{2}$  the weight of the previous one.

Table 15. X\_GYRO\_LOW (Page 0, Base Address = 0x10)

| Bits   | Description                                       |
|--------|---|
| [15:0] | X-axis gyroscope data; additional resolution bits |

Table 16. Y\_GYRO\_LOW (Page 0, Base Address = 0x14)

| Bits   | Description                                       |
|--------|---|
| [15:0] | Y-axis gyroscope data; additional resolution bits |

Table 17. Z\_GYRO\_LOW (Page 0, Base Address = 0x18)

| Bits   | Description                                       |
|--------|---|
| [15:0] | Z-axis gyroscope data; additional resolution bits |

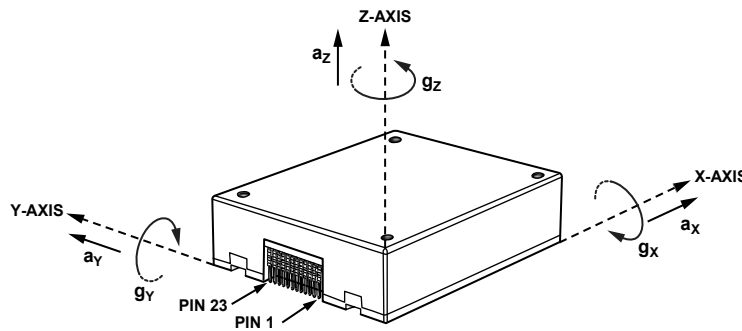


Figure 19. Inertial Sensor Direction Reference Diagram



**ACCELERATION**

The registers that use the x\_ACCL\_OUT format are the primary registers for the accelerometer measurements (see Table 18, Table 19, and Table 20). When processing data from these registers, use a 16-bit, twos complement data format. Table 21 provides x\_ACCL\_OUT digital coding examples.

**Table 18. X\_ACCL\_OUT (Page 0, Base Address = 0x1E)**

| Bits   | Description   |
|--------|---|
| [15:0] | X-axis accelerometer data; twos complement, ±5 g range, 0 g = 0x0000, 1 LSB = 0.25 mg |

**Table 19. Y\_ACCL\_OUT (Page 0, Base Address = 0x22)**

| Bits   | Description   |
|--------|---|
| [15:0] | Y-axis accelerometer data; twos complement, ±5 g range, 0 g = 0x0000, 1 LSB = 0.25 mg |

**Table 20. Z\_ACCL\_OUT (Page 0, Base Address = 0x26)**

| Bits   | Description   |
|--------|---|
| [15:0] | Z-axis accelerometer data; twos complement, ±5 g range, 0 g = 0x0000, 1 LSB = 0.25 mg |

**Table 21. x\_ACCL\_OUT Data Format Examples**

| Acceleration | Decimal | Hex    | Binary              |
|--------------|---------|--------|---------------------|
| +5 g         | +20,000 | 0x4E20 | 0100 1110 0010 0000 |
| +0.5 mg      | +2      | 0x0002 | 0000 0000 0000 0010 |
| +0.25 mg     | +1      | 0x0001 | 0000 0000 0000 0001 |
| 0 mg         | 0       | 0x0000 | 0000 0000 0000 0000 |
| -0.25 mg     | -1      | 0xFFFF | 1111 1111 1111 1111 |
| -0.5 mg      | -2      | 0xFFFE | 1111 1111 1111 1110 |
| -5 g         | -20,000 | 0xB1E0 | 1011 0001 1110 0000 |

The registers that use the x\_ACCL\_LOW naming format provide additional resolution for the accelerometer measurements (see Table 22, Table 23, and Table 24). The MSB has a weight of 0.125 mg, and each subsequent bit has ½ the weight of the previous one.

**Table 22. X\_ACCL\_LOW (Page 0, Base Address = 0x1C)**

| Bits   | Description   |
|--------|---|
| [15:0] | X-axis accelerometer data; additional resolution bits |

**Table 23. Y\_ACCL\_LOW (Page 0, Base Address = 0x20)**

| Bits   | Description   |
|--------|---|
| [15:0] | Y-axis accelerometer data; additional resolution bits |

**Table 24. Z\_ACCL\_LOW (Page 0, Base Address = 0x24)**

| Bits   | Description   |
|--------|---|
| [15:0] | Z-axis accelerometer data; additional resolution bits |

**DELTA ANGLES**

The x\_DELTANG\_OUT registers are the primary output registers for the delta angle calculations. When processing data from these registers, use a 16-bit, twos complement data format (see Table 25, Table 26, and Table 27). Table 28 shows x\_DELTANG\_OUT digital coding examples.

The delta angle outputs represent an integration of the gyroscope measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta\theta_{x,nD} = \frac{1}{2f_s} \times \sum_{d=0}^{D-1} (\omega_{x,nD+d} + \omega_{x,nD+d-1})$$

where:

D is the decimation rate = DEC\_RATE + 1.

f<sub>s</sub> is the sample rate.

d is the incremental variable in the summation formula.

ω<sub>x</sub> is the x-axis rate of rotation (gyroscope).

n is the sample time, prior to the decimation filter.

When using the internal sample clock, f<sub>s</sub> is equal to 2460 SPS. When using the external clock option, f<sub>s</sub> is equal to the frequency of the external clock, which is limited to a minimum of 2 kHz, to prevent overflow in the x\_DELTANG\_xxx registers at high rotation rates. See Table 49 and Figure 20 for more information on the DEC\_RATE register (decimation filter).

The x\_DELTANG\_LOW registers (see Table 29, Table 30, and Table 31) provide additional resolution bits for the delta angle and combine with the x\_DELTANG\_OUT registers to provide a 32-bit, twos complement number. The MSB in the x\_DELTANG\_LOW registers have a weight of ~0.011° (720°/216), and each subsequent bit carries a weight of ½ of the previous one.

**Table 25. X\_DELTANG\_OUT (Page 0, Base Address = 0x42)**

| Bits   | Description  |
|--------|--|
| [15:0] | X-axis delta angle data; twos complement, ±720° range, 0° = 0x0000, 1 LSB = 720°/2 <sup>15</sup> = ~0.022° |

**Table 26. Y\_DELTANG\_OUT (Page 0, Base Address = 0x46)**

| Bits   | Description  |
|--------|--|
| [15:0] | Y-axis delta angle data; twos complement, ±720° range, 0° = 0x0000, 1 LSB = 720°/2 <sup>15</sup> = ~0.022° |

**Table 27. Z\_DELTANG\_OUT (Page 0, Base Address = 0x4A)**

| Bits   | Description  |
|--------|--|
| [15:0] | Z-axis delta angle data; twos complement, ±720° range, 0° = 0x0000, 1 LSB = 720°/2 <sup>15</sup> = ~0.022° |

**Table 28. x\_DELTANG\_OUT Data Format Examples**

| Angle (°)                                    | Decimal | Hex    | Binary              |
|--|---------|--------|---------------------|
| +720 × (2 <sup>15</sup> - 1)/2 <sup>15</sup> | +32,767 | 0x7FFF | 0111 1111 1111 1111 |
| +1440/2 <sup>15</sup>                        | +2      | 0x0002 | 0000 0000 0000 0010 |
| +720/2 <sup>15</sup>                         | +1      | 0x0001 | 0000 0000 0000 0001 |
| 0  | 0       | 0x0000 | 0000 0000 0000 0000 |
| -720/2 <sup>15</sup>                         | -1      | 0xFFFF | 1111 1111 1111 1111 |
| -1440/2 <sup>15</sup>                        | -2      | 0xFFFE | 1111 1111 1111 1110 |
| -720   | -32,768 | 0x8000 | 1000 0000 0000 0000 |

The x\_DELTANG\_LOW registers (see Table 29, Table 30, and Table 31) provide additional resolution for the angle measurement and combine with the x\_DELTANT\_OUT registers to provide a 32-bit, twos complement number. The MSBs in the x\_DELTANG\_LOW registers have a weight of ~0.011° (720°/2<sup>16</sup>), and each subsequent bit carries a weight of ½ of the previous one.

**Table 29. X\_DELTANG\_LOW (Page 0, Base Address = 0x40)**

| Bits   | Description   |
|--------|---|
| [15:0] | X-axis delta angle data; additional resolution bits |

**Table 30. Y\_DELTANG\_LOW (Page 0, Base Address = 0x44)**

| Bits   | Description   |
|--------|---|
| [15:0] | Y-axis delta angle data; additional resolution bits |

**Table 31. Z\_DELTANG\_LOW (Page 0, Base Address = 0x48)**

| Bits   | Description   |
|--------|---|
| [15:0] | Z-axis delta angle data; additional resolution bits |

**DELTA VELOCITY**

The registers that use the x\_DELTVEL\_OUT format are the primary registers for the delta velocity calculations. When processing data from these registers, use a 16-bit, twos complement data format (see Table 32, Table 33, and Table 34). Table 35 provides x\_DELTVEL\_OUT digital coding examples.

The delta velocity outputs represent an integration of the accelerometer measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta V_{x,nD} = \frac{1}{2f_s} \times \sum_{d=0}^{D-1} (a_{x,nD+d} + a_{x,nD+d-1})$$

where:

$a_x$  is the x-axis linear acceleration.

$f_s$  is the sample rate.

$n$  is the sample time, prior to the decimation filter.

$D$  is the decimation rate = DEC\_RATE + 1.

$d$  is the incremental variable in the summation formula.

When using the internal sample clock,  $f_s$  is equal to 2460 SPS. When using the external clock option,  $f_s$  is equal to the frequency of the external clock, which is limited to a minimum of 2 kHz, to prevent overflow in the x\_DELTVEL\_xxx registers at high rotation rates. See Table 49 and Figure 20 for more information on the DEC\_RATE register (decimation filter).

**Table 32. X\_DELTVEL\_OUT (Page 0, Base Address = 0x4E)**

| Bits   | Description   |
|--------|---|
| [15:0] | X-axis delta velocity data; twos complement, $\pm 50$ m/sec range, 0 m/sec = 0x0000, 1 LSB = 50 m/sec $\div$ ( $2^{15} - 1$ ) = $\sim 1.526$ mm/sec |

**Table 33. Y\_DELTVEL\_OUT (Page 0, Base Address = 0x52)**

| Bits   | Description   |
|--------|---|
| [15:0] | Y-axis delta velocity data; twos complement, $\pm 50$ m/sec range, 0 m/sec = 0x0000, 1 LSB = 50 m/sec $\div$ ( $2^{15} - 1$ ) = $\sim 1.526$ mm/sec |

**Table 34. Z\_DELTVEL\_OUT (Page 0, Base Address = 0x56)**

| Bits   | Description   |
|--------|---|
| [15:0] | Z-axis delta velocity data; twos complement, $\pm 50$ m/sec range, 0 m/sec = 0x0000, 1 LSB = 50 m/sec $\div$ ( $2^{15} - 1$ ) = $\sim 1.526$ mm/sec |

**Table 35. x\_DELTVEL\_OUT, Data Format Examples**

| Velocity (m/sec)                   | Decimal | Hex    | Binary              |
|------------------------------------|---------|--------|---------------------|
| $+50 \times (2^{15} - 1) / 2^{15}$ | +32,767 | 0x7FFF | 0111 1111 1111 1111 |
| $+100 / 2^{15}$                    | +2      | 0x0002 | 0000 0000 0000 0010 |
| $+50 / 2^{15}$                     | +1      | 0x0001 | 0000 0000 0000 0001 |
| 0                                  | 0       | 0x0000 | 0000 0000 0000 0000 |
| $-50 / 2^{15}$                     | -1      | 0xFFFF | 1111 1111 1111 1111 |
| $-100 / 2^{15}$                    | -2      | 0xFFFE | 1111 1111 1111 1110 |
| -50                                | -32,768 | 0x8000 | 1000 0000 0000 0000 |

The x\_DELTVEL\_LOW registers (see Table 36, Table 37, and Table 38) provide additional resolution bits for the delta-velocity measurement and combine with the x\_DELTVEL\_OUT registers to provide a 32-bit, twos complement number. The MSBs in the x\_DELTVEL\_LOW registers have a weight of  $\sim 0.7629$  mm/sec (50 m/sec  $\div$   $2^{16}$ ), and each subsequent bit carries a weight of  $1/2$  of the previous one.

**Table 36. X\_DELTVEL\_LOW (Page 0, Base Address = 0x4C)**

| Bits   | Description  |
|--------|--|
| [15:0] | X-axis delta velocity data; additional resolution bits |

**Table 37. Y\_DELTVEL\_LOW (Page 0, Base Address = 0x50)**

| Bits   | Description  |
|--------|--|
| [15:0] | Y-axis delta velocity data; additional resolution bits |

**Table 38. Z\_DELTVEL\_LOW (Page 0, Base Address = 0x54)**

| Bits   | Description  |
|--------|--|
| [15:0] | Z-axis delta velocity data; additional resolution bits |

**INTERNAL TEMPERATURE**

The TEMP\_OUT register provides an internal temperature measurement that can be useful for observing relative temperature changes inside of the ADIS16485 (see Table 39). Table 40 provides TEMP\_OUT digital coding examples. Note that this temperature reflects a higher temperature than ambient, due to self heating.

**Table 39. TEMP\_OUT (Page 0, Base Address = 0x0E)**

| Bits   | Description   |
|--------|---|
| [15:0] | Temperature data; twos complement, 0.00565°C per LSB, 25°C = 0x0000 |

**Table 40. TEMP\_OUT Data Format Examples**

| Temperature (°C) | Decimal | Hex    | Binary              |
|------------------|---------|--------|---------------------|
| +85              | +10,619 | 0x297B | 0010 1001 0111 1011 |
| +25 + 0.0113     | +2      | 0x0002 | 0000 0000 0000 0010 |
| +25 + 0.00565    | +1      | 0x0001 | 0000 0000 0000 0001 |
| +25              | 0       | 0x0000 | 0000 0000 0000 0000 |
| +25 - 0.00565    | -1      | 0xFFFF | 1111 1111 1111 1111 |

| Temperature (°C) | Decimal | Hex    | Binary              |
|------------------|---------|--------|---------------------|
| +25 – 0.0113     | –2      | 0xFFFE | 1111 1111 1111 1110 |
| –40              | –11,504 | 0xD310 | 1101 0011 0001 0000 |

### STATUS/ALARM INDICATORS

The SYS\_E\_FLAG register in Table 41 provides the system error flags for a variety of conditions (see Table 41). Reading the SYS\_E\_FLAG register clears all of its error flags and returns each bit to a zero value, with the exception of Bit[7]. If SYS\_E\_FLAG[7] is high, use the software reset (GLOB\_CMD[7], see Table 86) to clear this condition and restore normal operation. If any bit in the SYS\_E\_FLAG register is associated with an error condition that remains after reading this register, this bit automatically returns to an alarm value as 1.

**Table 41. SYS\_E\_FLAG (Page 0, Base Address = 0x08)**

| Bits   | Description (Default = 0x0000)   |
|--------|--|
| 15     | Watch dog timer flag (1 = timed out)   |
| [14:8] | Not used   |
| 7      | Processing overrun (1 = error)   |
| 6      | Flash memory update, result of GLOB_CMD[3] = 1 (1 = failed update, 0 = update successful)                      |
| 5      | Inertial self test failure (1 = DIAG_STS ≠ 0x0000)   |
| 4      | Sensor overrange (1 = at least one sensor overranged)  |
| 3      | SPI communication error (1 = error condition, when the number of SCLK pulses is not equal to a multiple of 16) |
| [2:1]  | Not used   |
| 0      | Alarm status flag (1 = ALM_STS ≠ 0x0000)   |

The DIAG\_STS register in Table 42 provides the flags for the internal self test function, which is from GLOB\_CMD[1] (see Table 86). Note that reading DIAG\_STS also resets it to 0x0000.

**Table 42. DIAG\_STS (Page 0, Base Address = 0x0A)**

| Bits   | Description (Default = 0x0000)                        |
|--------|---|
| [15:6] | Not used  |
| 5      | Self test failure, z-axis accelerometer (1 = failure) |
| 4      | Self test failure, y-axis accelerometer (1 = failure) |
| 3      | Self test failure, x-axis accelerometer (1 = failure) |
| 2      | Self test failure, z-axis gyroscope (1 = failure)     |
| 1      | Self test failure, y-axis gyroscope (1 = failure)     |
| 0      | Self test failure, x-axis gyroscope (1 = failure)     |

The ALM\_STS register in Table 43 provides the alarm bits for the programmable alarm levels of each sensor. Note that reading ALM\_STS also resets its value to 0x0000.

**Table 43. ALM\_STS (Page 0, Base Address = 0x0C)**

| Bits   | Description (Default = 0x0000)                        |
|--------|---|
| [15:6] | Not used  |
| 5      | Z-axis accelerometer alarm flag (1 = alarm is active) |
| 4      | Y-axis accelerometer alarm flag (1 = alarm is active) |
| 3      | X-axis accelerometer alarm flag (1 = alarm is active) |
| 2      | Z-axis gyroscope alarm flag (1 = alarm is active)     |

| Bits | Description (Default = 0x0000)                    |
|------|---|
| 1    | Y-axis gyroscope alarm flag (1 = alarm is active) |
| 0    | X-axis gyroscope alarm flag (1 = alarm is active) |

### FIRMWARE REVISION

The FIRM\_REV register (see Table 44) provides the firmware revision for the internal processor. Each nibble represents a digit in this revision code. For example, if FIRM\_REV = 0x0102, the firmware revision is 1.02.

**Table 44. FIRM\_REV (Page 3, Base Address = 0x78)**

| Bits    | Description                        |
|---------|------------------------------------|
| [15:12] | Binary, revision, 10s digit        |
| [11:8]  | Binary, revision, 1s digit         |
| [7:4]   | Binary, revision, tenths digit     |
| [3:0]   | Binary, revision, hundredths digit |

The FIRM\_DM register (see Table 45) contains the month and day of the factory configuration date. FIRM\_DM[15:12] and FIRM\_DM[11:8] contain digits that represent the month of factory configuration. For example, November is the 11<sup>th</sup> month in a year and represented by FIRM\_DM[15:8] = 0x11. FIRM\_DM[7:4] and FIRM\_DM[3:0] contain digits that represent the day of factory configuration. For example, the 27<sup>th</sup> day of the month is represented by FIRM\_DM[7:0] = 0x27.

**Table 45. FIRM\_DM (Page 3, Base Address = 0x7A)**

| Bits    | Description                            |
|---------|--|
| [15:12] | Binary, month 10s digit, range: 0 to 1 |
| [11:8]  | Binary, month 1s digit, range: 0 to 9  |
| [7:4]   | Binary, day 10s digit, range: 0 to 3   |
| [3:0]   | Binary, day 1s digit, range: 0 to 9    |

The FIRM\_Y register (see Table 46) contains the year of the factory configuration date. For example, the year of 2013 is represented by FIRM\_Y = 0x2013.

**Table 46. FIRM\_Y (Page 3, Base Address = 0x7C)**

| Bits    | Description                             |
|---------|---|
| [15:12] | Binary, year 1000s digit, range: 0 to 9 |
| [11:8]  | Binary, year 100s digit, range: 0 to 9  |
| [7:4]   | Binary, year 10s digit, range: 0 to 9   |
| [3:0]   | Binary, year 1s digit, range: 0 to 9    |

### PRODUCT IDENTIFICATION

The PROD\_ID register (see Table 47) contains the binary equivalent of the device number (16,485 = 0x4065), and the SERIAL\_NUM register (see Table 48) contains a lot-specific serial number.

**Table 47. PROD\_ID (Page 0, Base Address = 0x7E)**

| Bits   | Description (Default = 0x4065)           |
|--------|--|
| [15:0] | Product identification = 0x4065 (16,485) |

**Table 48. SERIAL\_NUM (Page 4, Base Address = 0x20)**

| Bits   | Description                |
|--------|----------------------------|
| [15:0] | Lot specific serial number |

## DIGITAL SIGNAL PROCESSING GYROSCOPES/ACCELEROMETERS

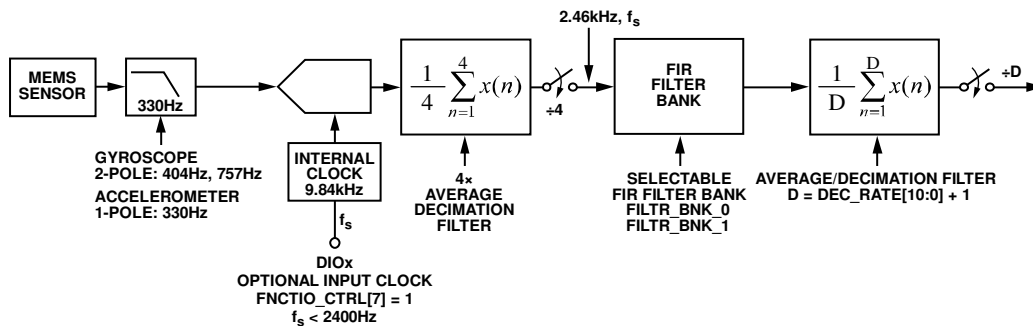
Figure 20 provides a signal flow diagram for all the components and settings that influence the frequency response for the accelerometers and gyroscopes. The sample rate for each accelerometer and gyroscope is 9.84 kHz. Each sensor has its own averaging/decimation filter stage that reduces the update rate to 2.46 kSPS. When using the external sync clock option (FNCTIO\_CTRL[7:4], see Table 89), the input clock drives a 4-sample burst at a sample rate of 9.84 kSPS, which feeds into the 4× averaging/decimation filter. This results in a data rate that is equal to the input clock frequency.

### AVERAGING/DECIMATION FILTER

The DEC\_RATE register (see Table 49) provides user control for the final filter stage (see Figure 20), which averages and decimates the accelerometers, gyroscopes, delta angle, and delta velocity data. The output sample rate is equal to  $2460 / (\text{DEC\_RATE} + 1)$ . When using the external sync clock option (FNCTIO\_CTRL[7:4], see Table 89), replace the 2460 number in this relationship with the input clock frequency. For example, turn to Page 3 (DIN = 0x8003), and set DEC\_RATE = 0x18 (DIN = 0x8C18, then DIN = 0x8D00) to reduce the output sample rate to 98.4 SPS ( $2460 \div 25$ ).

Table 49. DEC\_RATE (Page 3, Base Address = 0x0C)

| Bits    | Description (Default = 0x0000)  |
|---------|---|
| [15:11] | Don't care  |
| [10:0]  | Decimation rate, binary format, maximum = 2047, see Figure 20 for impact on sample rate |



**NOTES**  
 1. WHEN FNCTIO\_CTRL[7] = 1, EACH CLOCK PULSE ON THE DESIGNATED DIOx LINE (FNCTIO\_CTRL[5:4]) STARTS A 4-SAMPLE BURST, AT A SAMPLE RATE OF 9.84kHz. THESE FOUR SAMPLES FEED INTO THE 4x AVERAGE/DECIMATION FILTER, WHICH PRODUCES A DATA RATE THAT IS EQUAL TO THE INPUT CLOCK FREQUENCY.

10686-019

Figure 20. Sampling and Frequency Response Signal Flow

**FIR FILTER BANKS**

The ADIS16485 provides four configurable, 120-tap FIR filter banks. Each coefficient is 16 bits wide and occupies its own register location with each page. When designing a FIR filter for these banks, use a sample rate of 2.46 kHz and scale the coefficients so that their sum equals 32,768. For filter designs that have less than 120 taps, load the coefficients into the lower portion of the filter and start with Coefficient 1. Make sure that all unused taps are equal to zero, so that they do not add phase delay to the response. The FILTR\_BNK\_x registers provide three bits per sensor, which configure the filter bank (A, B, C, D) and turn filtering on and off. For example, turn to Page 3 (DIN = 0x8003), then write 0x002F to FILTR\_BNK\_0 (DIN = 0x962F, DIN = 0x9700) to set the x-axis gyroscope to use the FIR filter in Bank D, to set the y-axis gyroscope to use the FIR filter in Bank B, and to enable these FIR filters in both x- and y-axis gyroscopes. Note that the filter settings update after writing to the upper byte; therefore, always configure the lower byte first. In cases that require configuration to only the lower byte of either FILTR\_BNK\_0 or FILTR\_BNK\_1, complete the process by writing 0x00 to the upper byte.

**Table 50. FILTR\_BNK\_0 (Page 3, Base Address = 0x16)**

| Bits    | Description (Default = 0x0000)  |
|---------|---|
| 15      | Don't care  |
| 14      | Y-axis accelerometer filter enable (1 = enabled)  |
| [13:12] | Y-axis accelerometer filter bank selection:<br>00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D |
| 11      | X-axis accelerometer filter enable (1 = enabled)  |
| [10:9]  | X-axis accelerometer filter bank selection:<br>00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D |
| 8       | Z-axis gyroscope filter enable (1 = enabled)  |
| [7:6]   | Z-axis gyroscope filter bank selection:<br>00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D     |
| 5       | Y-axis gyroscope filter enable (1 = enabled)  |
| [4:3]   | Y-axis gyroscope filter bank selection:<br>00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D     |
| 2       | X-axis gyroscope filter enable (1 = enabled)  |
| [1:0]   | X-axis gyroscope filter bank selection:<br>00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D     |

**Table 51. FILTR\_BNK\_1 (Page 3, Base Address = 0x18)**

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:3] | Don't care  |
| 2      | Z-axis accelerometer filter enable (1 = enabled)  |
| [1:0]  | Z-axis accelerometer filter bank selection:<br>00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D |

**Filter Memory Organization**

Each filter bank uses two pages of the user register structure. See Table 52, Table 53, Table 54 and Table 55 for the register addresses in each filter bank.

**Table 52. Filter Bank A Memory Map, FIR\_COEF\_Axxx**

| Page | PAGE_ID | Address      | Register                          |
|------|---------|--------------|-----------------------------------|
| 5    | 0x05    | 0x00         | PAGE_ID                           |
| 5    | 0x05    | 0x02 to 0x07 | Not used                          |
| 5    | 0x05    | 0x08         | FIR_COEF_A000                     |
| 5    | 0x05    | 0x0A         | FIR_COEF_A001                     |
| 5    | 0x05    | 0x0C to 0x7C | FIR_COEF_A002 to<br>FIR_COEF_A058 |
| 5    | 0x05    | 0x7E         | FIR_COEF_A059                     |
| 6    | 0x06    | 0x00         | PAGE_ID                           |
| 6    | 0x06    | 0x02 to 0x07 | Not used                          |
| 6    | 0x06    | 0x08         | FIR_COEF_A060                     |
| 6    | 0x06    | 0x0A         | FIR_COEF_A061                     |
| 6    | 0x06    | 0x0C to 0x7C | FIR_COEF_A062 to<br>FIR_COEF_A118 |
| 6    | 0x06    | 0x7E         | FIR_COEF_A119                     |

**Table 53. Filter Bank B Memory Map, FIR\_COEF\_Bxxx**

| Page | PAGE_ID | Address      | Register                          |
|------|---------|--------------|-----------------------------------|
| 7    | 0x07    | 0x00         | PAGE_ID                           |
| 7    | 0x07    | 0x02 to 0x07 | Not used                          |
| 7    | 0x07    | 0x08         | FIR_COEF_B000                     |
| 7    | 0x07    | 0x0A         | FIR_COEF_B001                     |
| 7    | 0x07    | 0x0C to 0x7C | FIR_COEF_B002 to<br>FIR_COEF_B058 |
| 7    | 0x07    | 0x7E         | FIR_COEF_B059                     |
| 8    | 0x08    | 0x00         | PAGE_ID                           |
| 8    | 0x08    | 0x02 to 0x07 | Not used                          |
| 8    | 0x08    | 0x08         | FIR_COEF_B060                     |
| 8    | 0x08    | 0x0A         | FIR_COEF_B061                     |
| 8    | 0x08    | 0x0C to 0x7C | FIR_COEF_B062 to<br>FIR_COEF_B118 |
| 8    | 0x08    | 0x7E         | FIR_COEF_B119                     |

**Table 54. Filter Bank C Memory Map, FIR\_COEF\_Cxxx**

| Page | PAGE_ID | Address      | Register                          |
|------|---------|--------------|-----------------------------------|
| 9    | 0x09    | 0x00         | PAGE_ID                           |
| 9    | 0x09    | 0x02 to 0x07 | Not used                          |
| 9    | 0x09    | 0x08         | FIR_COEF_C000                     |
| 9    | 0x09    | 0x0A         | FIR_COEF_C001                     |
| 9    | 0x09    | 0x0C to 0x7C | FIR_COEF_C002 to<br>FIR_COEF_C058 |
| 9    | 0x09    | 0x7E         | FIR_COEF_C059                     |
| 10   | 0x0A    | 0x00         | PAGE_ID                           |
| 10   | 0x0A    | 0x02 to 0x07 | Not used                          |
| 10   | 0x0A    | 0x08         | FIR_COEF_C060                     |
| 10   | 0x0A    | 0x0A         | FIR_COEF_C061                     |
| 10   | 0x0A    | 0x0C to 0x7C | FIR_COEF_C062 to<br>FIR_COEF_C118 |
| 10   | 0x0A    | 0x7E         | FIR_COEF_C119                     |

Table 55. Filter Bank D Memory Map, FIR\_COEF\_Dxxx

| Page | PAGE_ID | Address      | Register                          |
|------|---------|--------------|-----------------------------------|
| 11   | 0x0B    | 0x00         | PAGE_ID                           |
| 11   | 0x0B    | 0x02 to 0x07 | Not used                          |
| 11   | 0x0B    | 0x08         | FIR_COEF_D000                     |
| 11   | 0x0B    | 0x0A         | FIR_COEF_D001                     |
| 11   | 0x0B    | 0x0C to 0x7C | FIR_COEF_D002 to<br>FIR_COEF_D058 |
| 11   | 0x0B    | 0x7E         | FIR_COEF_D059                     |
| 12   | 0x0C    | 0x00         | PAGE_ID                           |
| 12   | 0x0C    | 0x02 to 0x07 | Not used                          |
| 12   | 0x0C    | 0x08         | FIR_COEF_D060                     |
| 12   | 0x0C    | 0x0A         | FIR_COEF_D061                     |
| 12   | 0x0C    | 0x0C to 0x7C | FIR_COEF_D062 to<br>FIR_COEF_D118 |
| 12   | 0x0C    | 0x7E         | FIR_COEF_D119                     |

**Default Filter Performance**

The FIR filter banks have factory programmed filter designs. They are all low-pass filters that have unity dc gain. Table 56 provides a summary of each filter design, and Figure 21 shows the frequency response characteristics. The phase delay is equal to 1/2 of the total number of taps.

Table 56. FIR Filter Descriptions, Default Configuration

| FIR Filter Bank | Taps | -3 dB Frequency (Hz) |
|-----------------|------|----------------------|
| A               | 120  | 310                  |
| B               | 120  | 55                   |
| C               | 32   | 275                  |
| D               | 32   | 63                   |

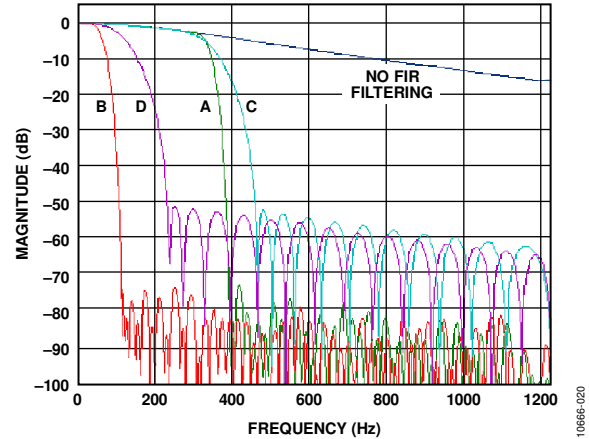


Figure 21. FIR Filter Frequency Response Curves

# CALIBRATION

The ADIS16485 factory calibration produces correction formulas for the gyroscopes and the accelerometers and then programs them into the flash memory. In addition, there are a series of user-configurable calibration registers for in-system tuning.

## GYROSCOPES

The user calibration for the gyroscopes includes registers for adjusting bias and sensitivity, as shown in Figure 22.

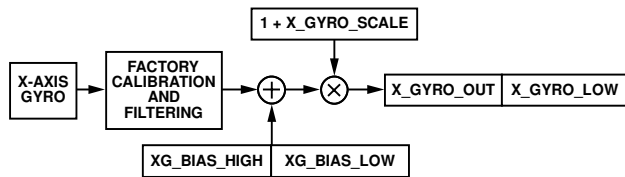


Figure 22. User Calibration Signal Path, Gyroscopes

### Manual Bias Correction

The xG\_BIAS\_HIGH registers (see Table 57, Table 58, and Table 59) and xG\_BIAS\_LOW registers (see Table 60, Table 61, and Table 62) provide a bias adjustment function for the output of each gyroscope sensor.

Table 57. XG\_BIAS\_HIGH (Page 2, Base Address = 0x12)

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:0] | X-axis gyroscope offset correction, upper word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec |

Table 58. YG\_BIAS\_HIGH (Page 2, Base Address = 0x16)

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:0] | Y-axis gyroscope offset correction, upper word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec |

Table 59. ZG\_BIAS\_HIGH (Page 2, Base Address = 0x1A)

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:0] | Z-axis gyroscope offset correction, upper word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec |

Table 60. XG\_BIAS\_LOW (Page 2, Base Address = 0x10)

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:0] | X-axis gyroscope offset correction, lower word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec ÷ 2 <sup>16</sup> = ~0.000000305°/sec |

Table 61. YG\_BIAS\_LOW (Page 2, Base Address = 0x14)

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:0] | Y-axis gyroscope offset correction, lower word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec ÷ 2 <sup>16</sup> = ~0.000000305°/sec |

Table 62. ZG\_BIAS\_LOW (Page 2, Base Address = 0x18)

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:0] | Z-axis gyroscope offset correction, lower word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec ÷ 2 <sup>16</sup> = ~0.000000305°/sec |

### Bias Null Command

The continuous bias estimator (CBE) accumulates and averages data in a 64-sample FIFO. The average time (t<sub>A</sub>) for the bias estimates relies on the sample time base setting in NULL\_CNFG[3:0] (see Table 63). Users can load the correction factors of the CBE into the gyroscope offset correction registers (see Table 57, Table 58, Table 59, Table 60, Table 61, and Table 62) using the bias null command in GLOB\_CMD[0] (see Table 86). NULL\_CNFG[13:8] provide on/off controls for the sensors that update when issuing a bias null command. The factory default configuration for NULL\_CNFG enables the bias null command for the gyroscopes, disables the bias null command for the accelerometers, and establishes the average time to ~26.64 seconds. For best results, make sure the ADIS16485 is stationary for this entire time.

Table 63. NULL\_CNFG (Page 3, Base Address = 0x0E)

| Bits    | Description (Default = 0x070A)  |
|---------|---|
| [15:14] | Not used  |
| 13      | Z-axis acceleration bias correction enable (1 = enabled)  |
| 12      | Y-axis acceleration bias correction enable (1 = enabled)  |
| 11      | X-axis acceleration bias correction enable (1 = enabled)  |
| 10      | Z-axis gyroscope bias correction enable (1 = enabled)   |
| 9       | Y-axis gyroscope bias correction enable (1 = enabled)   |
| 8       | X-axis gyroscope bias correction enable (1 = enabled)   |
| [7:4]   | Not used  |
| [3:0]   | Time base control (TBC), range: 0 to 13 (default = 10); t <sub>B</sub> = 2 <sup>TBC</sup> /2460, time base, t <sub>A</sub> = 64 × t <sub>B</sub> , average time |

Turn to Page 3 (DIN = 0x8003) and set GLOB\_CMD[0] = 1 (DIN = 0x8201, then DIN = 0x8300) to update the user offset registers with the correction factors of the CBE.

### Manual Sensitivity Correction

The x\_GYRO\_SCALE registers enable sensitivity adjustment (see Table 64, Table 65, and Table 66).

Table 64. X\_GYRO\_SCALE (Page 2, Base Address = 0x04)

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:0] | X-axis gyroscope scale correction; twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2 <sup>15</sup> = ~0.003052% |

Table 65. Y\_GYRO\_SCALE (Page 2, Base Address = 0x06)

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:0] | Y-axis gyroscope scale correction; twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2 <sup>15</sup> = ~0.003052% |

Table 66. Z\_GYRO\_SCALE (Page 2, Base Address = 0x08)

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:0] | Z-axis gyroscope scale correction; twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2 <sup>15</sup> = ~0.003052% |

**Linear Acceleration on Effect on Gyroscope Bias**

MEMS gyroscopes typically have a bias response to linear acceleration that is normal to their axes of rotation. The ADIS16485 offers an optional compensation function for this effect; the factory default setting (0x00C0) for the CONFIG register enables this function. To turn it off, turn to Page 3 (DIN = 0x8003) and set CONFIG[7] = 0 (DIN = 0x8A20, DIN = 0x8B00). Note that this also keeps the point of percussion alignment function enabled.

**Table 67. CONFIG (Page 3, Base Address = 0x0A)**

| Bits   | Description (Default = 0x00C0)   |
|--------|--|
| [15:8] | Not used   |
| 7      | Linear-g compensation for gyroscopes (1 = enabled)                         |
| 6      | Point of percussion alignment (1 = enabled)                                |
| [5:2]  | Not used   |
| 1      | Real-time clock, daylight savings time (1: enabled, 0: disabled)           |
| 0      | Real-time clock control (1: relative/elapsed timer mode, 0: calendar mode) |

**ACCELEROMETERS**

The user calibration for the accelerometers includes registers for adjusting bias and sensitivity, as shown in Figure 23.

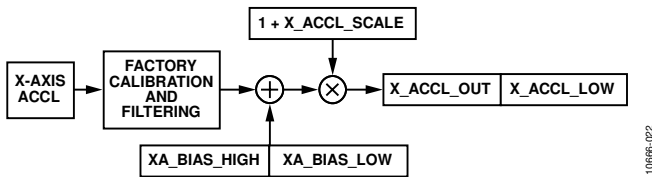


Figure 23. User Calibration Signal Path, Gyroscopes

**Manual Bias Correction**

The xA\_BIAS\_HIGH (see Table 68, Table 69, and Table 70) and xA\_BIAS\_LOW (see Table 71, Table 72, and Table 73) registers provide a bias adjustment function for the output of each accelerometer sensor. The xA\_BIAS\_HIGH registers use the same format as x\_ACCL\_OUT registers. The xA\_BIAS\_LOW registers use the same format as x\_ACCL\_LOW registers.

**Table 68. XA\_BIAS\_HIGH (Page 2, Base Address = 0x1E)**

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:0] | X-axis accelerometer offset correction, high word; twos complement, 0 g = 0x0000, 1 LSB = 0.25 mg |

**Table 69. YA\_BIAS\_HIGH (Page 2, Base Address = 0x22)**

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:0] | Y-axis accelerometer offset correction, high word; twos complement, 0 g = 0x0000, 1 LSB = 0.25 mg |

**Table 70. ZA\_BIAS\_HIGH (Page 2, Base Address = 0x26)**

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:0] | Z-axis accelerometer offset correction, high word; twos complement, 0 g = 0x0000, 1 LSB = 0.25 mg |

**Table 71. XA\_BIAS\_LOW (Page 2, Base Address = 0x1C)**

| Bits   | Description (Default = 0x0000)   |
|--------|--|
| [15:0] | X-axis accelerometer offset correction, low word; twos complement, 0 g = 0x0000, 1 LSB = 0.25 mg ÷ 2 <sup>16</sup> = ~0.000003815 mg |

**Table 72. YA\_BIAS\_LOW (Page 2, Base Address = 0x20)**

| Bits   | Description (Default = 0x0000)   |
|--------|--|
| [15:0] | Y-axis accelerometer offset correction, low word; twos complement, 0 g = 0x0000, 1 LSB = 0.25 mg ÷ 2 <sup>16</sup> = ~0.000003815 mg |

**Table 73. ZA\_BIAS\_LOW (Page 2, Base Address = 0x24)**

| Bits   | Description (Default = 0x0000)   |
|--------|--|
| [15:0] | Z-axis accelerometer offset correction, low word; twos complement, 0 g = 0x0000, 1 LSB = 0.25 mg ÷ 2 <sup>16</sup> = ~0.000003815 mg |

**Manual Sensitivity Correction**

The x\_ACCL\_SCALE registers enable sensitivity adjustment (see Table 74, Table 75, Table 76).

**Table 74. X\_ACCL\_SCALE (Page 2, Base Address = 0x0A)**

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:0] | X-axis accelerometer scale correction; twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2 <sup>15</sup> = ~0.003052% |

**Table 75. Y\_ACCL\_SCALE (Page 2, Base Address = 0x0C)**

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:0] | Y-axis accelerometer scale correction; twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2 <sup>15</sup> = ~0.003052% |

**Table 76. Z\_ACCL\_SCALE (Page 2, Base Address = 0x0E)**

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:0] | Z-axis accelerometer scale correction; twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2 <sup>15</sup> = ~0.003052% |



### RESTORING FACTORY CALIBRATION

Turn to Page 3 (DIN = 0x8003) and set GLOB\_CMD[6] = 1 (DIN = 0x8240, DIN = 0x8300) to execute the factory calibration restore function. This function resets each user calibration register to zero, resets all sensor data to 0, and automatically updates the flash memory within 900 ms. See Table 86 for more information on GLOB\_CMD.

### POINT OF PERCUSSION ALIGNMENT

CONFIG[6] offers a point of percussion alignment function that maps the accelerometer sensors to the corner of the package identified in Figure 24. To activate this feature, turn to Page 3 (DIN = 0x8003), then set CONFIG[6] = 1 (DIN = 0x8A40, DIN = 0x8B00). See Table 67 for more information on the CONFIG register.

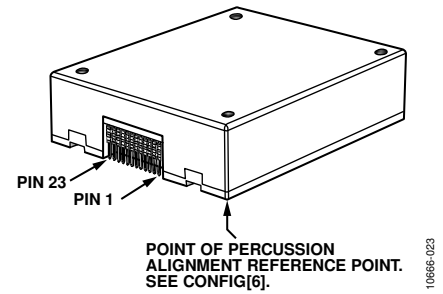


Figure 24. Point of Percussion Reference Point

## ALARMS

Each sensor has an independent alarm function that provides controls for alarm magnitude, polarity, and enabling a dynamic rate-of-change option. The ALM\_STS register (see Table 43) contains the alarm output flags and the FNCTIO\_CTRL register (see Table 89) provides an option for configuring one of the digital I/O lines as an alarm indicator.

### STATIC ALARM USE

The static alarm setting compares the output of each sensor with the trigger settings in the xx\_ALM\_MAGN registers (see Table 77, Table 78, Table 79, Table 80, Table 81, and Table 82) of that sensor. The polarity controls for each alarm are in the ALM\_CNFG\_x registers (see Table 83 and Table 84) and establish the relationship for the condition that causes the corresponding alarm flag to be active. For example, when ALM\_CNFG\_0[13] = 1, the alarm flag for the x-axis accelerometer (ALM\_STS[3], see Table 43) becomes active (equal to 1) when X\_ACCL\_OUT is greater than XA\_ALM\_MAGN.

### DYNAMIC ALARM USE

The dynamic alarm setting provides the option to compare the change in each sensor output over a period of 48.7 ms with the xx\_ALM\_MAGN register that sensor.

**Table 77. XG\_ALM\_MAGN (Page 3, Base Address = 0x28)**

| Bits   | Description (Default = 0x0000)   |
|--------|--|
| [15:0] | X-axis gyroscope alarm threshold settings; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec |

**Table 78. YG\_ALM\_MAGN (Page 3, Base Address = 0x2A)**

| Bits   | Description (Default = 0x0000)   |
|--------|--|
| [15:0] | Y-axis gyroscope alarm threshold settings; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec |

**Table 79. ZG\_ALM\_MAGN (Page 3, Base Address = 0x2C)**

| Bits   | Description (Default = 0x0000)   |
|--------|--|
| [15:0] | Z-axis gyroscope alarm threshold settings; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec |

**Table 80. XA\_ALM\_MAGN (Page 3, Base Address = 0x2E)**

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:0] | X-axis accelerometer alarm threshold settings; twos complement, 0 g = 0x0000, 1 LSB = 0.25 mg |

**Table 81. YA\_ALM\_MAGN (Page 3, Base Address = 0x30)**

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:0] | Y-axis accelerometer alarm threshold settings; twos complement, 0 g = 0x0000, 1 LSB = 0.25 mg |

**Table 82. ZA\_ALM\_MAGN (Page 3, Base Address = 0x32)**

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:0] | Z-axis accelerometer alarm threshold settings; twos complement, 0 g = 0x0000, 1 LSB = 0.25 mg |

**Table 83. ALM\_CNFG\_0 (Page 3, Base Address = 0x20)**

| Bits | Description (Default = 0x0000)  |
|------|---|
| 15   | X-axis accelerometer alarm (1 = enabled)  |
| 14   | Not used  |
| 13   | X-axis accelerometer alarm polarity<br>1 = active when X_ACCL_OUT > XA_ALM_MAGN<br>0 = active when X_ACCL_OUT > XA_ALM_MAGN |
| 12   | X-axis accelerometer dynamic enable (1 = enabled)   |
| 11   | Z-axis gyroscope alarm (1 = enabled)  |
| 10   | Not used  |
| 9    | Z-axis gyroscope alarm polarity<br>1 = active when Z_GYRO_OUT > ZG_ALM_MAGN<br>0 = active when Z_GYRO_OUT > ZG_ALM_MAGN     |
| 8    | Z-axis gyroscope dynamic enable (1 = enabled)   |
| 7    | Y-axis gyroscope alarm (1 = enabled)  |
| 6    | Not used  |
| 5    | Y-axis gyroscope alarm polarity<br>1 = active when Y_GYRO_OUT > YG_ALM_MAGN<br>0 = active when Y_GYRO_OUT > YG_ALM_MAGN     |
| 4    | Y-axis gyroscope dynamic enable (1 = enabled)   |
| 3    | X-axis gyroscope alarm (1 = enabled)  |
| 2    | Not used  |
| 1    | X-axis gyroscope alarm polarity<br>1 = active when X_GYRO_OUT > XG_ALM_MAGN<br>0 = active when X_GYRO_OUT > XG_ALM_MAGN     |
| 0    | X-axis gyroscope dynamic enable (1 = enabled)   |

**Table 84. ALM\_CNFG\_1 (Page 3, Base Address = 0x22)**

| Bits   | Description (Default = 0x0000)  |
|--------|---|
| [15:8] | Don't care  |
| 7      | Z-axis accelerometer alarm (1 = enabled)  |
| 6      | Not used  |
| 5      | Z-axis accelerometer alarm polarity<br>1 = active when Z_ACCL_OUT > ZA_ALM_MAGN<br>0 = active when Z_ACCL_OUT > ZA_ALM_MAGN |
| 4      | Z-axis accelerometer dynamic enable (1 = enabled)   |
| 3      | Y-axis accelerometer alarm (1 = enabled)  |
| 2      | Not used  |
| 1      | Y-axis accelerometer alarm polarity<br>1 = active when Y_ACCL_OUT > YA_ALM_MAGN<br>0 = active when Y_ACCL_OUT > YA_ALM_MAGN |
| 0      | Y-axis accelerometer dynamic enable (1 = enabled)   |

### Alarm Example

Table 85 offers an alarm configuration example, which sets the z-axis gyroscope alarm to trip when Z\_GYRO\_OUT > 131.1°/sec (0x199B).

**Table 85. Alarm Configuration Example**

| DIN            | Description              |
|----------------|--------------------------|
| 0xAC9B, 0xAD19 | Set ZG_ALM_MAGN = 0x199B |
| 0xA000, 0xA10A | Set ALM_CNFG_0 = 0x0A00  |

## SYSTEM CONTROLS

The ADIS16485 provides a number of system level controls for managing its operation, which include reset, self test, calibration, memory management, and I/O configuration.

### GLOBAL COMMANDS

The GLOB\_CMD register (see Table 86) provides trigger bits for several operations. Write 1 to the appropriate bit in GLOB\_CMD to start a function. After the function completes, the bit restores to 0.

**Table 86. GLOB\_CMD (Page 3, Base Address = 0x02)**

| Bits   | Description                 | Execution Time |
|--------|-----------------------------|----------------|
| [15:8] | Not used                    | Not applicable |
| 7      | Software reset              | 120 ms         |
| 6      | Factory calibration restore | 75 ms          |
| [5:4]  | Not used                    | Not applicable |
| 3      | Flash memory update         | 375 ms         |
| 2      | Flash memory test           | 50 ms          |
| 1      | Self test                   | 12 ms          |
| 0      | Bias null                   | See Table 63   |

#### Software Reset

Turn to Page 3 (DIN = 0x8003) and then set GLOB\_CMD[7] = 1 (DIN = 0x8280, DIN = 0x8300) to reset the operation, which removes all data, initializes all registers from their flash settings, and starts data collection. This function provides a firmware alternative to the RST pin (see Table 6, Pin 8).

#### Automatic Self Test

Turn to Page 3 (DIN = 0x8003) and then set GLOB\_CMD[1] = 1 (DIN = 0x8202, then DIN = 0x8300) to run an automatic, self test routine, which executes the following steps:

1. Measure the output on each sensor.
2. Activate the self test on each sensor.
3. Measure the output on each sensor.
4. Deactivate the self test on each sensor.
5. Calculate the difference with the self test on and off.
6. Compare the difference with the internal pass/fail criteria.
7. Report the pass/fail results for each sensor in DIAG\_STS.

After waiting 12 ms for this test to complete, turn to Page 0 (DIN = 0x8000) and read DIAG\_STS using DIN = 0x0A00. Note that using an external clock can extend this time. When using an external clock of 100 Hz, this time extends to 35 ms. Note that 100 Hz is too slow for optimal sensor performance.

## MEMORY MANAGEMENT

The data retention of the flash memory depends on the temperature and the number of write cycles. Figure 25 characterizes the dependence on temperature, and the FLSHCNT\_LOW and FLSHCNT\_HIGH registers (see Table 87 and Table 88) provide a running count of flash write cycles. The flash updates every time GLOB\_CMD[6], GLOB\_CMD[3], or GLOB\_CMD[0] is set to 1.

**Table 87. FLSHCNT\_LOW (Page 2, Base Address = 0x7C)**

| Bits   | Description   |
|--------|---|
| [15:0] | Binary counter; number of flash updates, lower word |

**Table 88. FLSHCNT\_HIGH (Page 2, Base Address = 0x7E)**

| Bits   | Description   |
|--------|---|
| [15:0] | Binary counter; number of flash updates, upper word |

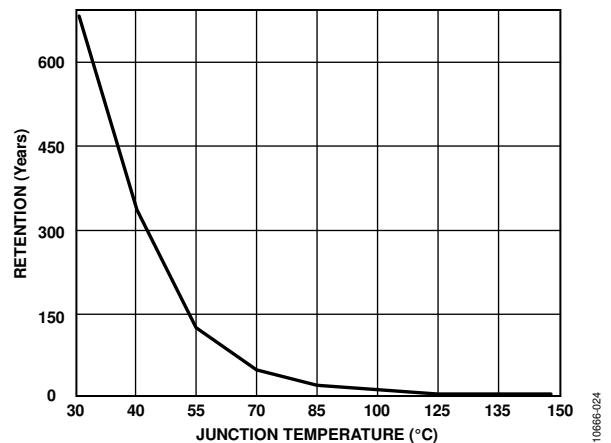


Figure 25. Flash Memory Retention

#### Flash Memory Test

Turn to Page 3 (DIN = 0x8003), and then set GLOB\_CMD[2] = 1 (DIN = 0x8204, DIN = 0x8300) to run a checksum test of the internal flash memory, which compares a factory programmed value with the current sum of the same memory locations. The result of this test loads into SYS\_E\_FLAG[6]. Turn to Page 0 (DIN = 0x8000) and use DIN = 0x0800 to read SYS\_E\_FLAG.

## GENERAL-PURPOSE I/O

There are four general-purpose I/O pins: DIO1, DIO2, DIO3, and DIO4. The FNCTIO\_CTRL register controls the basic function of each I/O pin. Each I/O pin only supports one function at a time. In cases where a single pin has two different assignments, the enable bit for the lower priority function automatically resets to zero and is disabled. The priority is (1) data-ready, (2) sync clock input, (3) alarm indicator, and (4) general-purpose, where 1 identifies the highest priority and 4 indicates the lowest priority.

**Table 89. FNCTIO\_CTRL (Page 3, Base Address = 0x06)**

| Bits    | Description (Default = 0x000D)   |
|---------|--|
| [15:12] | Not used   |
| 11      | Alarm indicator: 1 = enabled, 0 = disabled                                     |
| 10      | Alarm indicator polarity: 1 = positive, 0 = negative                           |
| [9:8]   | Alarm indicator line selection:<br>00 = DIO1, 01 = DIO2, 10 = DIO3, 11 = DIO4  |
| 7       | Sync clock input enable: 1 = enabled, 0 = disabled                             |
| 6       | Sync clock input polarity: 1 = rising edge, 0 = falling edge                   |
| [5:4]   | Sync clock input line selection:<br>00 = DIO1, 01 = DIO2, 10 = DIO3, 11 = DIO4 |
| 3       | Data-ready enable: 1 = enabled, 0 = disabled                                   |
| 2       | Data-ready polarity: 1 = positive, 0 = negative                                |
| [1:0]   | Data-ready line selection:<br>00 = DIO1, 01 = DIO2, 10 = DIO3, 11 = DIO4       |

### Data-Ready Indicator

FNCTIO\_CTRL[3:0] provide some configuration options for using one of the DIOx lines as a data-ready indicator signal, which can drive the interrupt control line of a processor. The factory default assigns DIO2 as a positive polarity, data-ready signal. Use the following sequence to change this assignment to DIO1 with a negative polarity: turn to Page 3 (DIN = 0x8003) and set FNCTIO\_CTRL[3:0] = 1000 (DIN = 0x8608, then DIN = 0x8700). The timing jitter on the data-ready signal is  $\pm 1.4 \mu\text{s}$ .

### Input Sync/Clock Control

FNCTIO\_CTRL[7:4] provide some configuration options for using one of the DIOx lines as an input synchronization signal for sampling inertial sensor data. For example, use the following sequence to establish DIO4 as a positive polarity, input clock pin and keep the factory default setting for the data-ready function: turn to Page 3 (DIN = 0x8003) and set FNCTIO\_CTRL[7:0] = 0xFD (DIN = 0x86FD, then DIN = 0x8700). Note that this command also disables the internal sampling clock, and no data sampling takes place without the input clock signal. When selecting a clock input frequency, consider the 330 Hz sensor bandwidth, because under sampling the sensors can degrade noise and stability performance.

## General-Purpose I/O Control

When FNCTIO\_CTRL does not configure a DIOx pin, GPIO\_CTRL provides register controls for general-purpose use of the pin. GPIO\_CTRL[3:0] provides input/output assignment controls for each pin. When the DIOx pins are inputs, monitor their levels by reading GPIO\_CTRL[7:4]. When the DIOx pins are used as outputs, set their levels by writing to GPIO\_CTRL[7:4]. For example, use the following sequence to set DIO1 and DIO3 as high and low output pins, respectively, and set DIO2 and DIO4 as input pins. Turn to Page 3 (DIN = 0x8003) and set GPIO\_CTRL[7:0] = 0x15 (DIN = 0x8815, then DIN = 0x8900).

**Table 90. GPIO\_CTRL (Page 3, Base Address = 0x08)**

| Bits   | Description (Default = 0x00X0) <sup>1</sup>                                    |
|--------|--|
| [15:8] | Don't care   |
| 7      | General-Purpose I/O Line 4 (DIO4) data level                                   |
| 6      | General-Purpose I/O Line 3 (DIO3) data level                                   |
| 5      | General-Purpose I/O Line 2 (DIO2) data level                                   |
| 4      | General-Purpose I/O Line 1 (DIO1) data level                                   |
| 3      | General-Purpose I/O Line 4 (DIO4) direction control<br>(1 = output, 0 = input) |
| 2      | General-Purpose I/O Line 3 (DIO3) direction control<br>(1 = output, 0 = input) |
| 1      | General-Purpose I/O Line 2 (DIO2) direction control<br>(1 = output, 0 = input) |
| 0      | General-Purpose I/O Line 1 (DIO1) direction control<br>(1 = output, 0 = input) |

<sup>1</sup> The GPIO\_CTRL register, Bits[7:4], reflect the levels on the DIOx pins and do not have a default setting.

## POWER MANAGEMENT

The SLP\_CNT register (see Table 91) provides controls for both power-down mode and sleep mode. The trade-off between power-down mode and sleep mode is between idle power and recovery time. Power-down mode offers the best idle power consumption but requires the most time to recover. Also, all volatile settings are lost during power-down but are preserved during sleep mode.

For timed sleep mode, turn to Page 3 (DIN = 0x8003), write the amount of sleep time to SLP\_CNT[7:0] and then, set SLP\_CNT[8] = 1 (DIN = 0x9101) to start the sleep period. For a timed power-down period, change the last command to set SLP\_CNT[9] = 1 (DIN = 0x9102). To power down or sleep for an indefinite period, set SLP\_CNT[7:0] = 0x00 first, then set either SLP\_CNT[8] or SLP\_CNT[9] to 1. Note that the command takes effect when the  $\overline{\text{CS}}$  line goes high. To awaken the device from sleep or power-down mode, use one of the following options to restore normal operation:

- Assert  $\overline{\text{CS}}$  from high to low.
- Pulse  $\overline{\text{RST}}$  low, then high again.
- Cycle the power.

For example, set SLP\_CNT[7:0] = 0x64 (DIN = 0x9064), then set SLP\_CNT[8] = 1 (DIN = 0x9101) to start a sleep period of 100 seconds.

**Table 91. SLP\_CNT (Page 3, Base Address = 0x10)**

| Bits    | Description  |
|---------|--|
| [15:10] | Not used   |
| 9       | Power-down mode                                      |
| 8       | Normal sleep mode                                    |
| [7:0]   | Programmable time bits; 1 sec/LSB; 0x00 = indefinite |

If the sleep mode and power-down mode bits are both set high, the normal sleep mode (SLP\_CNT[8]) bit takes precedence.

### General-Purpose Registers

The USER\_SCR\_x registers (see Table 92, Table 93, Table 94, and Table 95) provide four 16-bit registers for storing data.

**Table 92. USER\_SCR\_1 (Page 2, Base Address = 0x74)**

| Bits   | Description  |
|--------|--------------|
| [15:0] | User-defined |

**Table 93. USER\_SCR\_2 (Page 2, Base Address = 0x76)**

| Bits   | Description  |
|--------|--------------|
| [15:0] | User-defined |

**Table 94. USER\_SCR\_3 (Page 2, Base Address = 0x78)**

| Bits   | Description  |
|--------|--------------|
| [15:0] | User-defined |

**Table 95. USER\_SCR\_4 (Page 2, Base Address = 0x7A)**

| Bits   | Description  |
|--------|--------------|
| [15:0] | User-defined |

### Real-Time Clock Configuration/Data

The VDDRTC power supply pin (see Table 6, Pin 23) provides a separate supply for the real-time clock (RTC) function. This enables the RTC to keep track of time, even when the main supply (VDD) is off. Configure the RTC function by selecting one of two modes in CONFIG[0] (see Table 67). The real-time clock data is available in the TIME\_MS\_OUT register (see Table 96), TIME\_DH\_OUT register (see Table 97), and TIME\_YM\_OUT register (see Table 98). When using the elapsed timer mode, the time data registers start at 0x0000 when the device starts up (or resets) and begin keeping time in a manner that is similar to a stopwatch. When using the clock/calendar mode, write the current time to the real-time registers in the following sequence: seconds (TIME\_MS\_OUT[5:0]), minutes (TIME\_MS\_OUT[13:8]), hours (TIME\_DH\_OUT[5:0]), day (TIME\_DH\_OUT[12:8]), month (TIME\_YM\_OUT[3:0]), and year (TIME\_YM\_OUT[14:8]).

The updates to the timer do not become active until there is a successful write to the TIME\_YM\_OUT[14:8] byte. The real-time clock registers reflect the newly updated values only after the next seconds tick of the clock that follows the write to TIME\_YM\_OUT[14:8] (year). Writing to TIME\_YM\_OUT[14:8] activates all timing values; therefore, always write to this location last when updating the timer, even if the year information does not require updating.

Write the current time to each time data register after setting CONFIG[0] = 1 (DIN = 0x8003, DIN = 0x8A01). Note that CONFIG[1] provides a bit for managing daylight savings time. After the CONFIG and TIME\_xx\_OUT registers are configured, set GLOB\_CMD[3] = 1 (DIN = 0x8003, DIN = 0x8208, DIN = 0x8300) to back up these settings up in flash, and use a separate 3.3 V source to supply power to the VDDRTC function. Note that access to time data in the TIME\_xx\_OUT registers requires normal operation (VDD = 3.3 V and full startup), but the timer function only requires that VDDRTC = 3.3 V when the rest of the ADIS16485 is turned off.

**Table 96. TIME\_MS\_OUT (Page 0, Base Address = 0x78)**

| Bits    | Description                           |
|---------|---------------------------------------|
| [15:14] | Not used                              |
| [13:8]  | Minutes, binary data, range = 0 to 59 |
| [7:6]   | Not used                              |
| [5:0]   | Seconds, binary data, range = 0 to 59 |

**Table 97. TIME\_DH\_OUT (Page 0, Base Address = 0x7A)**

| Bits    | Description                         |
|---------|-------------------------------------|
| [15:13] | Not used                            |
| [12:8]  | Day, binary data, range = 1 to 31   |
| [7:6]   | Not used                            |
| [5:0]   | Hours, binary data, range = 0 to 23 |

**Table 98. TIME\_YM\_OUT (Page 0, Base Address = 0x7C)**

| Bits   | Description   |
|--------|---|
| [15]   | Not used  |
| [14:8] | Year, binary data, range = 0 to 99, relative to 2000 A.D. |
| [7:4]  | Not used  |
| [3:0]  | Month, binary data, range = 1 to 12                       |

# APPLICATIONS INFORMATION

## MOUNTING TIPS

For best performance, follow these simple rules when installing the ADIS16485 into a system.

1. Eliminate opportunity for translational force (x-axis and y-axis direction; see Figure 6).
2. Isolate mounting force to the four corners, on the part of the package surface that surrounds the mounting holes.
3. Use uniform mounting forces on all four corners. The suggested torque setting is 40 inch-ounces (0.285 N-m).

These three rules help prevent nonuniform force profiles, which can warp the package and introduce bias errors in the sensors. Figure 26 provides an example that leverages washers to set the package off the mounting surface and uses 2.85 mm pass-through holes and backside washers/nuts for attachment. Figure 27 and Figure 28 provide some details from mounting hole and connector alignment pin drill locations. For more information on mounting the ADIS16485, see the AN-1295 Application Note.

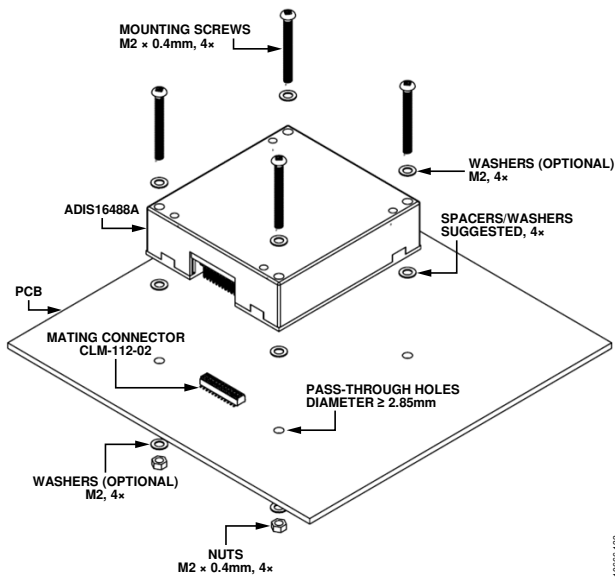
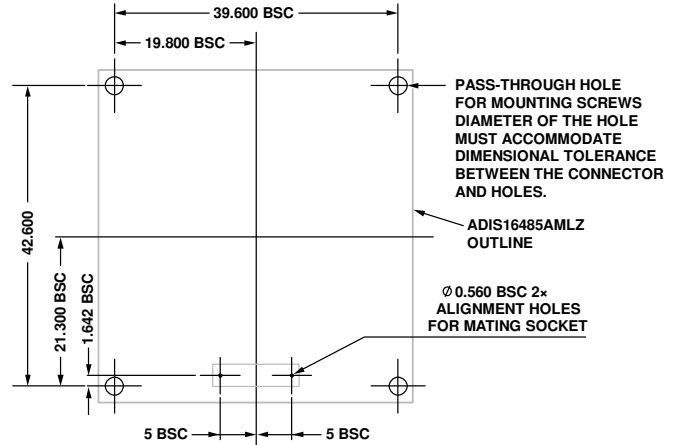


Figure 26. Mounting Example



- NOTES
1. ALL DIMENSIONS IN mm UNITS.
  2. THE CONNECTOR FACES DOWN AND ARE NOT VISIBLE FROM THIS VIEW.

Figure 27. Suggested PCB Layout Pattern, Connector Down

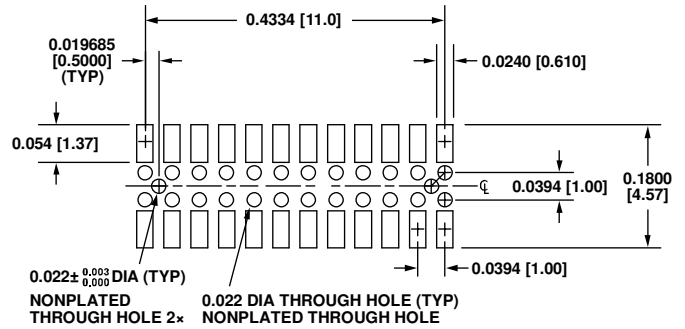


Figure 28. Suggested Layout and Mechanical Design when Using Samtec P/N CLM-112-02-G-D-A for the Mating Connector

## EVALUATION TOOLS

### Breakout Board, ADIS16IMU/PCBZ

The ADIS16IMU1/PCBZ (sold separately) provides a breakout board function for the ADIS16485, which means that it provides access to the ADIS16485 through larger connectors that support standard 1 mm ribbon cabling. It also provides four mounting holes for attachment of the ADIS16485 to the breakout board. For more information on the ADIS16IMU1/PCBZ, see <https://www.analog.com/en/evaluation/eval-adis16imu1/eb.html>.

### PC-Based Evaluation, EVAL-ADIS2

Use the EVAL-ADIS and the ADIS16IMU1/PCBZ to evaluate the ADIS16485 on a PC-based platform.

## POWER SUPPLY CONSIDERATIONS

The ADIS16485 has approximately  $\sim 24 \mu\text{F}$  of capacitance across the VDD and GND pins. While this capacitor bank provides a large amount of localized filtering, it also presents an opportunity for excessive charging current when the VDD voltage ramps too quickly. Use the following relationship to help determine the appropriate VDD voltage profile, with respect to any current limit functions that can cause the power supply to lose regulation and potentially introduce unsafe conditions for the ADIS16485.

$$i(t) = C \frac{dV}{dt}$$

In addition to managing the initial voltage ramp, take note of the transient current demand that the ADIS16485 requires during its start-up/self-initialization process. Once VDD reaches 2.85 V, the ADIS16485 begins its start-up process. Figure 29 offers a broad connection that communicates when to expect the spikes in current, and Figure 30 provides more detail on the current/time behavior during the peak transient condition, which typically occurs approximately 350 ms after VDD reaches 2.85 V. In Figure 30 notice that the peak current approaches 600 mA and the transient condition lasts for approximately 1.75 ms.

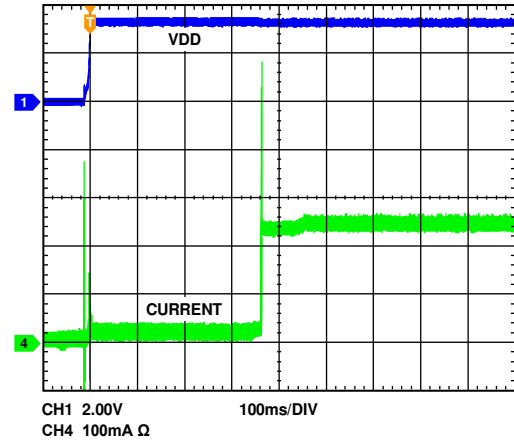


Figure 29. Transient Current Demand, Start-Up

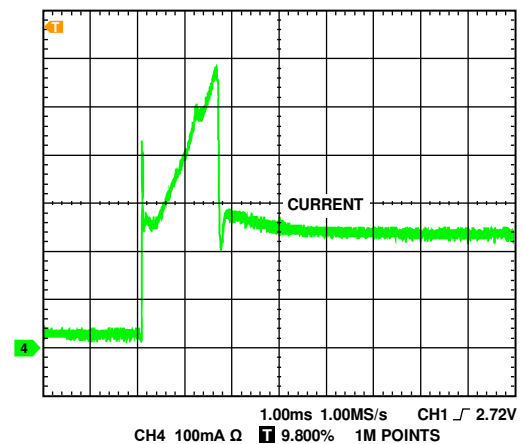


Figure 30. Transient Current Demand, Peak Demand

## X-RAY SENSITIVITY

Exposure to high dose rate X-rays, such as those in production systems that inspect solder joints in electronic assemblies, may affect accelerometer bias errors. For optimal performance, avoid exposing the ADIS16485 to this type of inspection.

OUTLINE DIMENSIONS

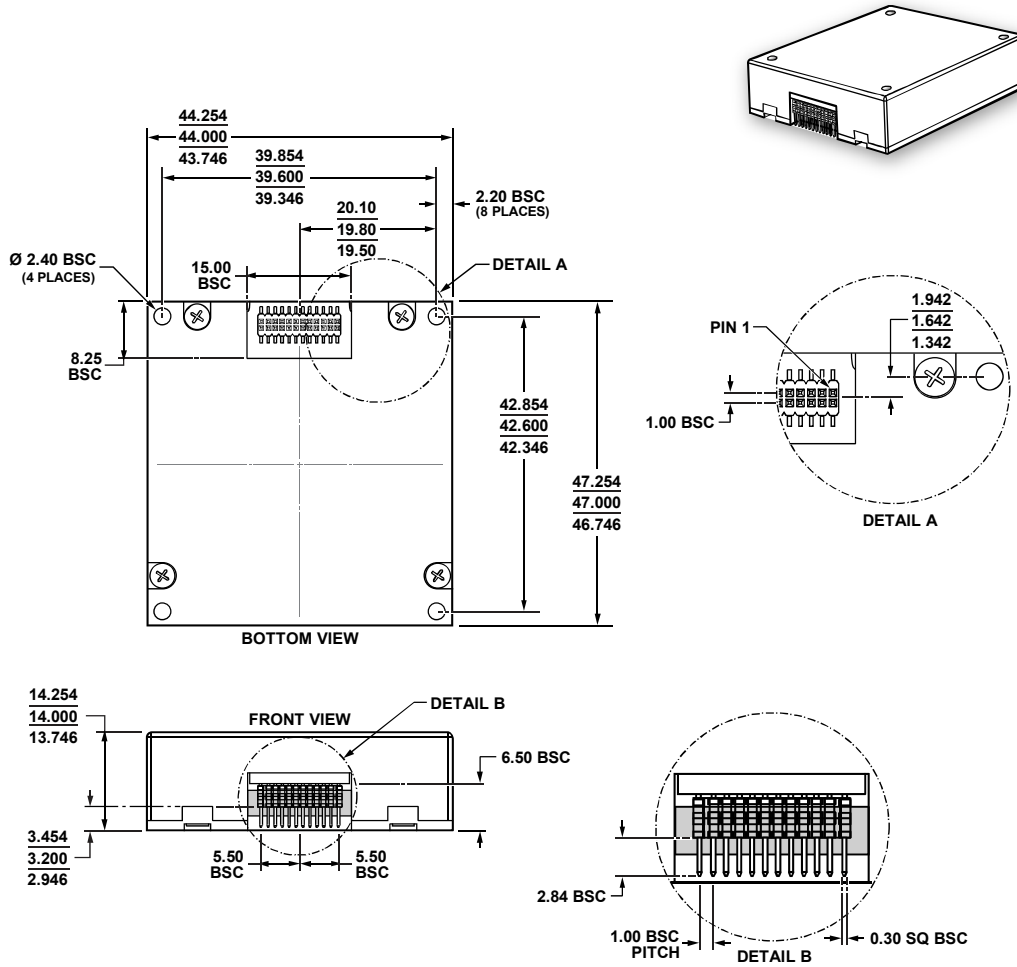


Figure 31. 24-Lead Module with Connector Interface [MODULE]  
(ML-24-6)  
Dimensions shown in millimeters

12-07-2012 E

ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description                              | Package Option |
|--------------------|-------------------|--|----------------|
| ADIS16485BMLZ      | -40°C to +105°C   | 24-Lead Module with Connector Interface [MODULE] | ML-24-6        |

<sup>1</sup> Z = RoHS Compliant Part.