HITFET^{TM}

BTS3060TF

Smart Low-Side Power Switch

Single channel, 50 mΩ

Datasheet

Rev. 1.0, 2014-07-21

Automotive Power

Table of Contents

HITFET - BTS3060TF
Smart Low-Side Power Switch

BTS3060TF

AEC Qualified RoHS

1 Overview

PG-TO252-3

Application

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for inductive loads as well as loads with inrush currents

Basic Features

- Single channel device
- Very low power DMOS leakage current in OFF state
- Electrostatic discharge protection (ESD)
- Green Product (RoHS compliant)
- AEC Qualified

Description

The BTS3060TF is a 50 mΩ single channel Smart Low-Side Power Switch with in a TO252-3 package providing embedded protective functions. The power transistor is built by an N-channel vertical power MOSFET.
The device is monolithically integrated. The BTS3060TF is automotive qualified and is optimized for 12V automotive applications.

Table 1 Product Summary

Operating voltage range	V_{OUT}	3.0 .. 35.0 V
Maximum load voltage	$V_{BAT(LD)}$	42 V
Maximum input voltage	V_{IN}	5.5 V
Maximum On-State resistance at T_J = 150°C, V_{IN} = 5 V	$R_{DS(ON)}$	135 mΩ
Nominal load current	$I_{L(NOM)}$	3 A
Minimum current limitation	$I_{L(LIM)}$	10.5 A
Maximum OFF state load current at T_J = 25°C	$I_{L(OFF)}$	2 µA

Protection Functions

- Latching over temperature protection
- Active clamp over voltage protection
- Current limitation

Type	Package	Marking
BTS3060TF	TO252-3	3060TF

Detailed Description

The device is able to switch all kind of resistive, inductive and capacitive loads, limited by E_{AS} and maximum current capabilities.

The BTS3060TF offers ESD protection on the IN Pin which refers to the Source pin (Ground).

The over temperature protection prevents the device from overheating due to overload and/or bad cooling conditions. The temperature information is given by a temperature sensor in the power MOSFET.

The BTS3060TF has a latching thermal shut-down function. The device will turn off until the input is toggeled and device reset.

The over voltage protection can be activated during load dump or inductive turn off conditions. The power MOSFET is limiting the drain-source voltage, if it rises above the $V_{OUT(CLAMP).}$

2 Block Diagram

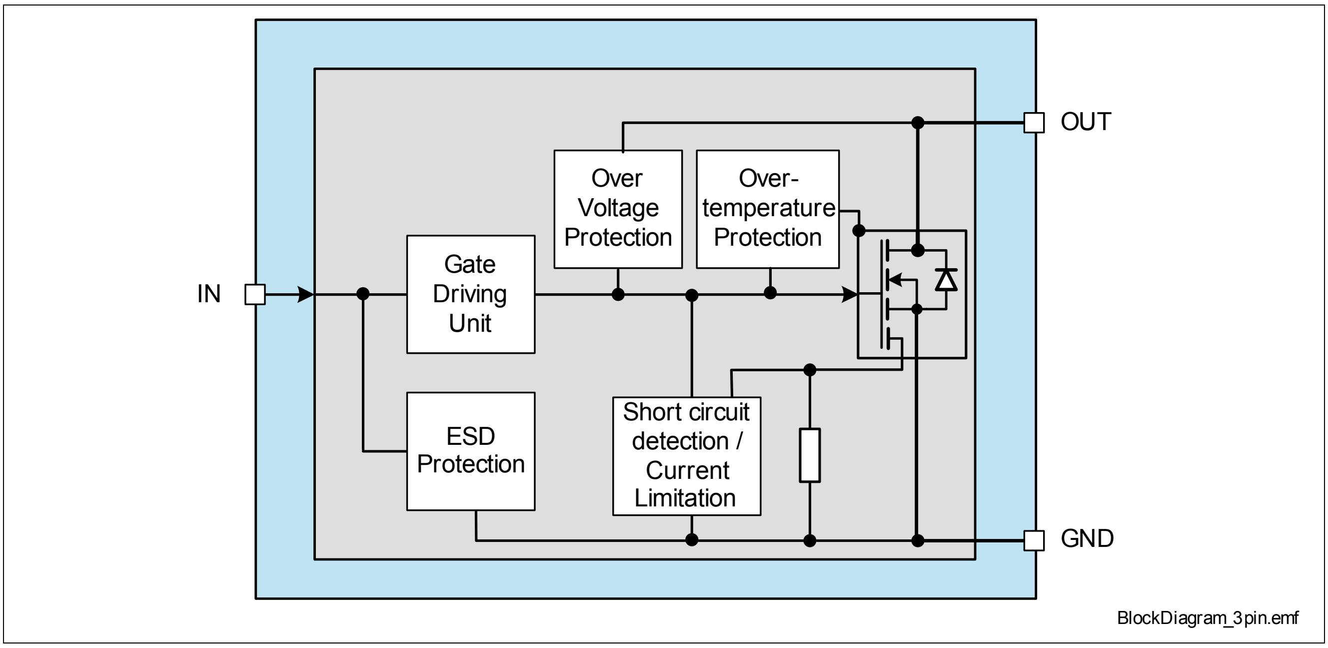


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment BTS3060TF

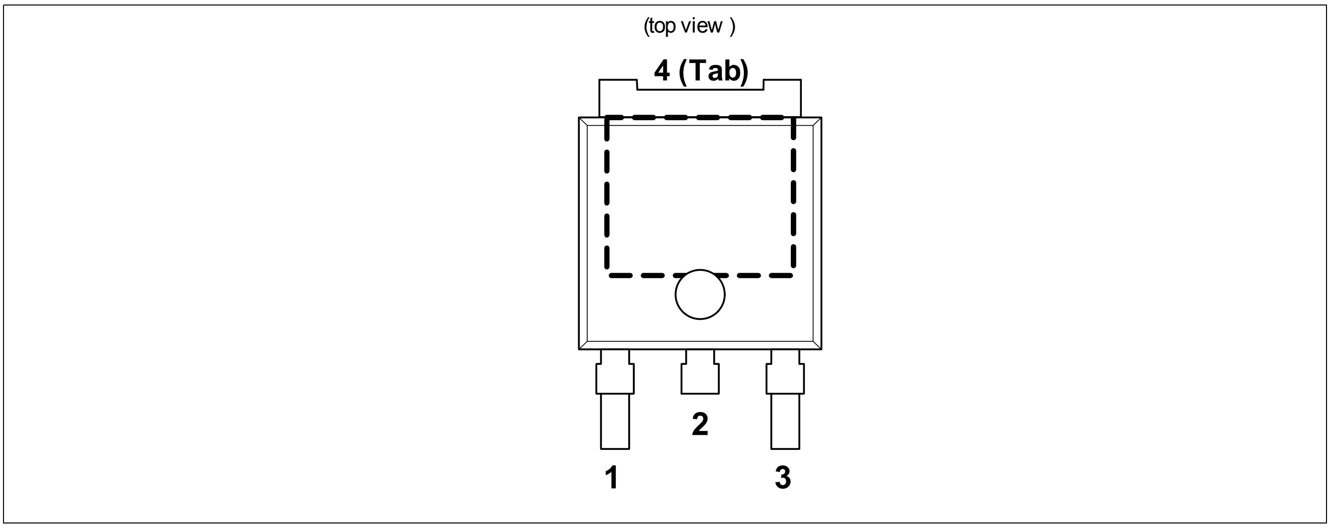


Figure 2 Pin Configuration TO252-3

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	IN	Input pin
2,4	OUT	Drain, Load connection for power DMOS
3	GND	Ground, Source of power DMOS

3.3 Voltage and current definition

Figure 3 shows all external terms used in this data sheet, with associated convention for positive values.

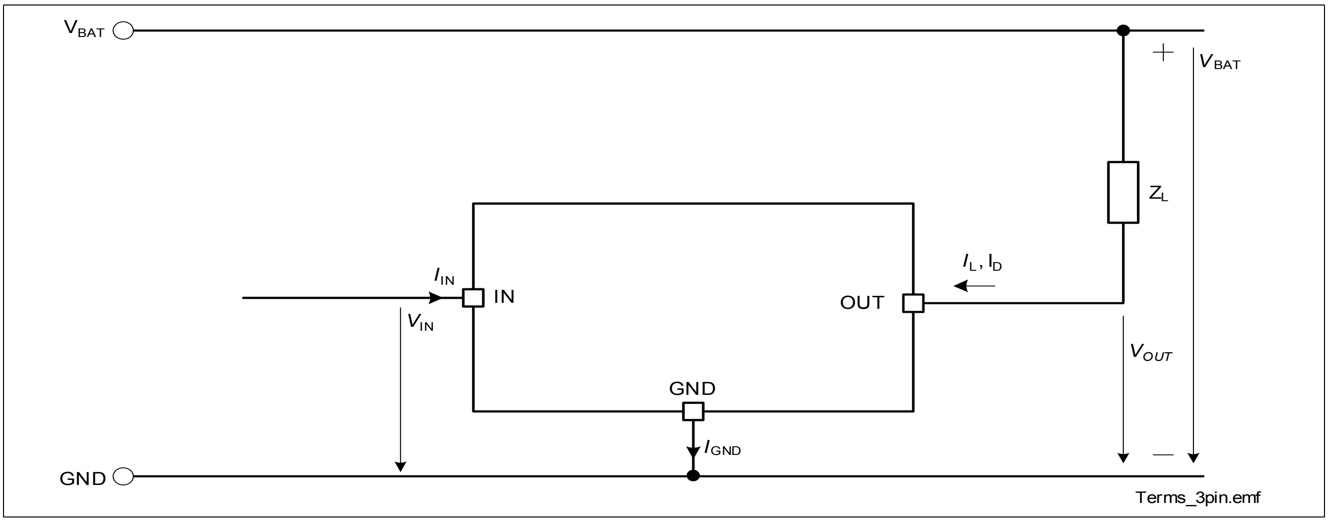


Figure 3 Naming definition of electrical parameters

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings 1)

T_J = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Note / Test Condition
			Min.	Max.		
Voltages						
4.1.1	Output voltage	V_{OUT}	–	42	V	internally clamped
4.1.2	Battery voltage for short circuit protection	$V_{BAT(SC)}$	–	35	V	l = 0 or 5m R_{SC} = 20 mΩ + R_{Cable} R_{Cable} = l * 16 mΩ/m L_{SC} = 5 µH + L_{Cable} L_{Cable} = l * 1 µH/m V_{IN} = 5 V
4.1.3	Battery voltage for load dump protection ($V_{BAT(LD)} = V_A + V_S$ with V_A = 13.5V)	$V_{BAT(LD)}$	–	42	V	2) R_i = 2 Ω R_{Load} = 4.5 Ω t_d = 400 ms suppressed pulse
Input Pin						
4.1.4	Input Voltage	V_{IN}	-0.3	5.5	V	–
Power Stage						
4.1.5	Load current	$\vert I_L \vert$	–	$I_{L(LIM)}$	A	–
Energies						
4.1.6	Unclamped single inductive energy single pulse	E_{AS}	–	55	mJ	$I_{L(0)}$ = 3 A V_{BAT} = 13.5 V $T_{J(0)}$ = 150 °C
4.1.7	Unclamped repetitive inductive energy pulse with 10k cycles	$E_{AR(10k)}$	–	40	mJ	$I_{L(0)}$ = 3 A V_{BAT} = 13.5 V $T_{J(0)}$ = 85 °C
4.1.8	Unclamped repetitive inductive energy pulse with 100k cycles	$E_{AR(100k)}$	–	20	mJ	$I_{L(0)}$ = 3 A V_{BAT} = 13.5 V $T_{J(0)}$ = 85 °C
Temperatures						
4.1.9	Operating temperature	T_j	-40	+150	°C	–
4.1.10	Storage temperature	T_{stg}	-55	+150	°C	–
ESD Susceptibility						
4.1.11	ESD susceptibility (all pins)	V_{ESD}	-2	2	kV	HBM3)
4.1.12	ESD susceptibility OUT-pin to GND	V_{ESD}	-4	4	kV	HBM3)
4.1.13	ESD susceptibility	V_{ESD}	-750	750	V	CDM4)

1) Not subject to production test, specified by design.

2) $V_{\mathrm{BAT(LD)}}$ is setup without the DUT connected to the generator per ISO7637-1;
R_{i} is the internal resistance of the load dump test pulse generator;
t_{d} is the pulse duration time for load dump pulse (pulse 5) according ISO 7637-1, -2.

3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ , 100 pF)

4) ESD susceptibility, Charged Device Model “CDM” ESDA STM5.3.1 or ANSI/ESD S.5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Table 3 Functional Range [1]

Please refer to **“Electrical Characteristics” on Page 18** for test conditions

Pos.	Parameter	Symbol	Limit Values		Unit	Note / Test Condition
			Min.	Max.		
4.2.1	Battery Voltage Range for Nominal Operation	V_{BAT}	8.0	18.0	V	–
4.2.2	Extended battery Voltage Range for Operation	V_{BAT}	3.0	35.0	V	parameter deviations possible
4.2.3	Input Voltage for Nominal Operation	$V_{\mathrm{IN(NOM)}}$	4.0	5.5	V	–
4.2.4	Extended Input Voltage Range for Operation	$V_{\mathrm{IN(EXT)}}$	2.5	4.0	V	over temperature latch available, parameter deviations possible
4.2.5	Junction Temperature	T_J	-40	150	°C	–

1) Not subject to production test, specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards.
*For more information, go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
4.3.1	Junction to Case	R_{thJC}	–	2	2.7	K/W	[1] [2]
4.3.2	Junction to Ambient (2s2p)	$R_{thJA(2s2p)}$	–	25	–	K/W	[1] [3]
4.3.3	Junction to Ambient (1s0p+600mm^2 Cu)	$R_{thJA(1s0p)}$	–	40	–	K/W	[1] [4]

1) Not subject to production test, specified by design
2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins are fixed to ambient temperature). T_a = 85 °C. Device is loaded with 1W power.
3) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the ex posed pad contacted the first inner copper layer. T_a = 85 °C, Device is loaded with 1W power.
4) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 600mm^2 and 70 µm thickness. T_a = 85 °C, Device is loaded with 1W power.

4.3.1 PCB set up

The following PCB set up was implemented to determine the transiet thermal impedance

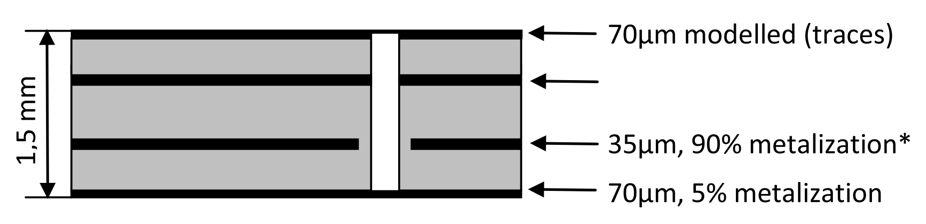


Figure 4 Cross section JEDEC2s2p.

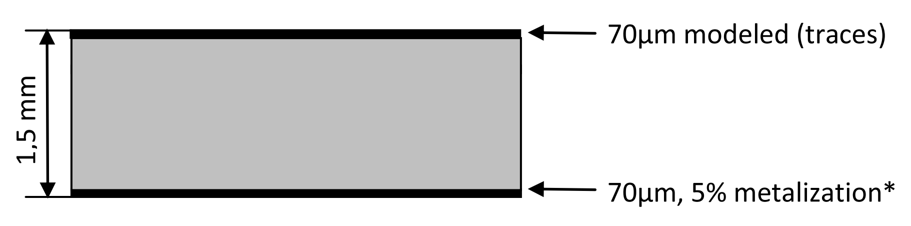
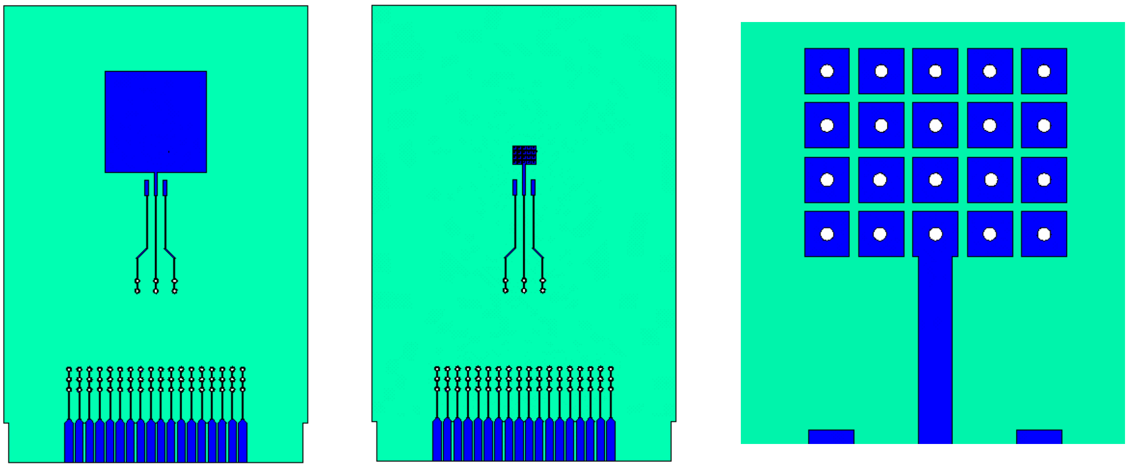


Figure 5 Cross section JEDEC1s0p.


JEDEC 1s0p 600mm²

JEDEC 1s0p / Footprint
JEDEC 2s2p

Detail: solder area

Figure 6 Cross section JEDEC1s0p.

4.3.2 Transient Thermal Impedance

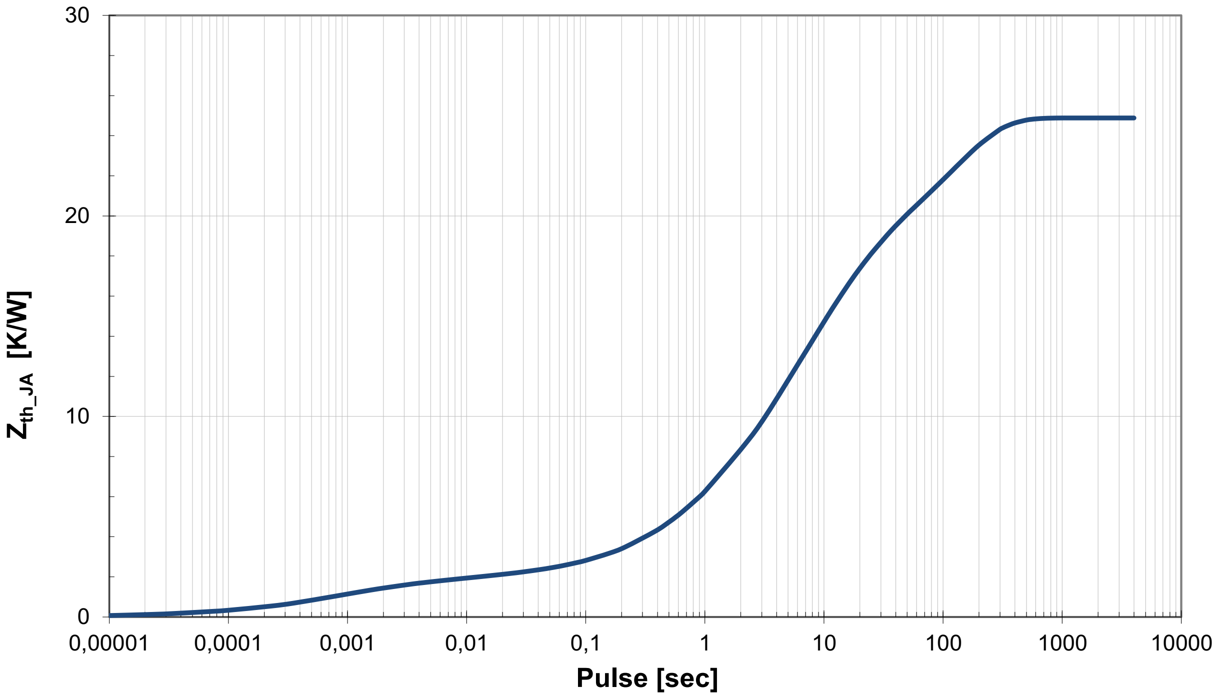


Figure 7 Typical transient thermal impedance $Z_{thJA} = f(t_p)$, T_a = 85°C
Value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Device is dissipating 1 W power.

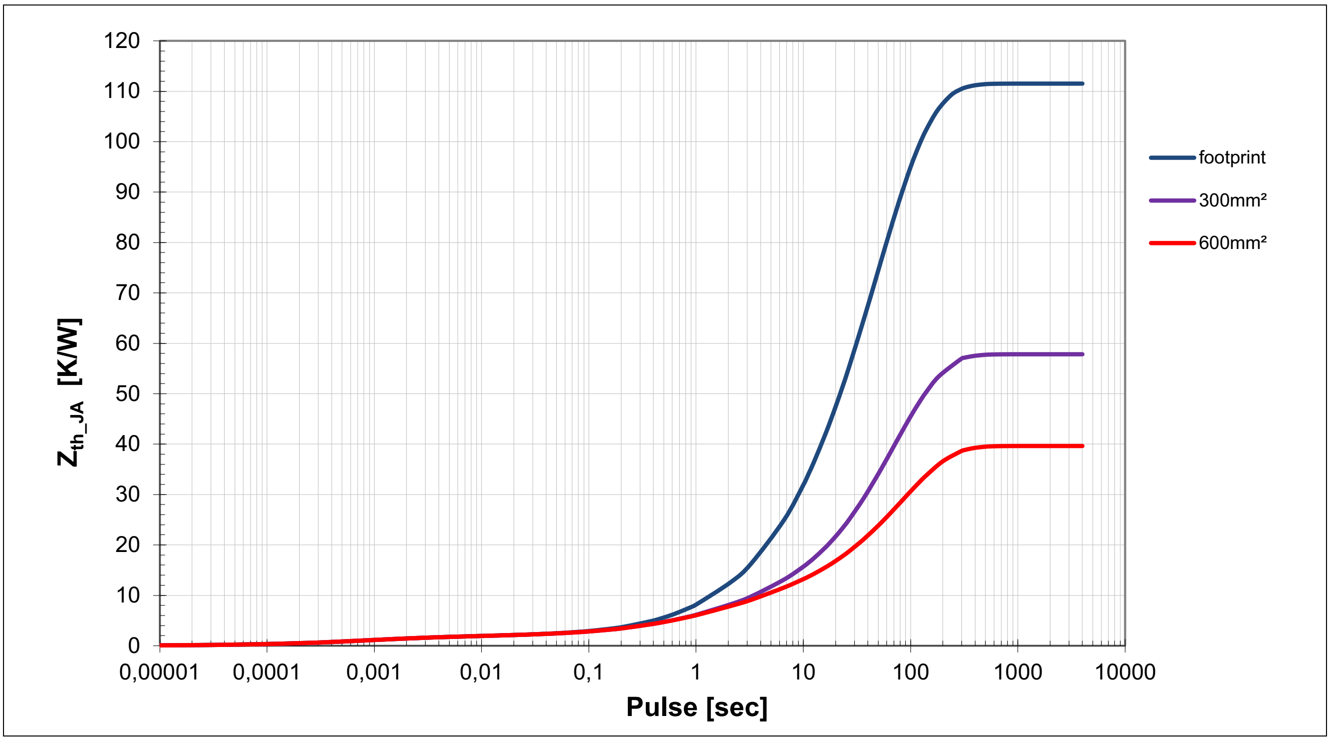


Figure 8 **Typical transient thermal impedance Z_{thJA} = f(t_p) , T_a = 85°C. PCB 1s0p -- cooling areas vs. R_{thJA}. Device is dissipating 1 W power.**

5 Power Stage

5.1 Output On-state Resistance

The on-state resistance depends on the junction temperature T_j and on the applied input voltage. **Figure 9** show this dependencies in terms of temperature and voltage for the typical on-state resistance $R_{DS(ON)}$. The behavior in reverse polarity is described in**"Reverse Current capability" on Page 14**

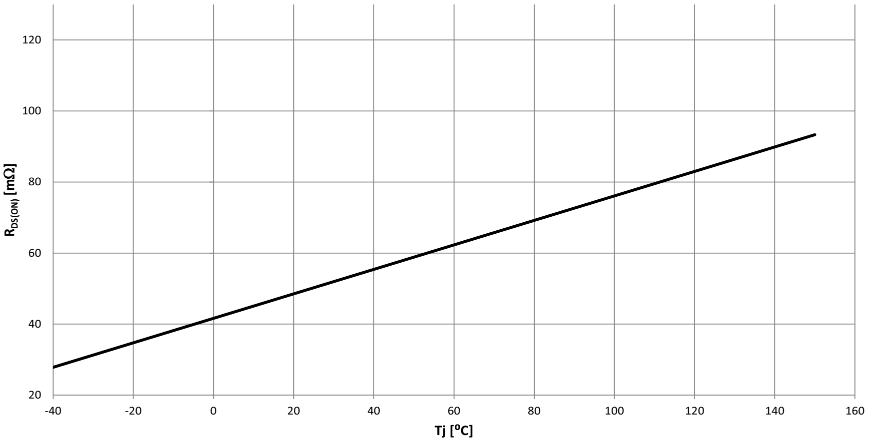


Figure 9 Typical On-State Resistance, $R_{DS(ON)} = f(T_j)$, V_{IN} = 5 V

5.2 Resistive Load Output Timing

Figure 10 shows the typical timing when switching a resisitive load .

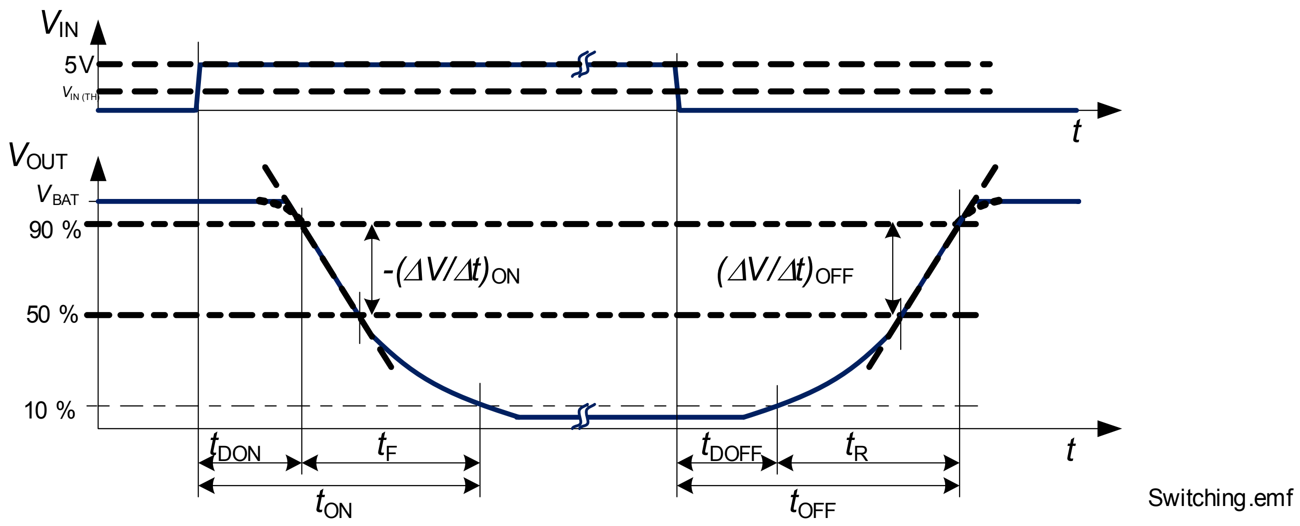


Figure 10 Definition of Power Output Timing for Resistive Load

5.3 Inductive Load

5.3.1 Output Clamping

When switching off inductive loads with low side switches, the Drain-Source voltage V_{OUT} rises above battery potential, because the inductance intends to continue driving the current. To prevent unwanted high voltages the device has a voltage clamping mechanism to keep the voltage at $V_{OUT(CLAMP)}$. During this clamping operation mode the device heats up as it dissipates the energy from the inductance. Therefore the maximum allowed load inductance is limited. See **Figure 11** and **Figure 12** for more details.

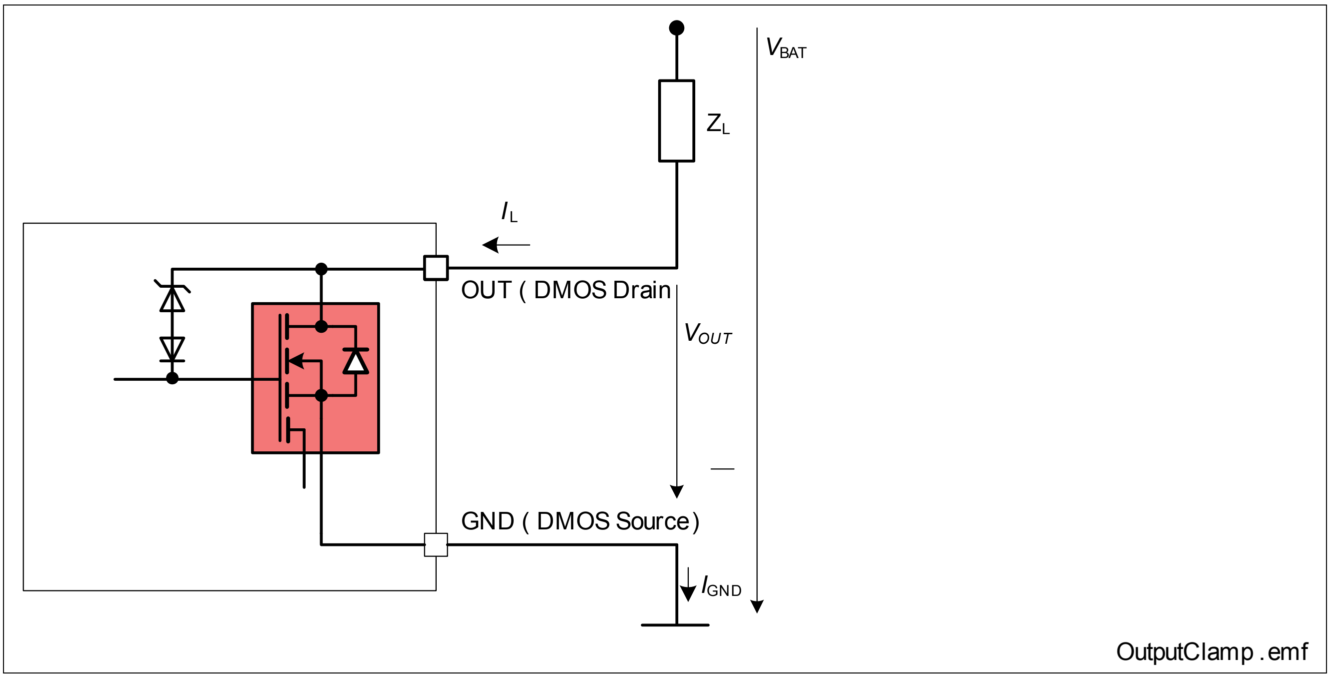


Figure 11 Output Clamp Circuitry

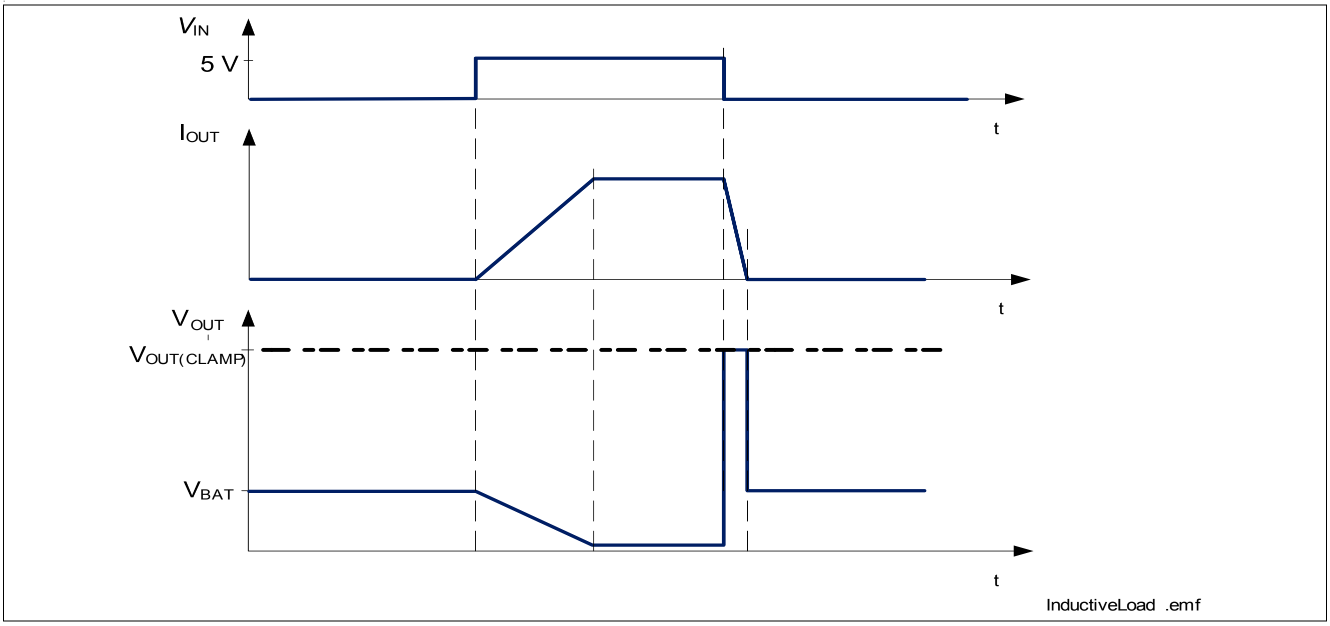


Figure 12 Switching an Inductive Load

5.3.2 Maximum Load Inductance

While demagnetization of inductive loads, energy has to be dissipated in the BTS3060TF.
This energy can be calculated by the following equation:

$$E = V_{\mathrm{OUT(CLAMP)}} \cdot \left[\frac{V_{\mathrm{BAT}} - V_{\mathrm{OUT(CLAMP)}}}{R_{\mathrm{L}}} \cdot \ln\left(1 - \frac{R_{\mathrm{L}} \cdot I_{\mathrm{L}}}{V_{\mathrm{BAT}} - V_{\mathrm{OUT(CLAMP)}}}\right) + I_{\mathrm{L}}\right] \cdot \frac{L}{R_{\mathrm{L}}}$$

Following equation simplifies under assumption of $R_{\mathrm{L}} = 0$

$$E = \frac{1}{2} L I_{\mathrm{L}}^{2} \cdot \left(1 - \frac{V_{\mathrm{BAT}}}{V_{\mathrm{BAT}} - V_{\mathrm{OUT(CLAMP)}}}\right)$$

Figure 13 shows the inductance / current combination the BTS3060TF can handle.

For maximum single avalanche energy please also refer to E_{AS} value in **"Energies" on Page 7**

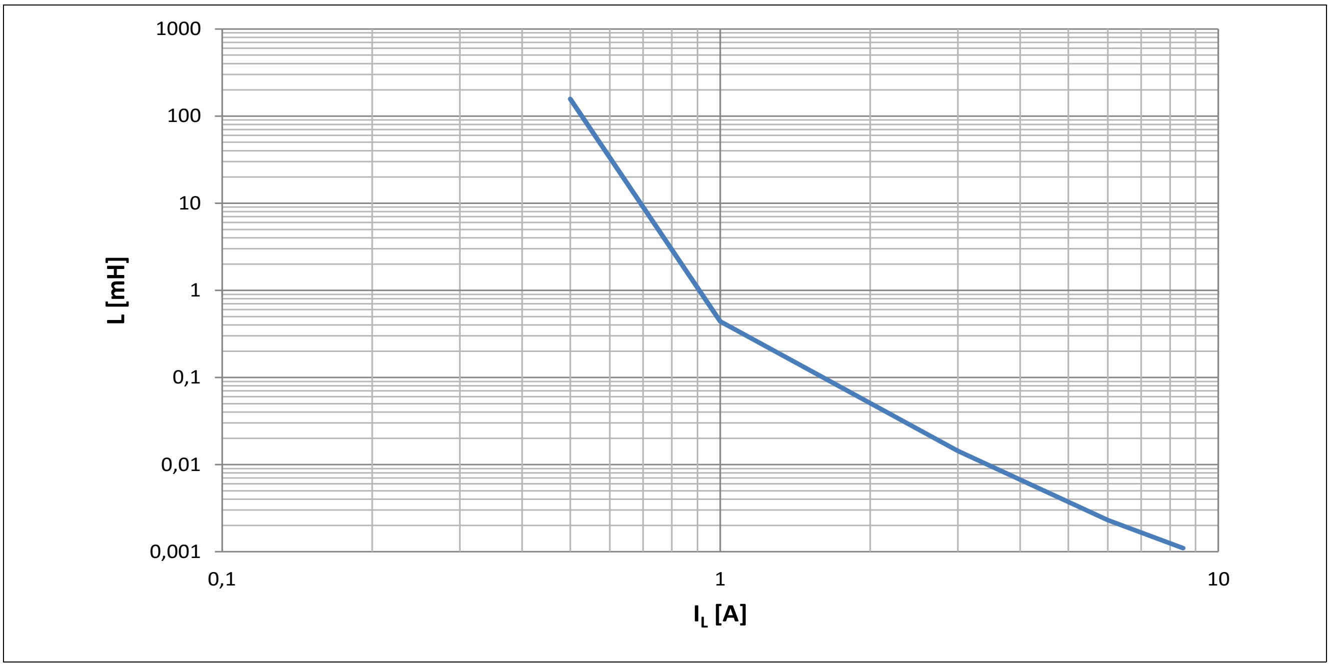


Figure 13 **Maximum load inductance for single pulse**
$L = f\ (I_L)$, $T_{j(0)} = T_{J,\ start} = 150\ °C$, $V_{BAT} = 13.5\ V$

5.4 Reverse Current capability

A reverse battery situation means the OUT pin is pulled below GND potential to $-V_{BAT}$ via the load Z_L.

In this situation the load is driven by a current through the intrinsic body diode of the BTS3060TF and all protection functions, like current limitation, over temperature shut down or over voltage clamping, are not available.

The device is dissipating a power loss which is defined by the driven current and the voltage drop on the DMOS reverse body diode "$-V_{\mathrm{OUT}}$".

5.5 Characteristics

Please see **"Power Stage" on Page 18** for electrical characteristic table.

6 Protection Functions

The device provides embedded protection functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operation.

6.1 Thermal Protection

The device is protected against over temperature due to overload and / or bad cooling conditions. To ensure this a temperature sensor is located in the power MOSFET.

The device incorporates an absolute ($T_{\mathrm{J(SD)}}$) and a dynamic temperature limitation ($\Delta T_{\mathrm{J(SW)}}$). Triggering one of them will cause the output to switch off.

The BTS3060TF has a latching thermal protection function. After the device has switched off due to over temperature the device will stay off even if the temperature drops down.

A protective switch off will be reset by setting the input pin voltage to low for a time longer than t_{RESET}. The next time the voltage on the IN pin rises above the input threshold voltage, the latch will be reset and the device will switch on, if the over temperature protection is no more present or triggered.

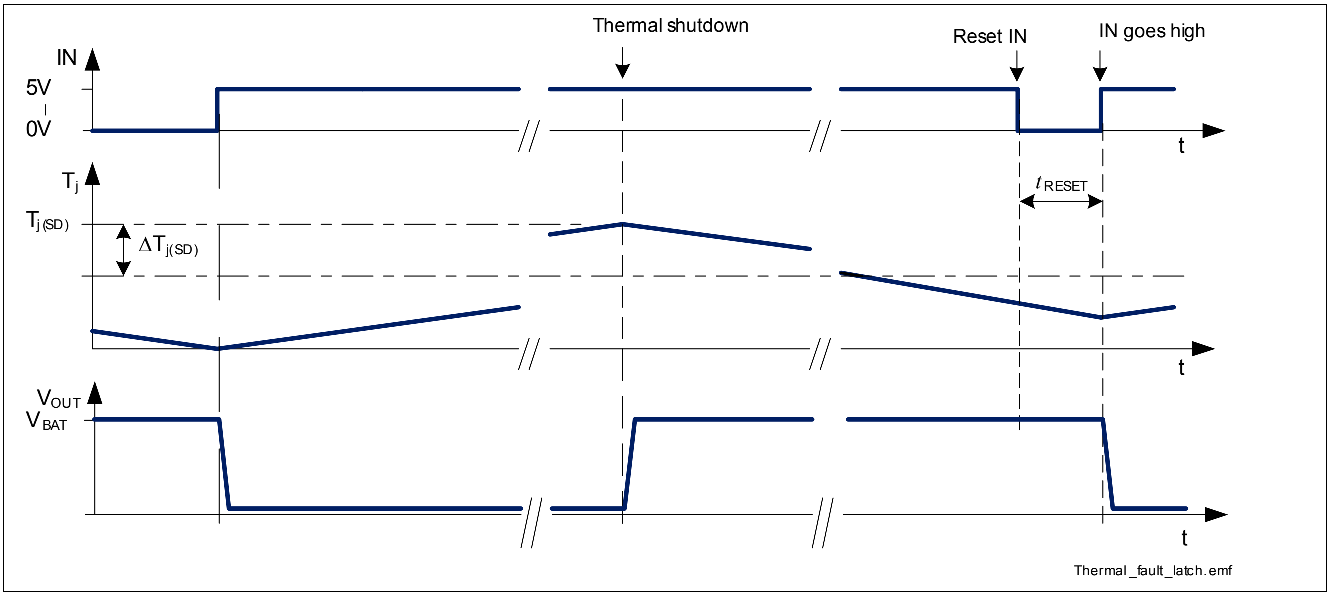


Figure 14 Thermal protective switch OFF scenario

6.2 Short Circuit Protection / Current limitation

The condition short circuit is an overload condition to the device. If the load current reaches the limitation value of $I_{\mathrm{L(LIM)}}$ the device limits the current and starts heating up. When the thermal shutdown temperature is reached, the device turns off.
The time from the beginning of current limitation until the over temperature switch off depends strongly on the cooling conditions.

Figure 15 shows this simplified behavior.

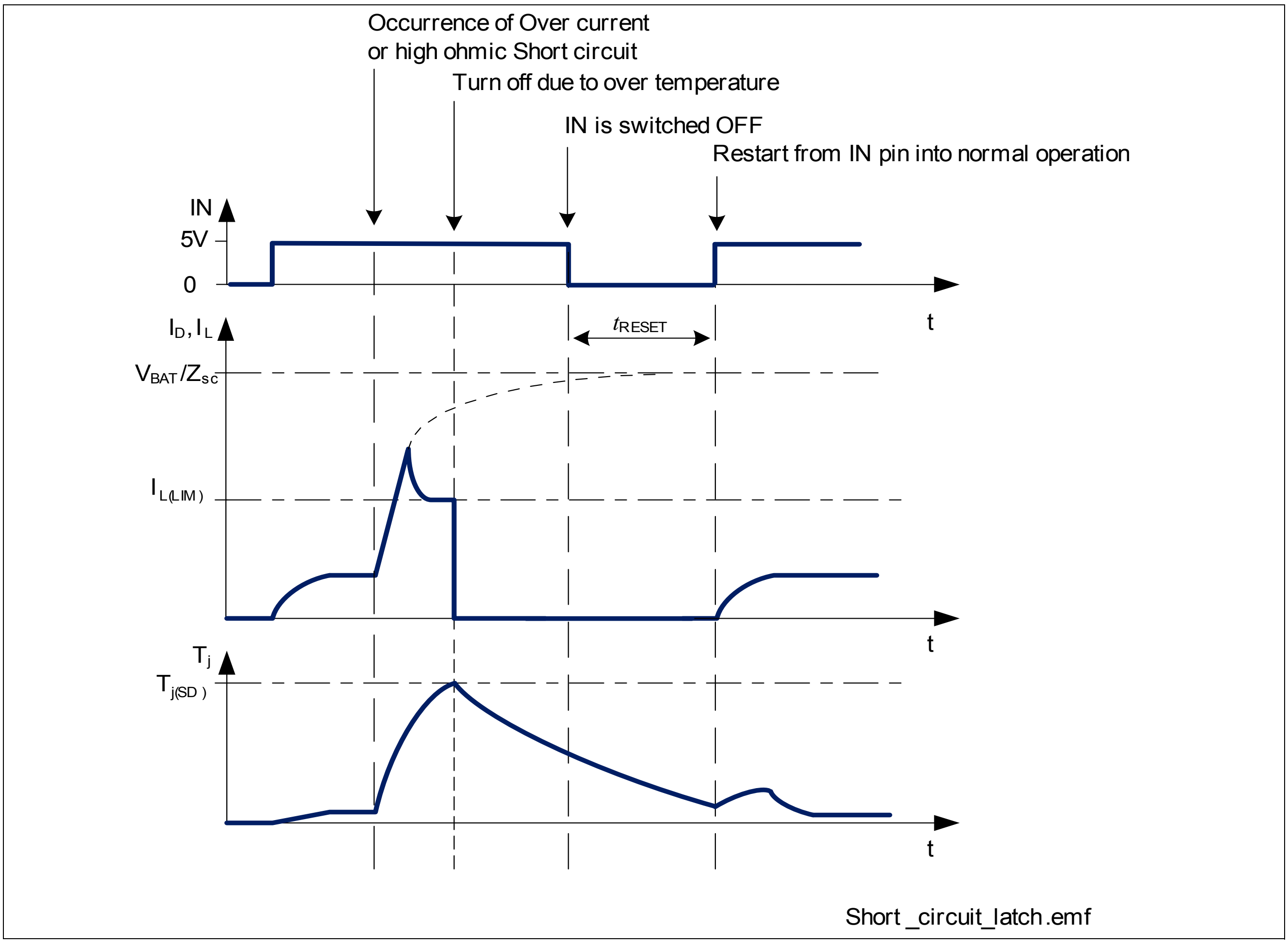


Figure 15 Short circuit protection via current limitation and over temperature switch off

6.3 Characteristics

Please see **"Protection" on Page 19** for electrical characteristic table.

7 Input Stage

7.1 Input Circuit

Figure 16 shows the input circuit of the BTS3060TF. It’s ensured that the device switches off in case of open input pin. A ESD Zener structure protects the input circuit against ESD pulses.

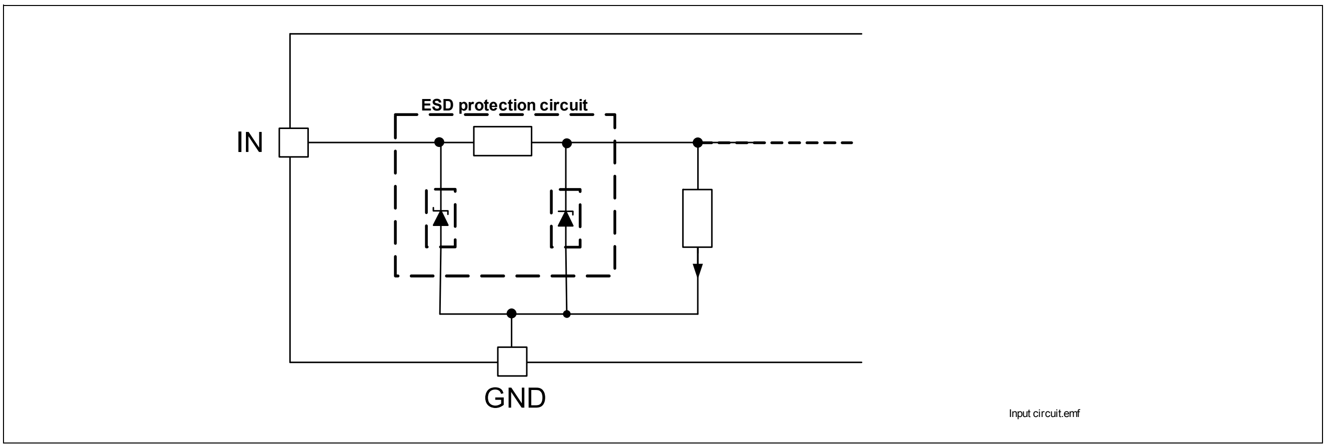


Figure 16 Simplified Input circuitry

7.2 Characteristics

Please see **“Input Stage” on Page 20** for electrical characteristic table.

8 Electrical Characteristics

Note: Characteristics show the deviation of parameter at given input voltage and junction temperature. Typical values show the typical parameters expected from manufacturing and in typical application condition.
All voltages and currents naming and polarity in accordance to
Figure 3 “Naming definition of electrical parameters” on Page 6

8.1 Power Stage

Please see Chapter **“Power Stage” on Page 12** for parameter description and further details.

Table 4 Electrical Characteristics: Power Stage

T_J = -40 °C to +150 °C, V_{BAT} = 8 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Power Stage							
8.1.1	On-State resistance at hot temperature	$R_{DS(ON)\_150}$	–	105	135	mΩ	T_J = 150 °C; V_{IN} = 5 V; I_L = 3.0 A
8.1.2	On-State resistance at ambient temperature	$R_{DS(ON)\_25}$	–	50	–	mΩ	T_J = 25 °C; V_{IN} = 5 V; I_L = 3.0 A
8.1.3	Nominal load current	$I_{L(NOM)}$	–	3	–	A	1) T_J < 150 °C; T_A = 85 °C V_{IN} = 5 V;
8.1.4	OFF state load current	$I_{L(OFF)}$	–	–	2	µA	2) V_{BAT} = 13.5 V; V_{IN} = 0 V; T_J ≤ 85 °C
			–	–	4	µA	V_{BAT} = 18 V; V_{IN} = 0 V; T_J = 150 °C
8.1.5	Reverse body diode forward voltage drop	$-V_{OUT}$	–	0.8	1.5	V	I_D = -3.0 A; V_{IN} = 0 V

Table 4 Electrical Characteristics: Power Stage (cont'd)

T_J = -40 °C to +150 °C, V_{BAT} = 8 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Dynamic characteristics - switching **V_{BAT} = 13.5 V, R_L = 4.7 Ω; single pulse** see *Figure 10 "Definition of Power Output Timing for Resistive Load" on Page 12* *for definition details*							
8.1.6	Turn-on time	t_{ON}	12	38	76	µs	V_{IN} = 0V to 5V; V_{OUT} = 10% V_{BAT}
8.1.7	Turn-on delay time	t_{DON}	2	8	16	µs	V_{IN} = 0 V to 5V; V_{OUT} = 90% V_{BAT}
8.1.8	Fall time, Falling output voltage	t_F	10	30	60	µs	V_{IN} = 0V to 5V; V_{OUT} = 90% V_{BAT} to V_{OUT} = 10% V_{BAT}
8.1.9	Turn-off time	t_{OFF}	20	65	130	µs	V_{IN} = 5 V to 0V; V_{OUT} = 90% V_{BAT}
8.1.10	Turn-off delay time	t_{DOFF}	10	35	70	µs	V_{IN} = 5 V to 0V; V_{OUT} = 10% V_{BAT}
8.1.11	Rise time, Rising output voltage	t_R	10	30	60	µs	V_{IN} = 5V to 0V; V_{OUT} = 10% V_{BAT} to V_{OUT} = 90% V_{BAT}
8.1.12	Rise time to fall time delta	t_R - t_F	–	0	–	µs	–
8.1.13	Rise time/Fall time factor	t_R / t_F	–	1	–	–	–
8.1.14	Turn-on Slew rate 3)	$-(\Delta V/\Delta t)_{ON}$	–	0.85	–	V/µs	V_{OUT} = 90% V_{BAT} to V_{OUT} = 50% V_{BAT}
8.1.15	Turn-off Slew rate 3)	$(\Delta V/\Delta t)_{OFF}$	–	0.85	–	V/µs	V_{OUT} = 50% V_{BAT} to V_{OUT} = 90% V_{BAT}

1) Not subject to production test, calculated by R_{thJA} and $R_{DS(on)}$.
2) Not subject to production test, specified by design
3) calculated value

8.2 Protection

Please see Chapter **"Protection Functions" on Page 15** for parameter description and further details.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation

Table 5 Electrical Characteristics: Protection

T_J = -40 °C to +150 °C, V_{BAT} = 8 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Thermal Protection							
8.2.1	Thermal shut down junction temperature	$T_{j(SD)}$	150	175	–	°C	[1], V_{IN} > 2.7 V
8.2.2	Dynamic temperature limitation/shutdown	$\Delta T_{J(SW)}$	–	70	–	K	[1]
8.2.3	minimum latch reset time	t_{RESET}	50	–	–	µs	[1]; $V_{IN} < 0.8$ V; DMOS is off, no over temperature, pulse times above to assure reset of latch
Overvoltage Protection							
8.2.4	Drain clamp voltage	$V_{OUT(CLAMP)}$	42	45	49	V	V_{IN} = 0 V; I_D = 10 mA
Current limitation							
8.2.5	Current limitation	$I_{L(LIM)}$	10.5	15	20	A	V_{IN} = 5 V; *see also* ***Figure 15***

1) Not subject to production test, specified by design.

8.3 Input Stage

Please see Chapter **"Input Stage" on Page 17** for description and further details.

Table 6 Electrical Characteristics: Input

T_J = -40 °C to +150 °C, V_{BAT} = 8 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Input							
8.3.1	Input Current, normal operation	$I_{IN(NOM)}$	–	310	400	µA	2.7 < V_{IN} < 5.5 V; DC operation normal, no fault
8.3.1	Input Current, protection latched	$I_{IN(PROT)}$	–	320	–	µA	2.7 < V_{IN} < 5.5 V; latched fault; [1]
8.3.2	Input Voltage on-threshold	$V_{IN(TH)}$	0.8	1.9	2.5	V	I_D = 1 mA; Power DMOS active

1) Not subject to production test, specified by design.

9 Characterisation Results

Typical performance characteristics

9.1 Power Stage

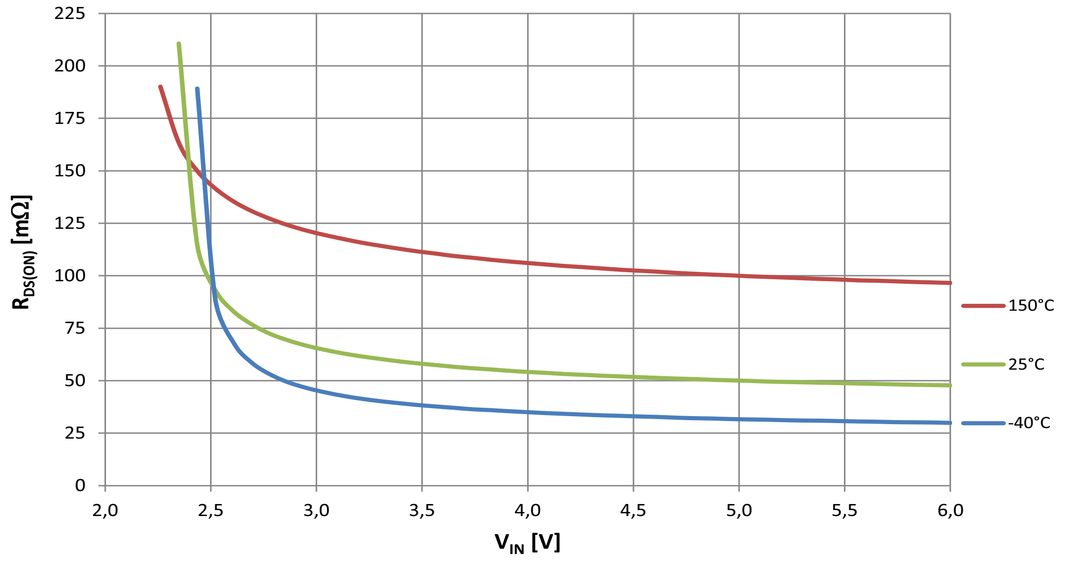


Figure 17 **Typical$R_{DS(ON)}$ vs. V_{IN} @ T_J=-40, 85, 150°C, I_L=3A**

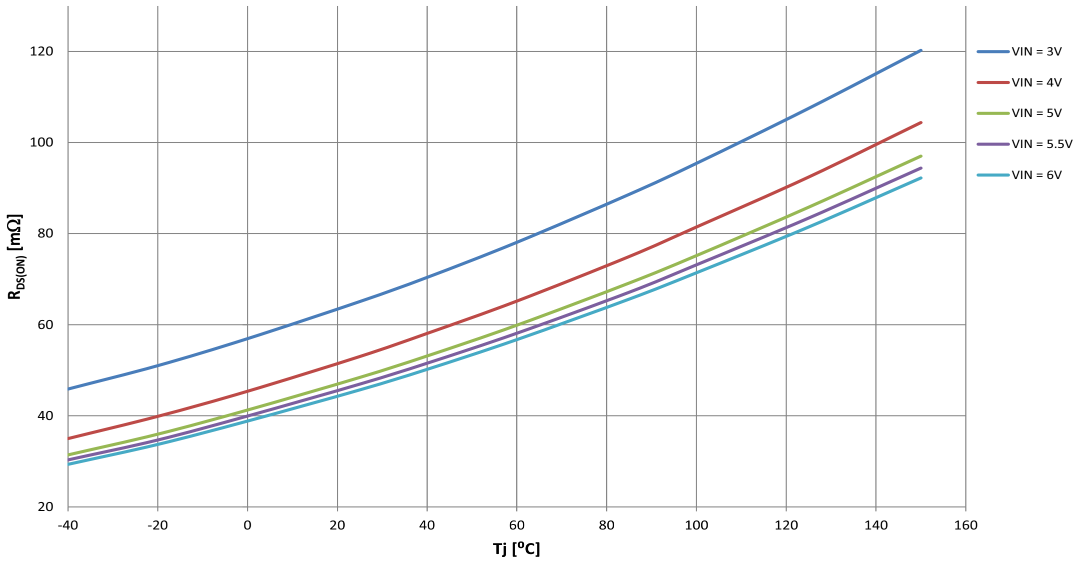


Figure 18 **Typical $R_{DS(ON)}$ vs. T_J @ V_{IN}= 3V, 4V, 5V, 5.5V, 6V, I_L=3A**

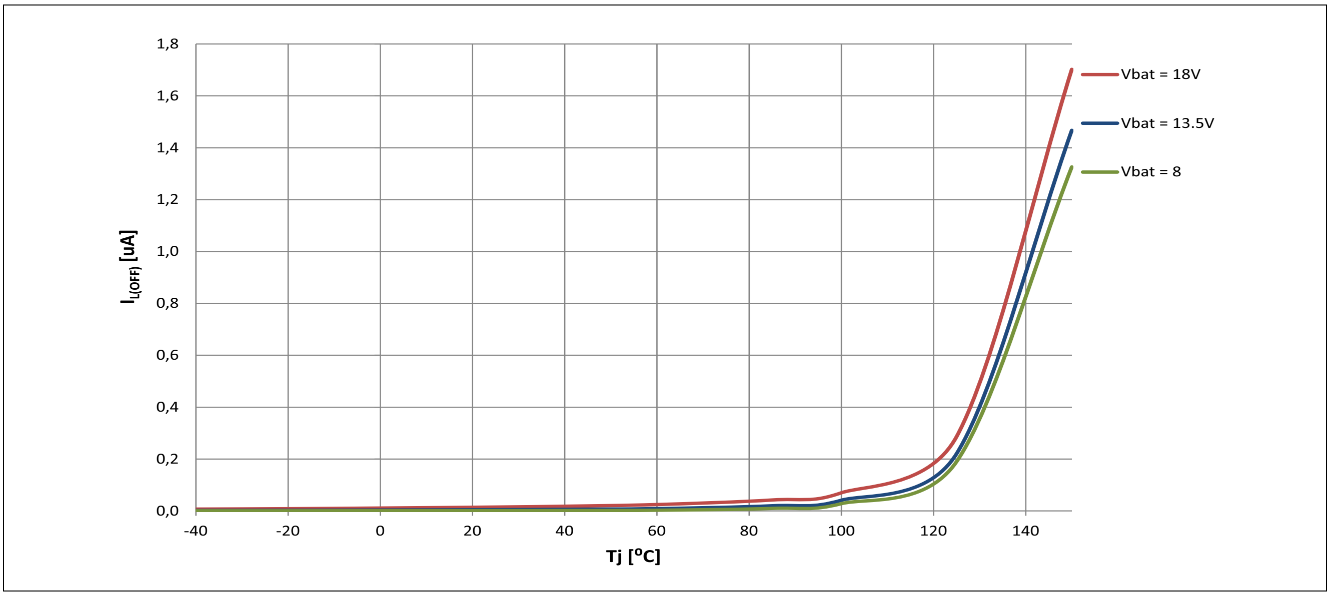


Figure 19 Typical $I_{L(OFF)}$ vs. Tj @ V_{BAT} = 8V, 13.5V, 18V

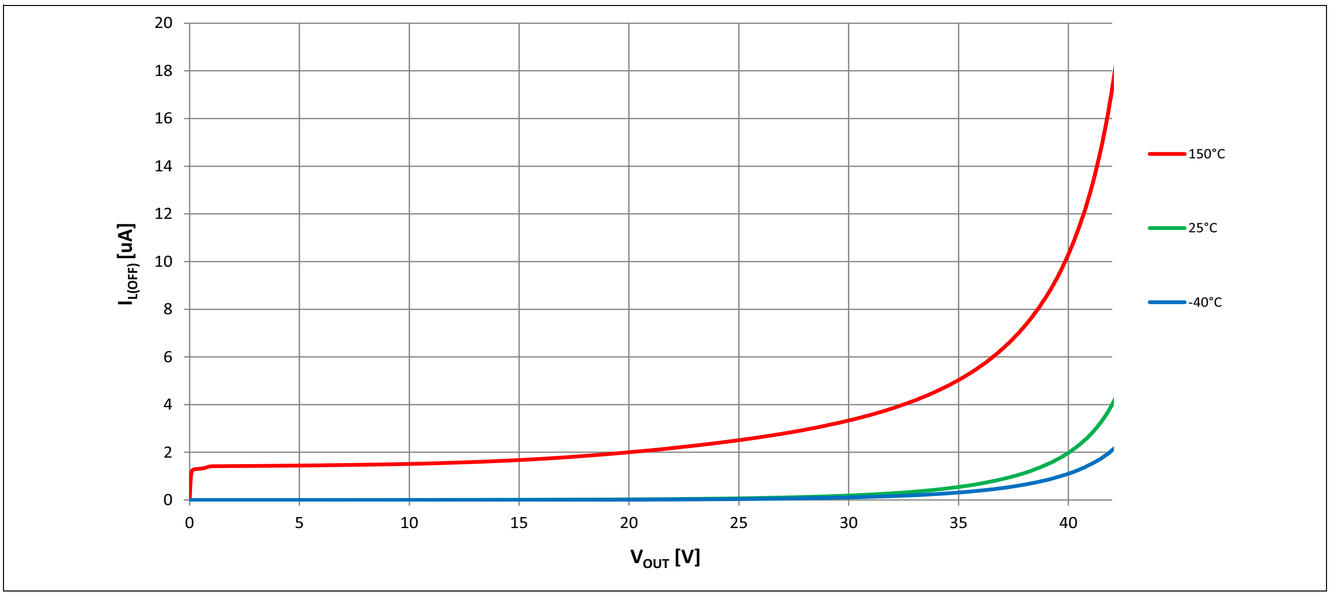


Figure 20 Typical $I_{L(OFF)}$ vs. V_{OUT} (0..40V) @ Tj = -40, 25, 150°C, V_{IN}=0V

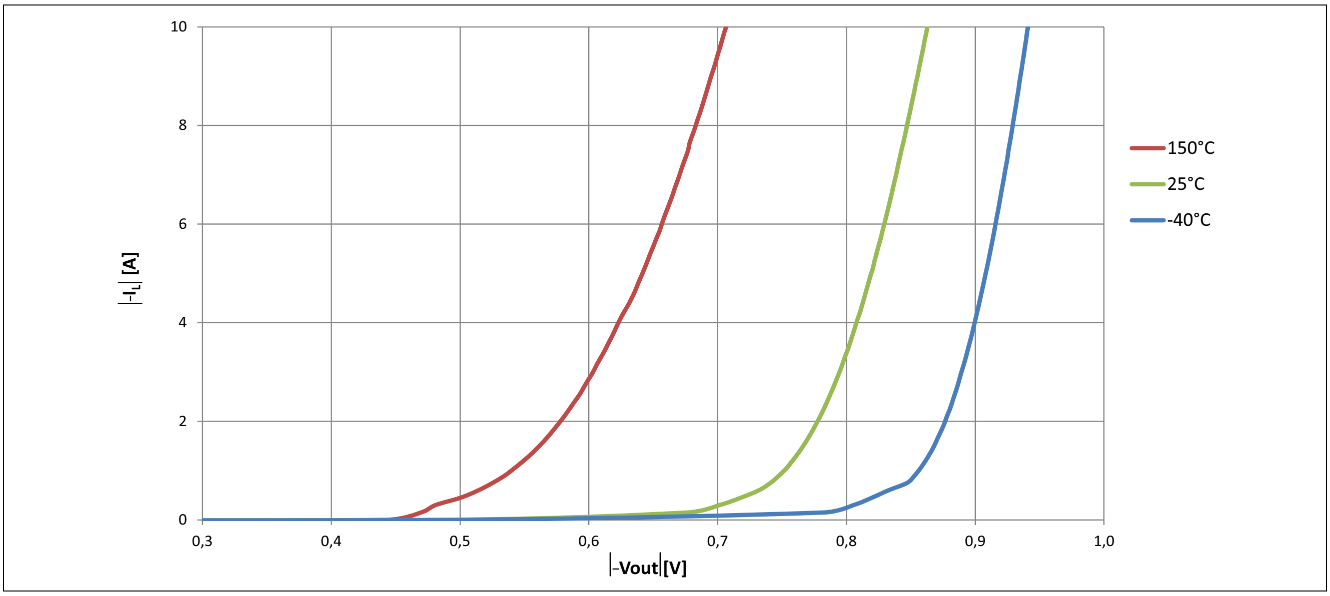


Figure 21 Typical -I_L vs.-V_{OUT} @ Tj=-40, 25, 150°C in absolute values.

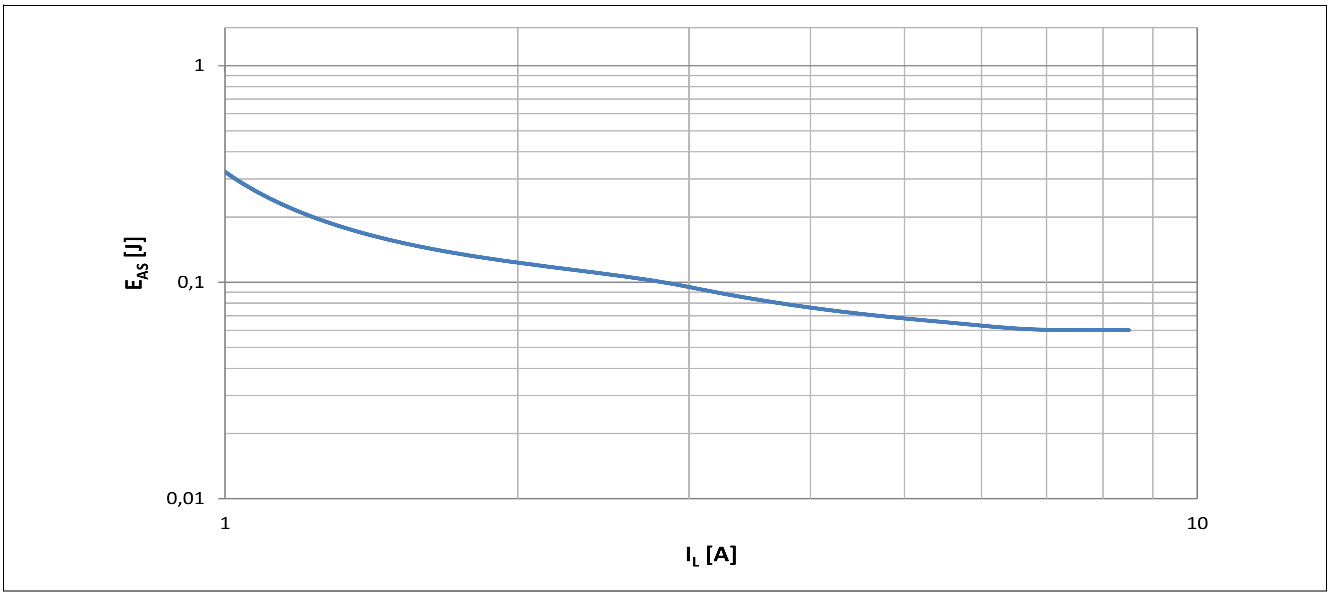


Figure 22 Maximum E_{AS} vs. I_L @ V_{BAT} = 13.5V, Tj=150°C

Dynamic charactersitics:

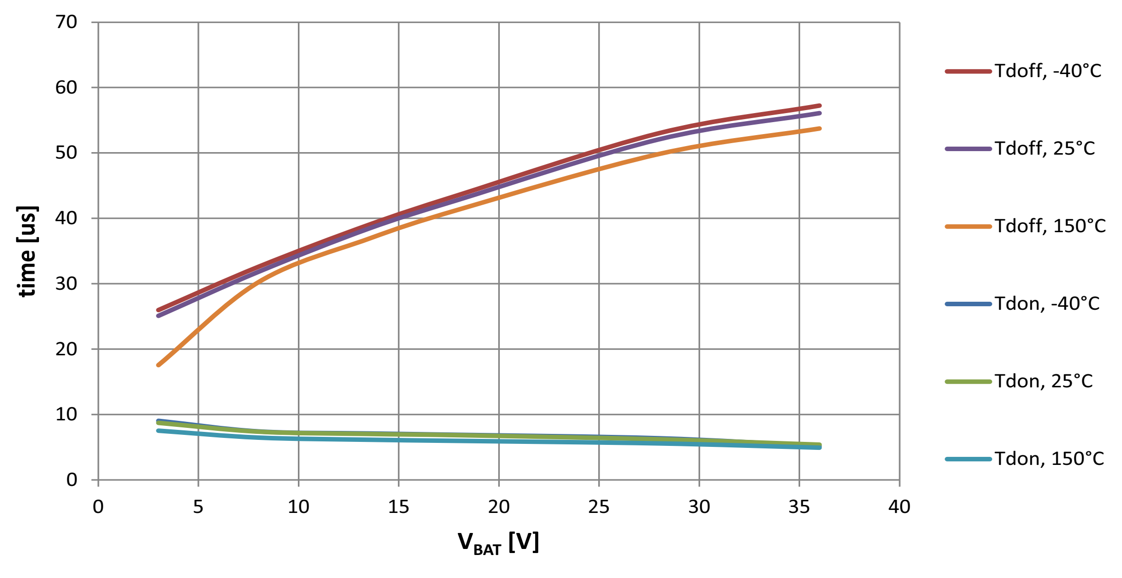


Figure 23 Typical delay on time, delay off time vs. V_{BAT} @ V_{IN}=5V, I_L=3A, Tj=-40, 25, 150°C

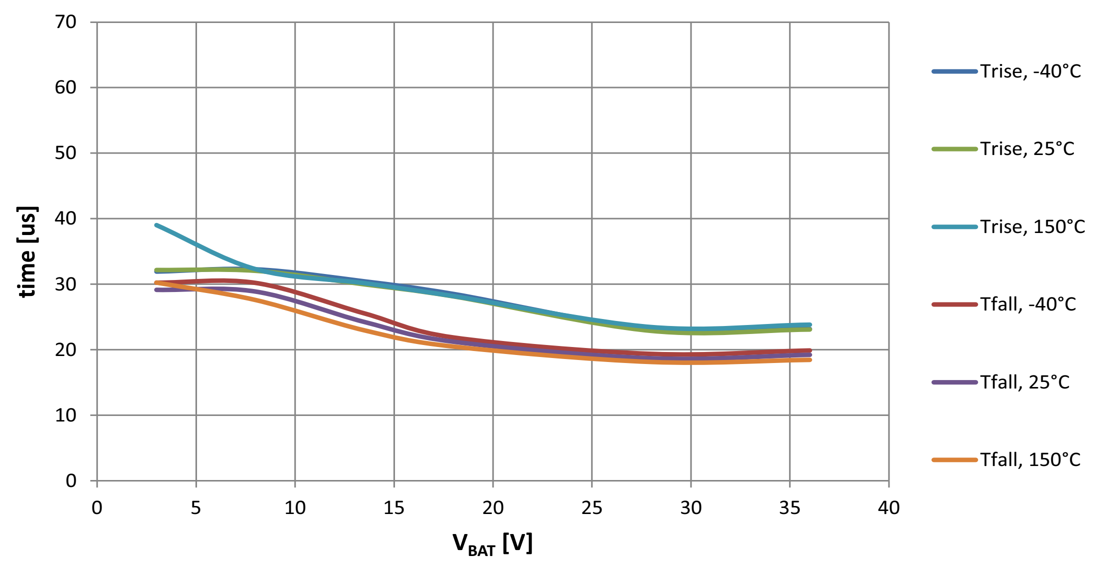


Figure 24 Typical rise time, fall time vs. V_{BAT} @ V_{IN}=5V, I_L=3A, Tj=-40, 25, 150°C

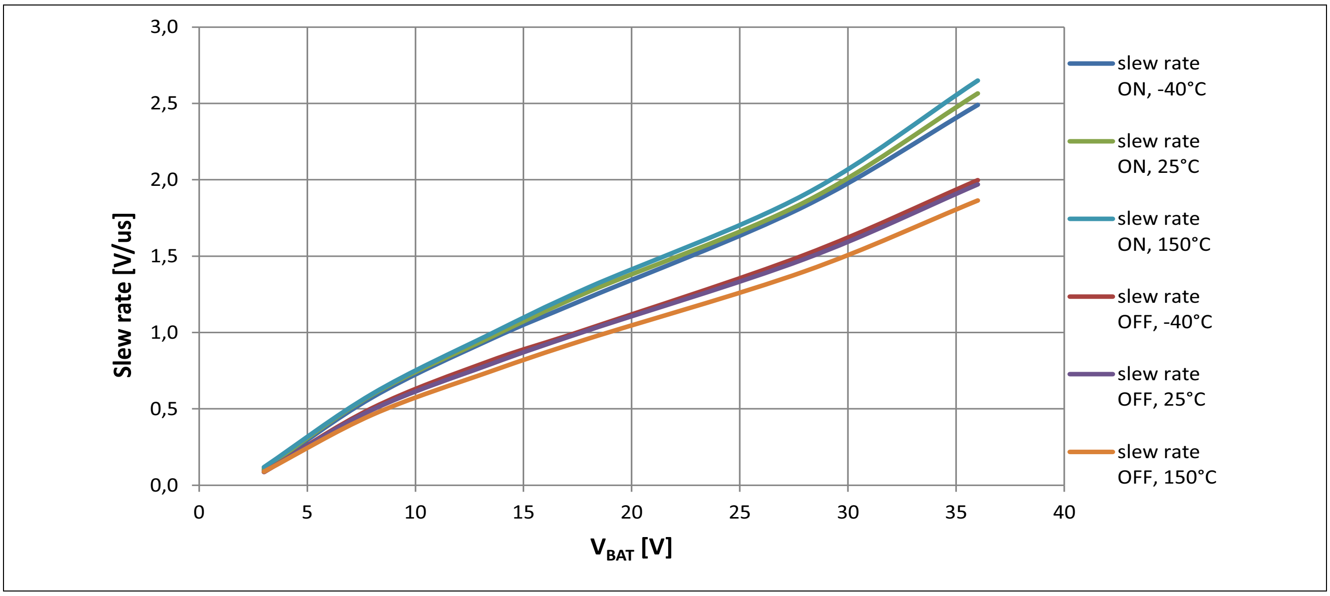


Figure 25 Typical slew rate vs. V_{BAT} @ V_{IN}=5V, I_L=3A, Tj=-40, 25, 150°C

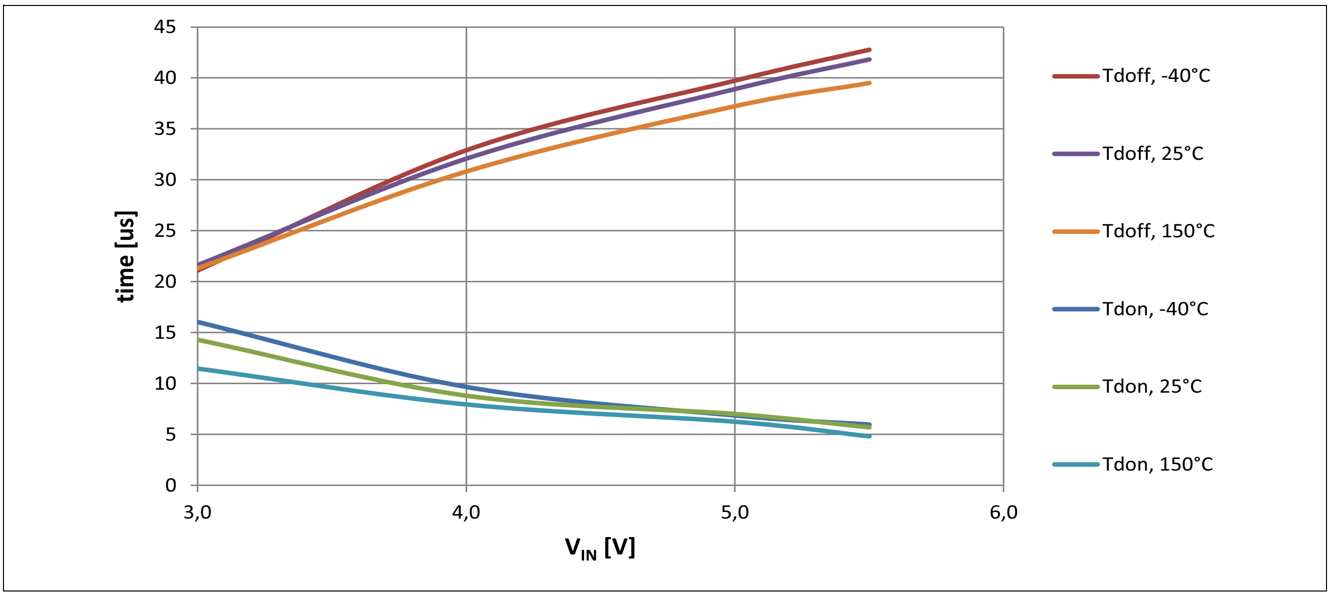


Figure 26 Typical delay on time, delay off time vs. V_{IN} @ V_{BAT}=13.5, R_L=4.5 Ohm, Tj=-40, 25, 150°C

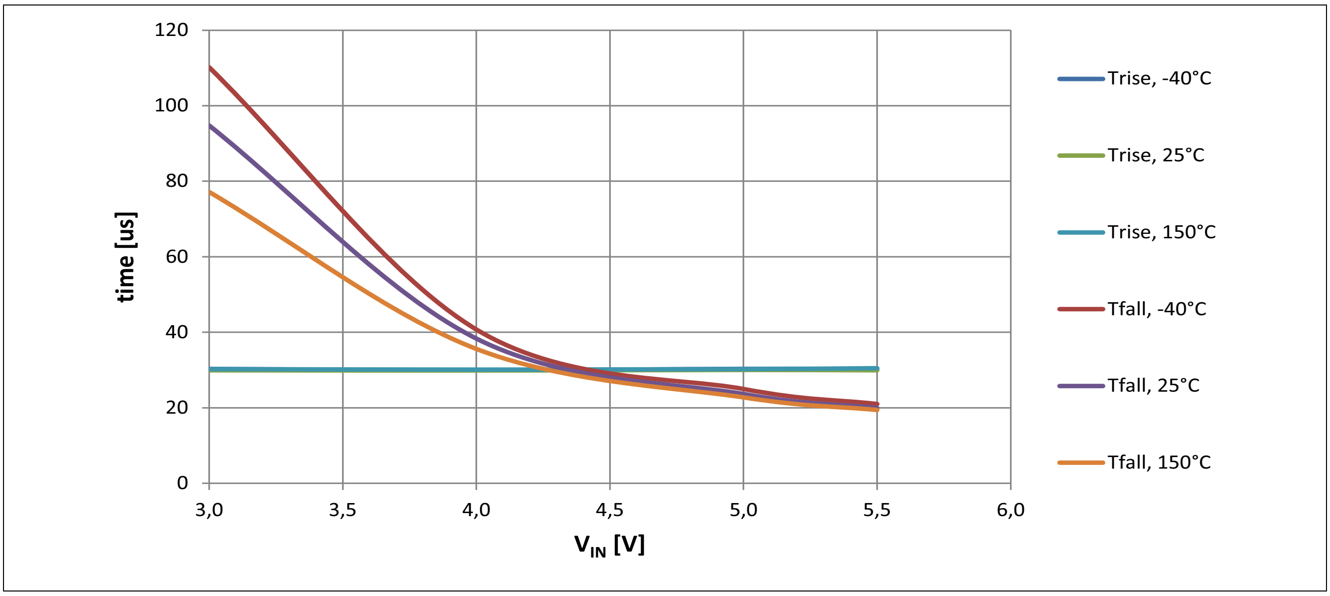


Figure 27 Typical turn on time, turn off time vs. V_{IN} @ V_{BAT}=13.5, R_L=4.5 Ohm, Tj=-40, 25, 150°C

9.2 Protection

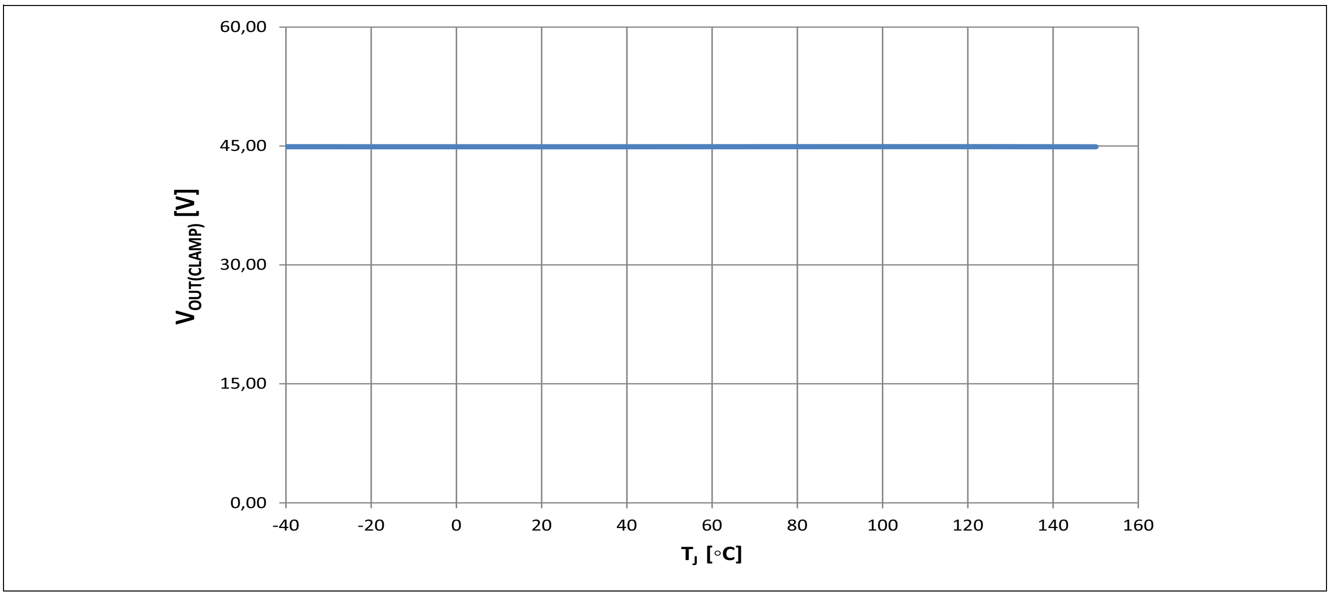


Figure 28 Typical $V_{OUT(CLAMP)}$ vs. Tj

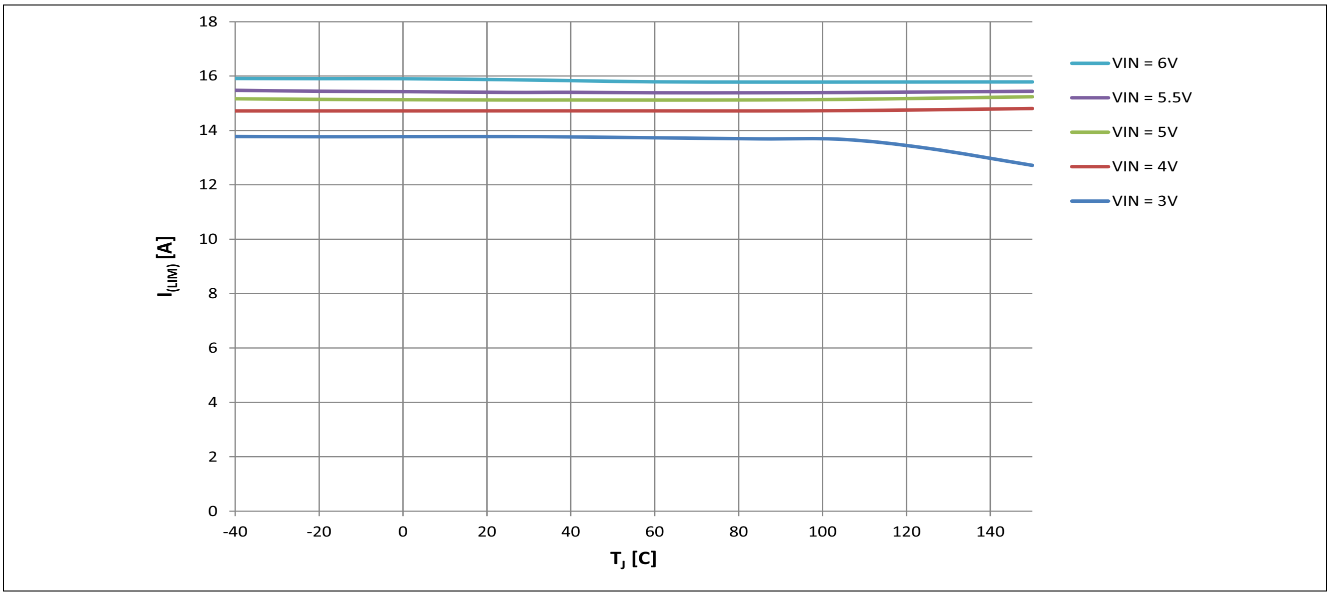


Figure 29 Typical $I_{L(LIM)}$ vs. Tj @ V_{IN}= 3V, 4V, 5V, 5.5V, 6V

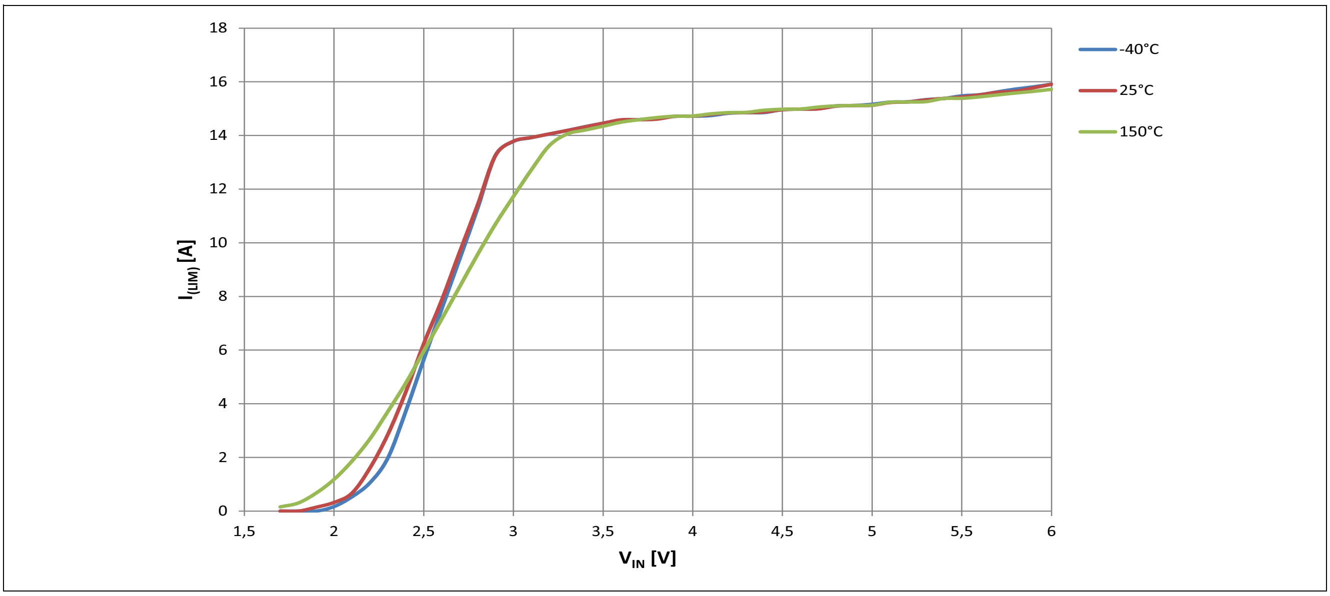


Figure 30 Typical $I_{L(LIM)}$ vs. V_{IN} @ Tj = -40°C, 25°C, 150°C

9.3 Input Stage

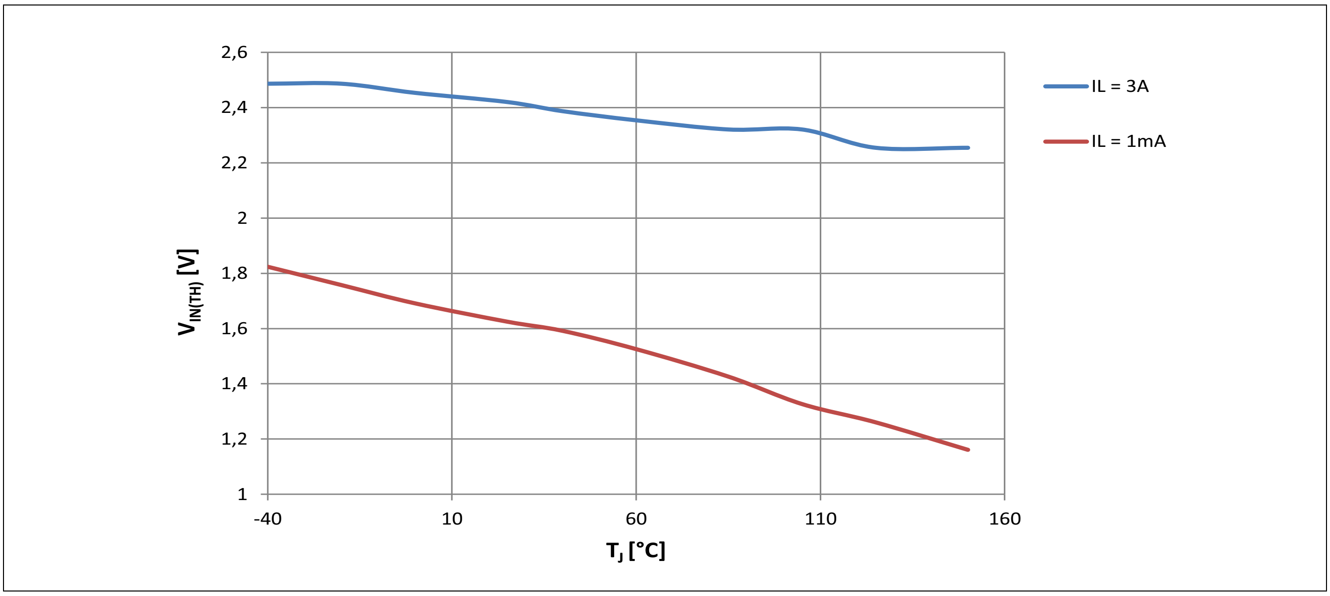


Figure 31 Typical $V_{IN(TH)}$ vs. Tj @ I_L = 3A, 1mA

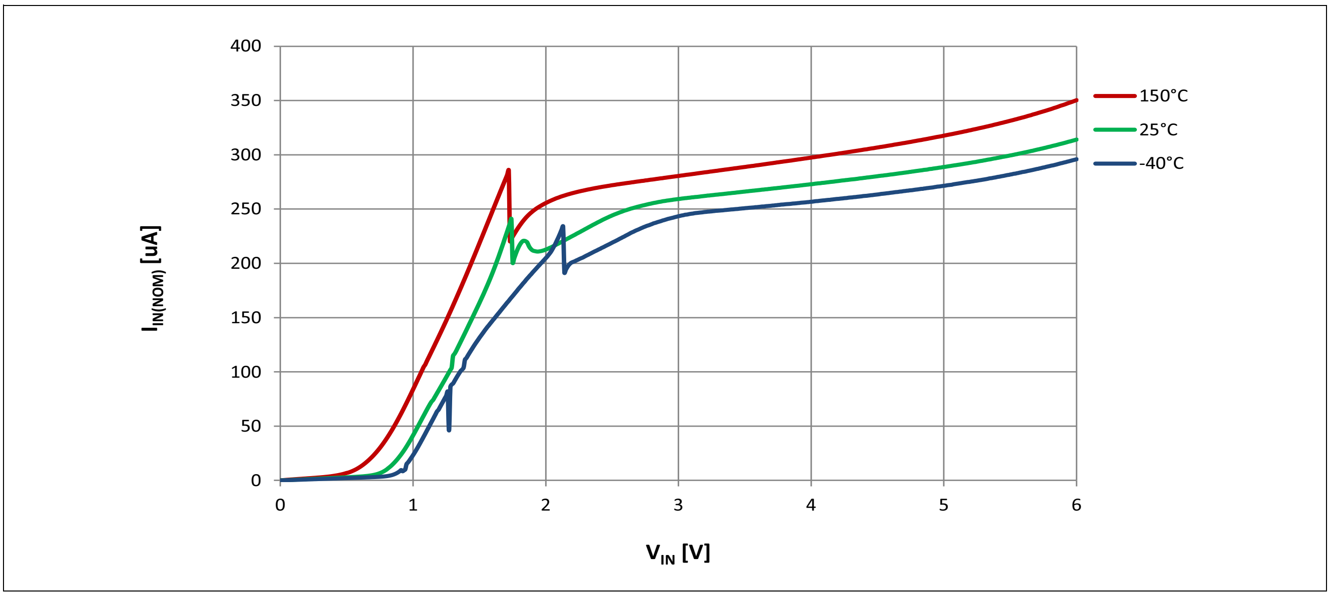


Figure 32 Typical $I_{IN(NOM)}$ vs. V_{IN} @ Tj = -40°C, 25°C, 150°C

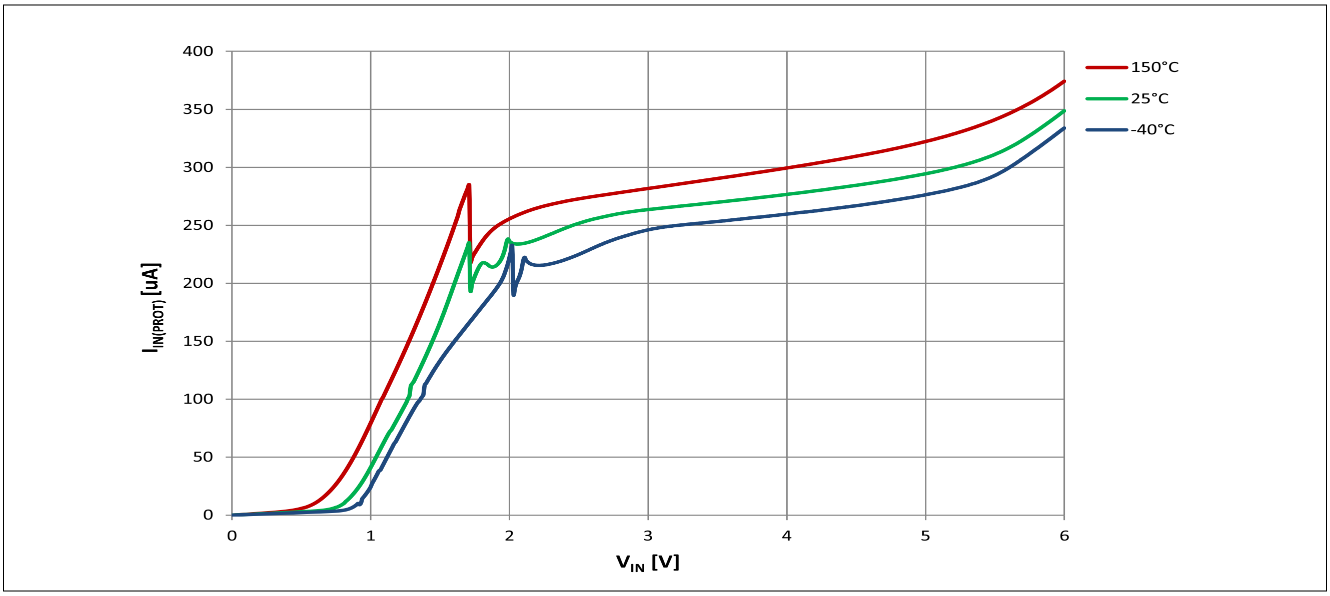


Figure 33 Typical $I_{IN(PROT)}$ vs. V_{IN} @ Tj = -40°C, 25°C, 150°C

10 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

10.1 Application Diagram

An application example with the BTS3060TF is shown below.

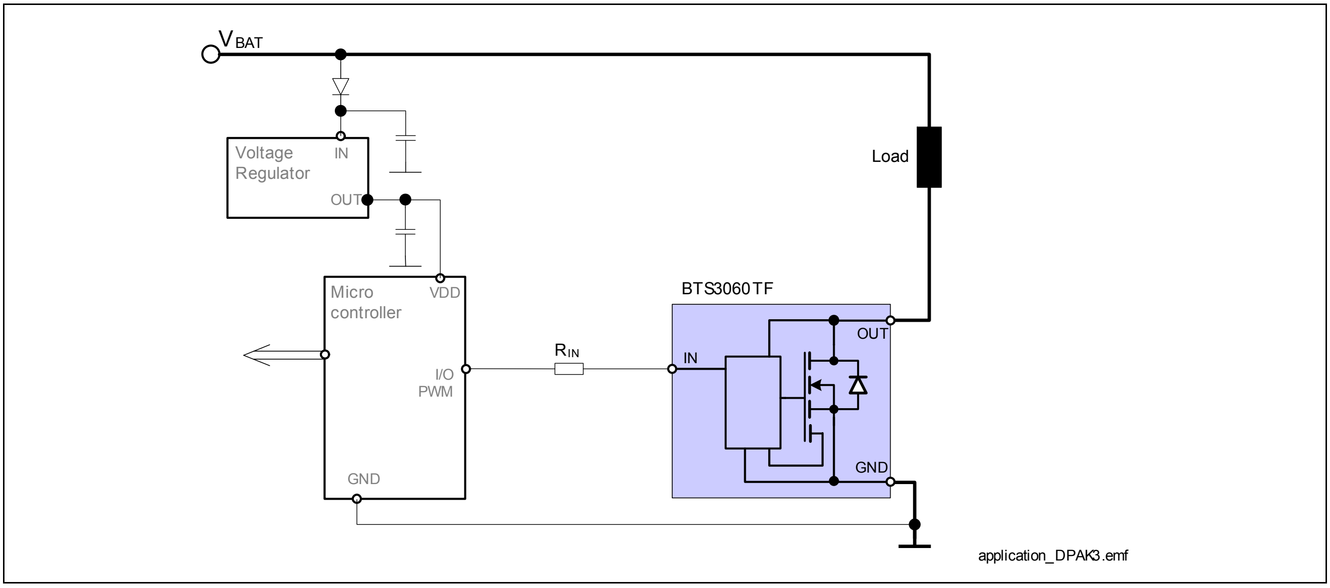
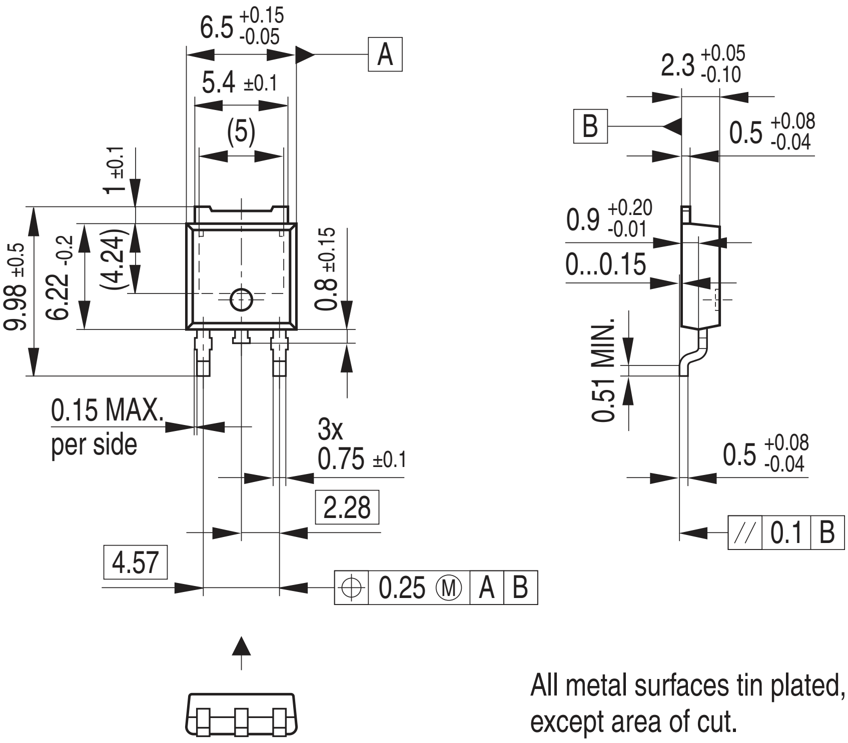


Figure 34 Application example circuitry

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

11 Package Outlines BTS3060TF



All metal surfaces tin plated, except area of cut.

GPT09277

PG-TO252-3 (Transistor Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

12 Revision History

Version	Date	Changes
Rev 1.0	2014-07-21	Datasheet released

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