S-576Z B Series

125°C OPERATION, HIGH-WITHSTAND VOLTAGE, HIGH-SPEED, ZCL™ HALL EFFECT IC

www.ablic.com

Rev.1.1_00

This IC, developed by CMOS technology, is a high-accuracy Hall effect IC that operates with high temperature and high-withstand voltage.
The IC switches output voltage level when the IC detects magnetic flux density (magnetic field) polarity changes. The ZCL (Zero Crossing Latch) detection method realizes polarity changes detection with the higher accuracy than the conventional bipolar latch method. Using this IC with a magnet makes it possible to detect the rotation status in various devices.

ABLIC Inc. offers a "magnetic simulation service" that provides the ideal combination of magnets and our Hall effect ICs for customer systems. Our magnetic simulation service will reduce prototype production, development period and development costs. In addition, it will contribute to optimization of parts to realize high cost performance.
For more information regarding our magnetic simulation service, contact our sales representatives.

■ Features

- Uses a thin (t0.80 mm max.) TSOT-23-3S or ultra-thin (t0.50 mm max.) HSNT-6(2025) package, allowing for device miniaturization
- Contributes to reduction of mechanism operation dispersion through high accuracy detection of magnetic flux density (magnetic field) polarity changes
- Contributes to device safe design with a built-in output current limit circuit

■ Specifications

- Pole detection: ZCL detection
- Output logic*1: V_{OUT} = "L" at S pole detection
  V_{OUT} = "H" at S pole detection
- Output form*1: Nch open-drain output
  Nch driver + built-in pull-up resistor (1.2 kΩ typ.)
- Zero crossing latch point: B_Z = 0.0 mT typ.
- Release point (S pole)*1: B_{RS} = 3.0 mT typ.
  B_{RS} = 6.0 mT typ.
- Chopping frequency: f_C = 500 kHz typ.
- Output delay time: t_D = 8.0 µs typ.
- Power supply voltage range*2: V_{DD} = 2.7 V to 26.0 V
- Built-in regulator
- Built-in output current limit circuit
- Operation temperature range: Ta = −40°C to +125°C
- Lead-free (Sn 100%), halogen-free

■ Applications

- DC brushless motor
- Home appliance
- Housing equipment
- Industrial equipment

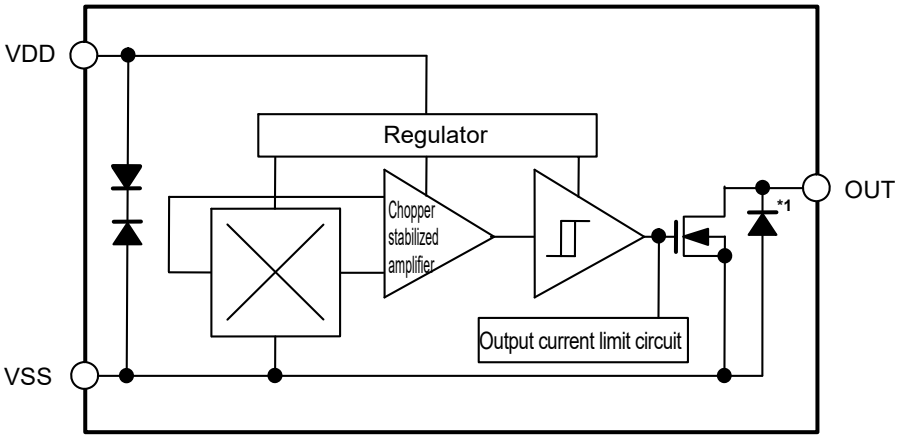
■ Packages

- TSOT-23-3S
- HSNT-6(2025)

***1.** The option can be selected.
***2.** V_{DD} = 2.7 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (1.2 kΩ typ.)

■ Block Diagrams

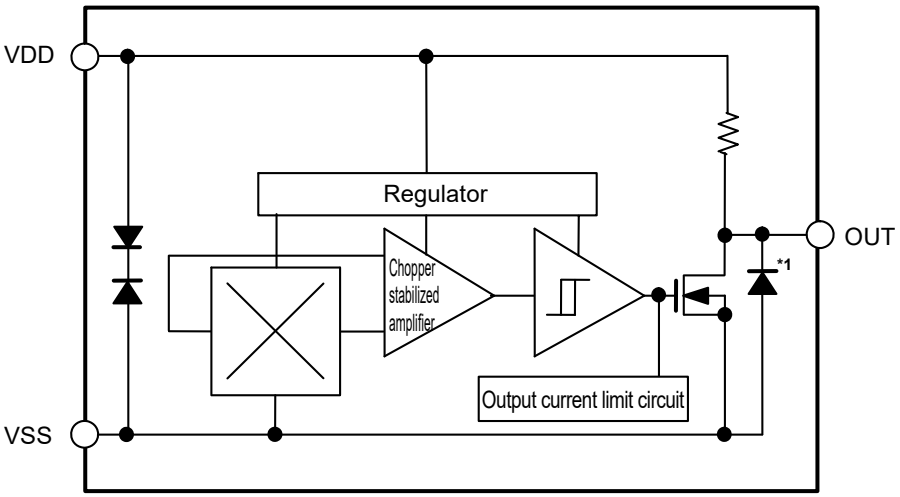
1. Nch open-drain output product



***1.** Parasitic diode

Figure 1

2. Nch driver + built-in pull-up resistor product



***1.** Parasitic diode

Figure 2

■ Product Name Structure

1. Product name

S-576Z x x x B - xxxx U

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- Package abbreviation and IC packing specifications*1
  - L3T2: TSOT-23-3S, Tape
  - A6T8: HSNT-6(2025), Tape
- Operation temperature
  - B: Ta = –40°C to +125°C
- Release point (S pole)
  - 1: B_{RS} = 3.0 mT typ.
  - 2: B_{RS} = 6.0 mT typ.
- Output logic
  - L: V_{OUT} = "L" at S pole detection
  - H: V_{OUT} = "H" at S pole detection
- Output form
  - N: Nch open-drain output
  - 1: Nch driver + built-in pull-up resistor (1.2 kΩ typ.)

***1.** Refer to the tape drawing.

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land	Stencil Opening
TSOT-23-3S	MP003-E-P-SD	MP003-E-C-SD	MP003-E-R-SD	–	–
HSNT-6(2025)	PJ006-B-P-SD	PJ006-B-C-SD	PJ006-B-R-SD	PJ006-B-LM-SD	PJ006-B-LM-SD

3. Product name list

3. 1 TSOT-23-3S

Table 2

Product Name	Output Form	Power Supply Voltage Range	Output Logic	Release Point (S pole) (B_{RS})
S-576ZNL1B-L3T2U	Nch open-drain output	V_{DD} = 2.7 V to 26.0 V	V_{OUT} = "L" at S pole detection	3.0 mT typ.
S-576Z1L1B-L3T2U	Nch driver + built-in pull-up resistor (1.2 kΩ typ.)	V_{DD} = 2.7 V to 5.5 V	V_{OUT} = "L" at S pole detection	3.0 mT typ.

Remark Please contact our sales representatives for products other than the above.

3. 2 HSNT-6(2025)

Table 3

Product Name	Output Form	Power Supply Voltage Range	Output Logic	Release Point (S pole) (B_{RS})
S-576ZNL1B-A6T8U	Nch open-drain output	V_{DD} = 2.7 V to 26.0 V	V_{OUT} = "L" at S pole detection	3.0 mT typ.
S-576Z1L1B-A6T8U	Nch driver + built-in pull-up resistor (1.2 kΩ typ.)	V_{DD} = 2.7 V to 5.5 V	V_{OUT} = "L" at S pole detection	3.0 mT typ.

Remark Please contact our sales representatives for products other than the above.

■ Pin Configurations

1. TSOT-23-3S

Top view

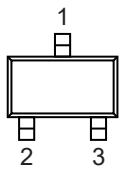


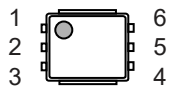
Figure 3

Table 4

Pin No.	Symbol	Description
1	VSS	GND pin
2	VDD	Power supply pin
3	OUT	Output pin

2. HSNT-6(2025)

Top view



Bottom view

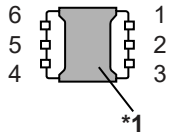


Figure 4

Table 5

Pin No.	Symbol	Description
1	VDD	Power supply pin
2	NC*2	No connection
3	OUT	Output pin
4	NC*2	No connection
5	VSS	GND pin
6	NC*2	No connection

***1.** Connect the heatsink of backside at shadowed area to the board, and set electric potential open or GND. However, do not use it as the function of electrode.

***2.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

■ Absolute Maximum Ratings

Table 6

Item		Symbol	Absolute Maximum Rating	Unit
Power supply voltage	Nch open-drain output product	V_{DD}	V_{SS} – 0.3 to V_{SS} + 28.0	V
	Nch driver + built-in pull-up resistor (1.2 kΩ typ.) product		V_{SS} – 0.3 to V_{SS} + 9.0	V
Power supply current		I_{DD}	±10	mA
Output current		I_{OUT}	±10	mA
Output voltage	Nch open-drain output product	V_{OUT}	V_{SS} – 0.3 to V_{SS} + 28.0	V
	Nch driver + built-in pull-up resistor (1.2 kΩ typ.) product		V_{SS} – 0.3 to V_{DD} + 0.3	V
Operation ambient temperature		T_{opr}	–40 to +125	°C
Storage temperature		T_{stg}	–40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 7

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	TSOT-23-3S	Board A	–	225	–	°C/W
			Board B	–	190	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W
		HSNT-6(2025)	Board A	–	180	–	°C/W
			Board B	–	128	–	°C/W
			Board C	–	43	–	°C/W
			Board D	–	44	–	°C/W
			Board E	–	36	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. Nch open-drain output product

Table 8

(Ta = +25°C, V_{DD} = 12.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–	2.7	12.0	26.0	V	–
Current consumption	I_{DD}	–	–	4.0	4.5	mA	1
Low level output voltage	V_{OL}	I_{OUT} = 5 mA, V_{OUT} = "L"	–	–	0.4	V	2
Leakage current	I_{LEAK}	V_{OUT} = "H"	–	–	1.0	μA	3
Output limit current	I_{OM}	V_{OUT} = 12.0 V	11	–	35	mA	3
Output delay time*1	t_D	–	–	8	16	μs	–
Chopping frequency*1	f_C	–	250	500	–	kHz	–
Start up time*1	t_{PON}	–	–	25	40	μs	4
Output rise time*1	t_R	C = 20 pF, R = 820 Ω	–	–	1.0	μs	5
Output fall time*1	t_F	C = 20 pF, R = 820 Ω	–	–	1.0	μs	5

***1.** This item is guaranteed by design.

2. Nch driver + built-in pull-up resistor (1.2 kΩ typ.) product

Table 9

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–	2.7	5.0	5.5	V	–
Current consumption	I_{DD}	V_{OUT} = "H"	–	4.0	4.5	mA	1
Low level output voltage	V_{OL}	I_{OUT} = 0 mA, V_{OUT} = "L"	–	–	0.4	V	2
High level output voltage	V_{OH}	I_{OUT} = 0 mA, V_{OUT} = "H"	$V_{DD} \times 0.9$	–	–	V	2
Output limit current	I_{OM}	V_{DD} = V_{OUT} = 5.0 V	11	–	35	mA	3
Output delay time*1	t_D	–	–	8	16	μs	–
Chopping frequency*1	f_C	–	250	500	–	kHz	–
Start up time*1	t_{PON}	–	–	25	40	μs	4
Output rise time*1	t_R	C = 20 pF	–	–	1.0	μs	5
Output fall time*1	t_F	C = 20 pF	–	–	1.0	μs	5
Pull-up resistor	R_L	–	0.9	1.2	1.5	kΩ	–

***1.** This item is guaranteed by design.

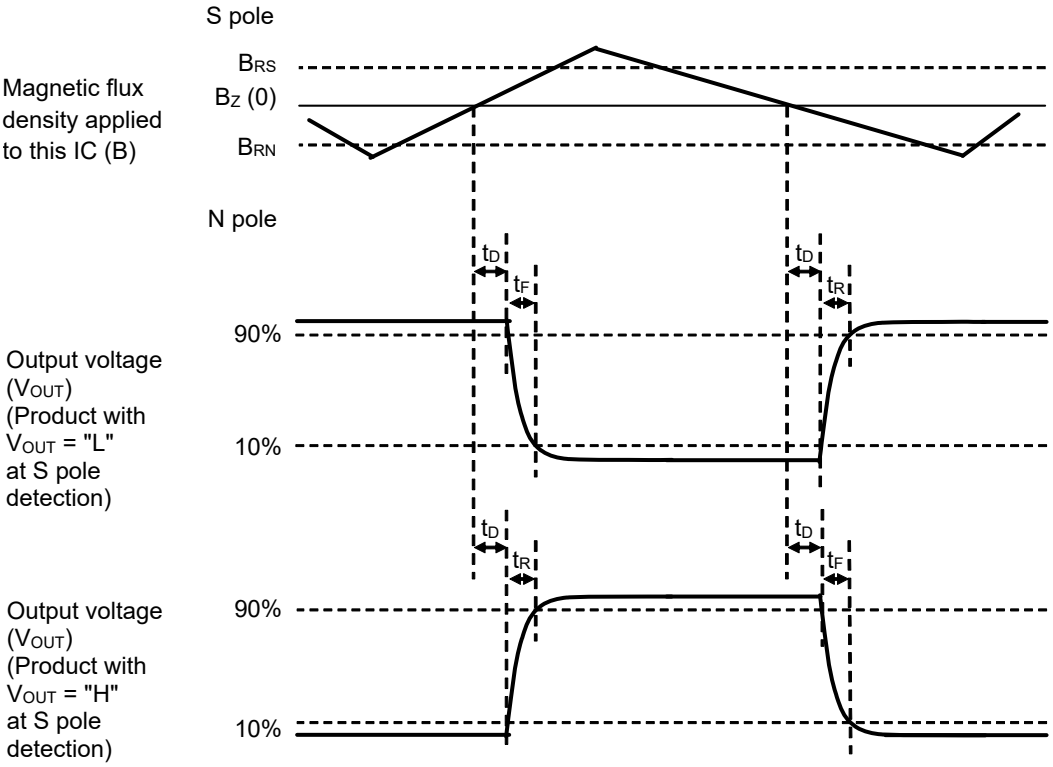


Figure 5 Operation Timing

■ Magnetic Characteristics

1. TSOT-23-3S

1. 1 Product with B_{RS} = 3.0 mT typ.

Table 10

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Zero crossing latch point		B_Z*1	–	–1.15	0.0	1.15	mT	4
Release point	S pole	B_{RS}*2	–	1.9	3.0	4.1	mT	4
	N pole	B_{RN}*3	–	–4.1	–3.0	–1.9	mT	4

1. 2 Product with B_{RS} = 6.0 mT typ.

Table 11

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Zero crossing latch point		B_Z*1	–	–1.35	0.0	1.35	mT	4
Release point	S pole	B_{RS}*2	–	4.0	6.0	8.0	mT	4
	N pole	B_{RN}*3	–	–8.0	–6.0	–4.0	mT	4

2. HSNT-6(2025)

2. 1 Product with B_{RS} = 3.0 mT typ.

Table 12

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Zero crossing latch point		B_Z*1	–	–1.65	0.0	1.65	mT	4
Release point	S pole	B_{RS}*2	–	1.0	3.0	5.0	mT	4
	N pole	B_{RN}*3	–	–5.0	–3.0	–1.0	mT	4

2. 2 Product with B_{RS} = 6.0 mT typ.

Table 13

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Zero crossing latch point		B_Z*1	–	–1.75	0.0	1.75	mT	4
Release point	S pole	B_{RS}*2	–	3.5	6.0	8.5	mT	4
	N pole	B_{RN}*3	–	–8.5	–6.0	–3.5	mT	4

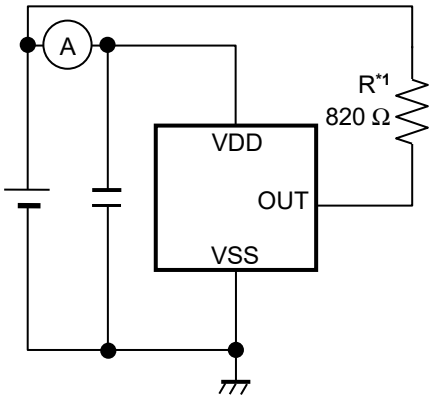
***1.** B_Z: Zero crossing latch point
B_Z is the value of magnetic flux density at which polarity changes are detected according to the magnetic flux density applied to this IC.

***2.** B_{RS}: Release point (S pole)
B_{RS} is the value of magnetic flux density of release point (S pole).
This IC releases the Hold status of the output voltage (V_{OUT}) when the magnetic flux density applied to this IC exceeds B_{RS} (by moving the magnet (S pole) closer).

***3.** B_{RN}: Release point (N pole)
B_{RN} is the value of magnetic flux density of release point (N pole).
This IC releases the Hold status of the output voltage (V_{OUT}) when the magnetic flux density applied to this IC exceeds B_{RN} (by moving the magnet (N pole) closer).

Remark The unit of magnetic density mT can be converted by using the formula 1 mT = 10 Gauss.

■ Test Circuits



*1. Resistor (R) is unnecessary for Nch driver + built-in pull-up resistor product.

Figure 6 Test Circuit 1

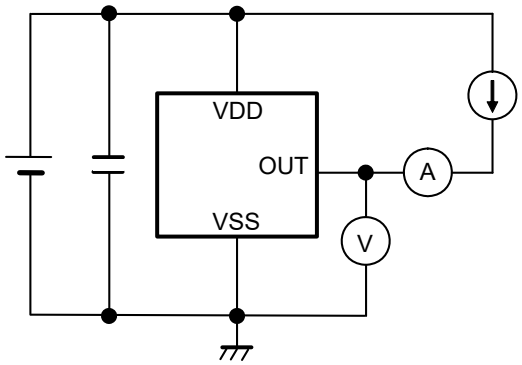


Figure 7 Test Circuit 2

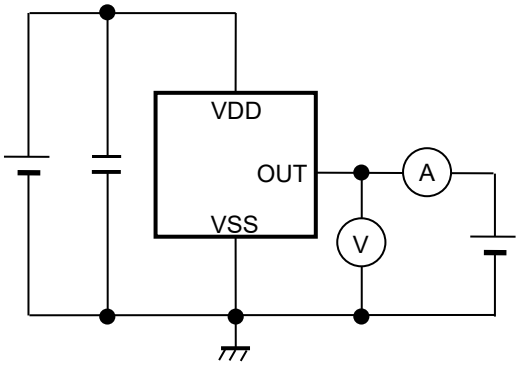
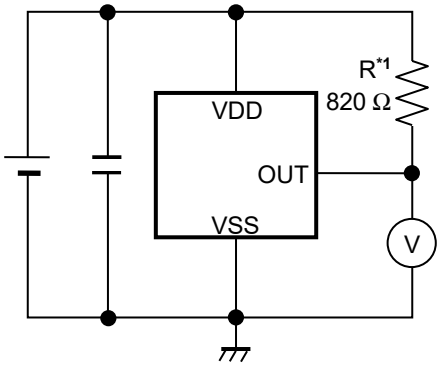
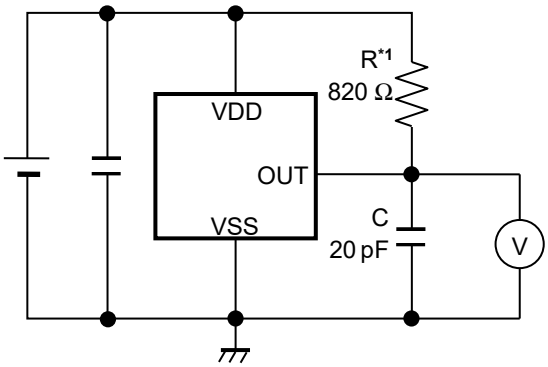


Figure 8 Test Circuit 3



*1. Resistor (R) is unnecessary for Nch driver + built-in pull-up resistor product.

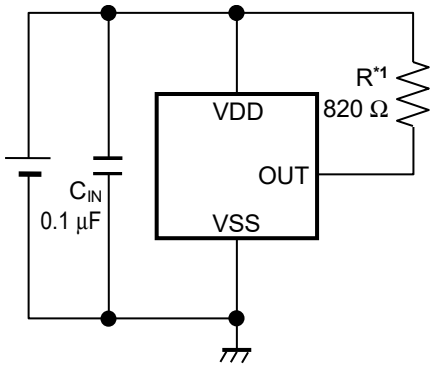
Figure 9 Test Circuit 4



*1. Resistor (R) is unnecessary for Nch driver + built-in pull-up resistor product.

Figure 10 Test Circuit 5

■ Standard Circuit



***1.** Resistor (R) is unnecessary for Nch driver + built-in pull-up resistor product.

Figure 11

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

■ Operation

1. Direction of applied magnetic flux

This IC detects the magnetic flux density which is perpendicular to the package marking surface. A magnetic field is defined as positive when marking side of the package is the S pole, and negative when it is the N pole.
Figure 12 and **Figure 13** show polarity in a magnetic field and direction in which magnetic flux is being applied.

1. 1 TSOT-23-3S

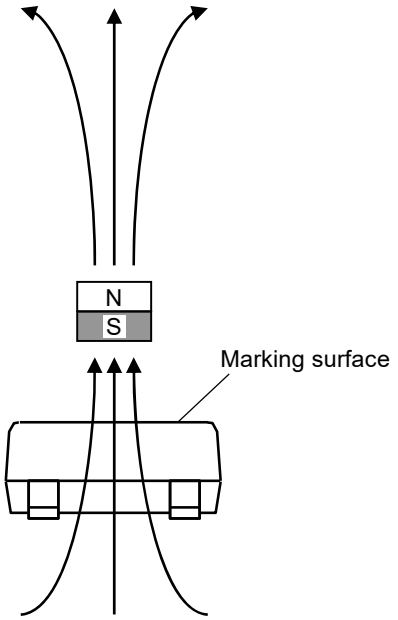


Figure 12

1. 2 HSNT-6(2025)

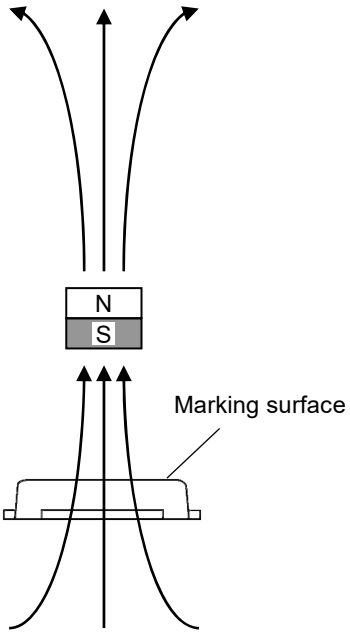


Figure 13

2. Position of Hall sensor

Figure 14 and **Figure 15** show the position of Hall sensor.
The center of this Hall sensor is located in the area indicated by a circle, which is in the center of a package as described below.
The following also shows the distance (typ. value) between the marking surface and the chip surface of a package.

2. 1 TSOT-23-3S

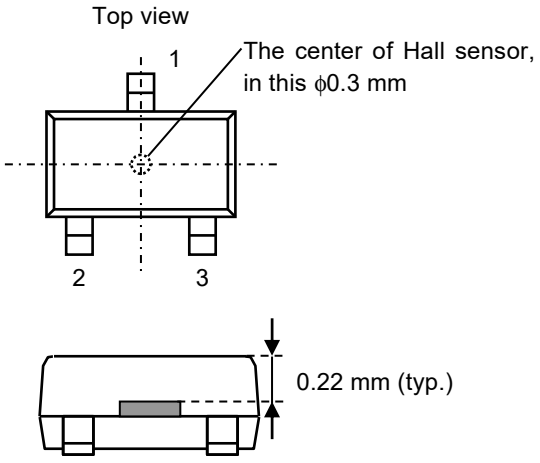


Figure 14

2. 2 HSNT-6(2025)

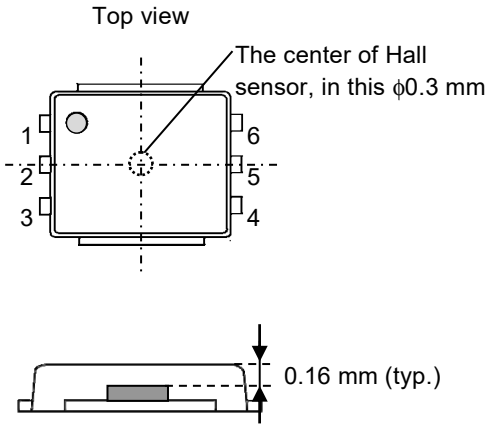


Figure 15

3. Basic operation

This IC switches output voltage level (V_{OUT}) when the IC detects magnetic flux density (magnetic field) polarity changes by using ZCL technology. ZCL technology realizes polarity changes detection and hold operation (Hold status) of V_{OUT}. This is different from the conventional bipolar latch method. ZCL detection method has no hysteresis width of the magnetic sensitivity to switch V_{OUT}. Instead, the ZCL detection method can switch V_{OUT} without chattering by using the Hold status.

3. 1 ZCL basic operation

This IC switches V_{OUT} after the output delay time (t_D) from when the magnetic flux density applied to this IC crosses B_Z (from $B > B_{RS}$ to $B < B_Z$ or from $B < B_{RN}$ to $B > B_Z$). When V_{OUT} is switched, this IC starts the Hold status. In the Hold status of V_{OUT}, when the magnetic flux density applied to this IC exceeds B_{RS} or B_{RN}, this IC releases the Hold status (from $B < B_Z$ to $B < B_{RN}$ or from $B > B_Z$ to $B > B_{RS}$).
Figure 16 and **Figure 17** show the V_{OUT} operation timing when sine wave magnetic flux density is applied to this IC.

(1) $B > B_{RS} \rightarrow B < B_Z$, and after t_D, V_{OUT} = "L" → "H", and Hold status starts
(2) $B < B_Z \rightarrow B < B_{RN}$, and after t_D, Hold status is released, and V_{OUT} = "H" continues
(3) $B < B_{RN} \rightarrow B > B_Z$, and after t_D, V_{OUT} = "H" → "L", and Hold status starts
(4) $B > B_Z \rightarrow B > B_{RS}$, and after t_D, Hold status is released, and V_{OUT} = "L" continues

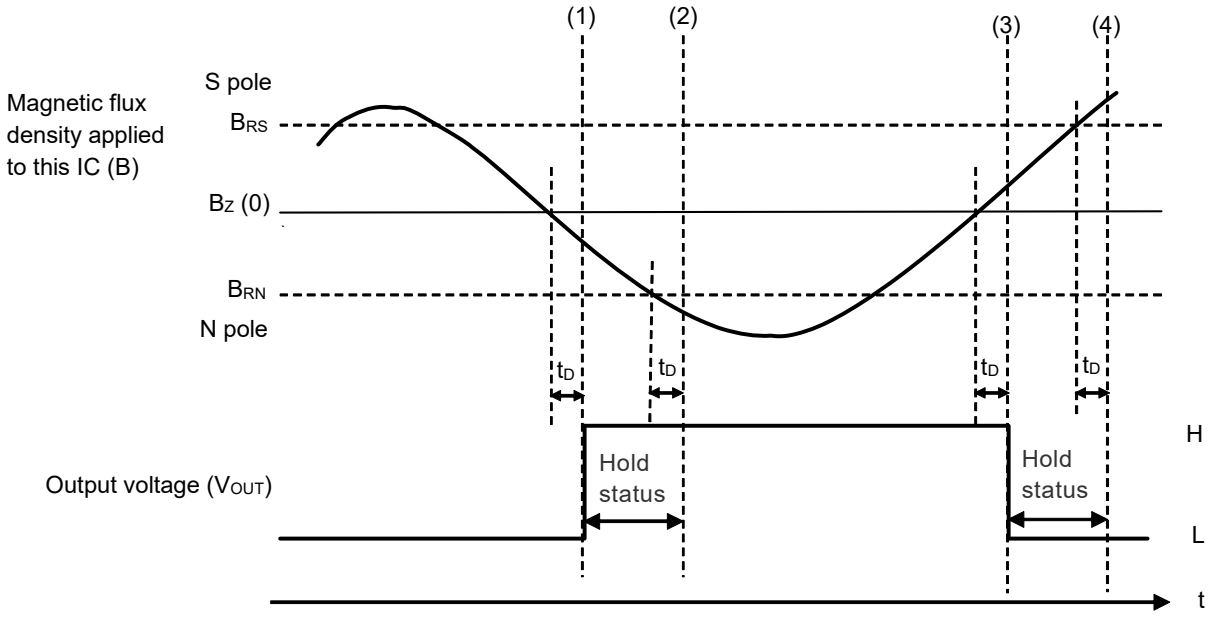


Figure 16 Product with V_{OUT} = "L" at S pole detection

(1) $B > B_{RS} \rightarrow B < B_Z$, and after t_D, V_{OUT} = "H" → "L", and Hold status starts
(2) $B < B_Z \rightarrow B < B_{RN}$, and after t_D, Hold status is released, and V_{OUT} = "L" continues
(3) $B < B_{RN} \rightarrow B > B_Z$, and after t_D, V_{OUT} = "L" → "H", and Hold status starts
(4) $B > B_Z \rightarrow B > B_{RS}$, and after t_D, Hold status is released, and V_{OUT} = "H" continues

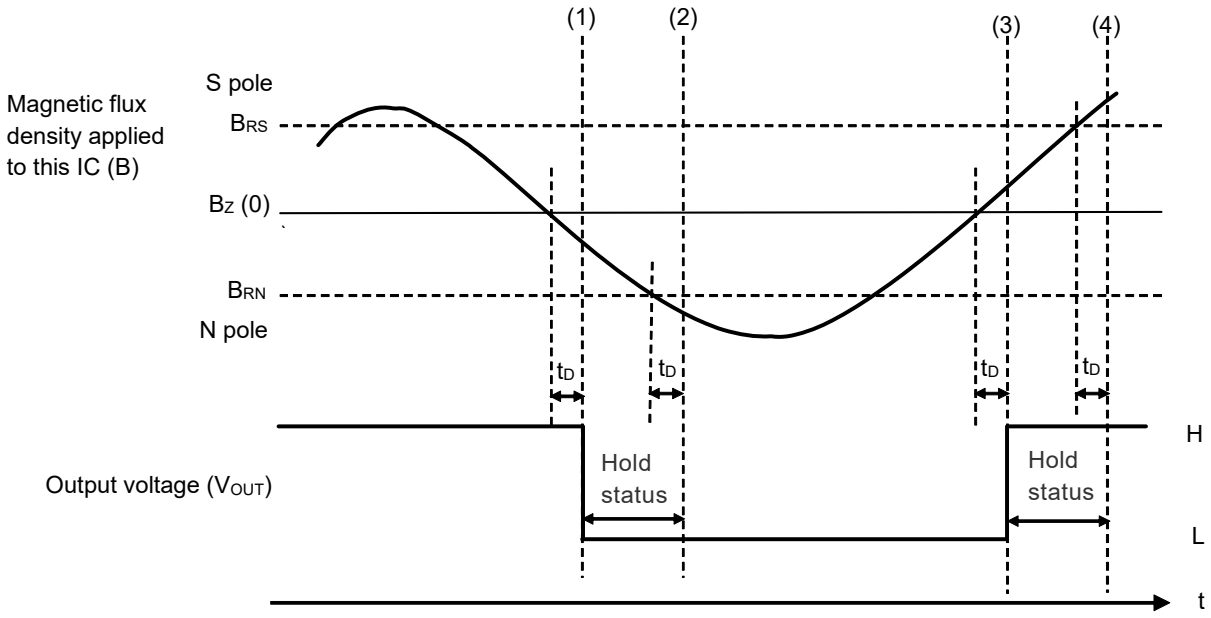


Figure 17 Product with V_{OUT} = "H" at S pole detection

3. 2 Prevention of V_{OUT} chattering by Hold status

By the Hold status, this IC can switch V_{OUT} without chattering even under an influence of external mechanical vibrations, electrical noise, or magnetic noise.
Figure 18 and **Figure 19** show the V_{OUT} operation when the magnetic flux density applied to this IC changes near the zero crossing latch point (B_Z) and B_Z is crossed multiple times.

(1) In the Hold status, the IC retains V_{OUT} when the magnetic flux density applied to this IC crosses B_Z.

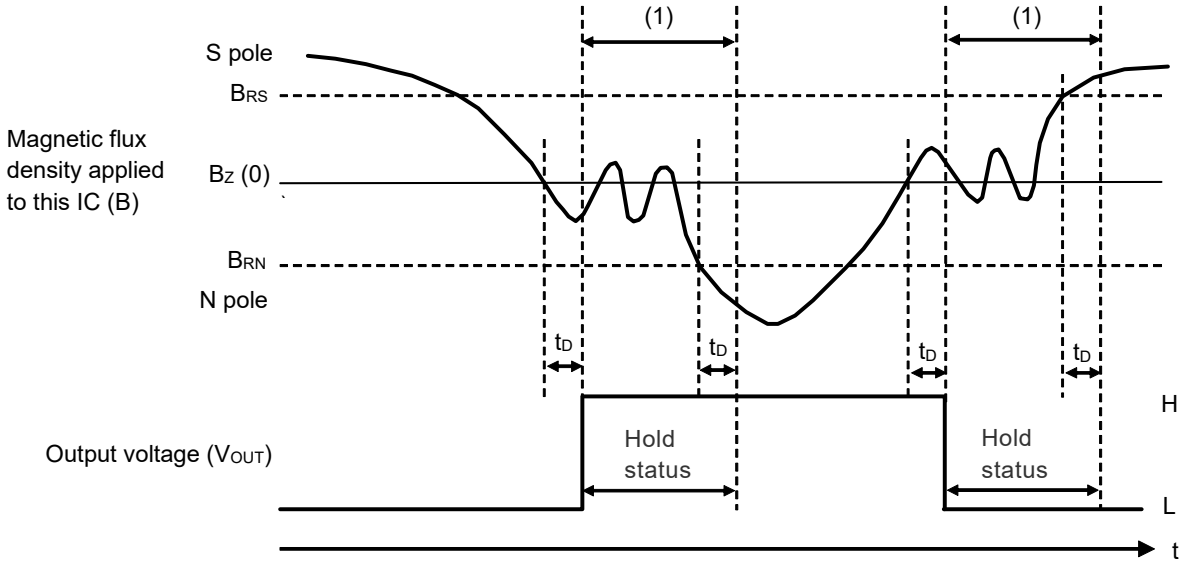


Figure 18 Product with V_{OUT} = "L" at S pole detection

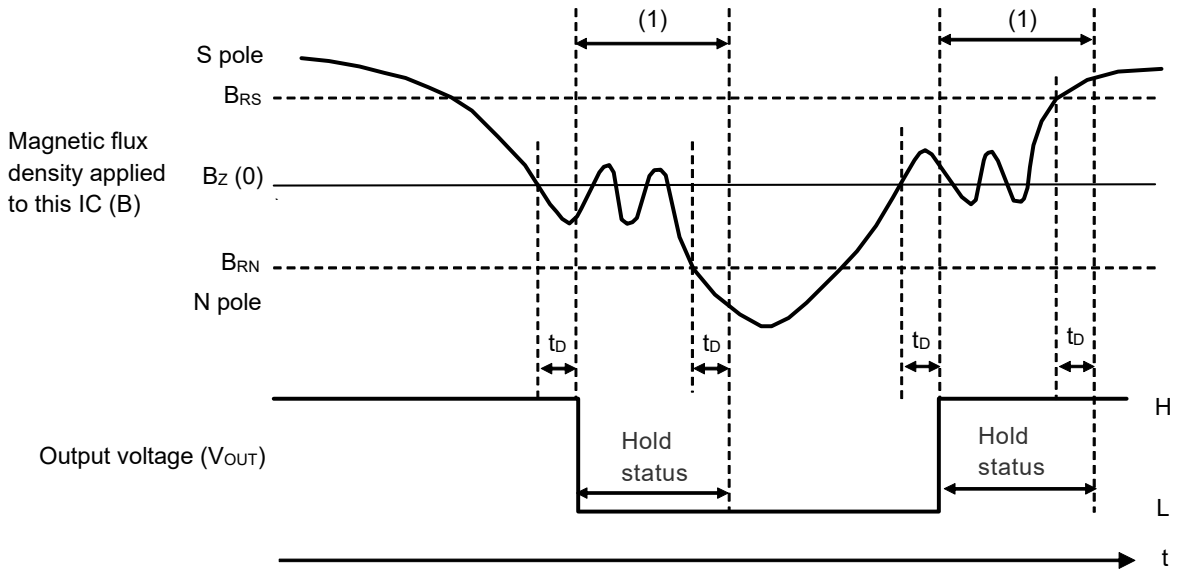


Figure 19 Product with V_{OUT} = "H" at S pole detection

3. 3 Operation when polarity changes direction is inverted in the Hold status

In the Hold status, when the polarity changes direction is inverted, this IC release the Hold status at the opposite release point and switches V_{OUT}.
Figure 20 and **Figure 21** show the V_{OUT} operation timing when the polarity change direction is inverted.

(1) $B > B_Z \rightarrow B < B_Z$, and after t_D, V_{OUT} = "L" → "H", and Hold status starts
(2) During Hold status, even after $B < B_Z \rightarrow B > B_Z$, V_{OUT} = "H" is retained
(3) $B > B_Z \rightarrow B > B_{RS}$, and after t_D, Hold status is released, and V_{OUT} = "H" → "L"
(4) $B < B_Z \rightarrow B > B_Z$, and after t_D, V_{OUT} = "H" → "L", and Hold status starts
(5) During Hold status, even after $B > B_Z \rightarrow B < B_Z$, V_{OUT} = "L" is retained
(6) $B < B_Z \rightarrow B < B_{RN}$, and after t_D, Hold status is released, and V_{OUT} = "L" → "H"

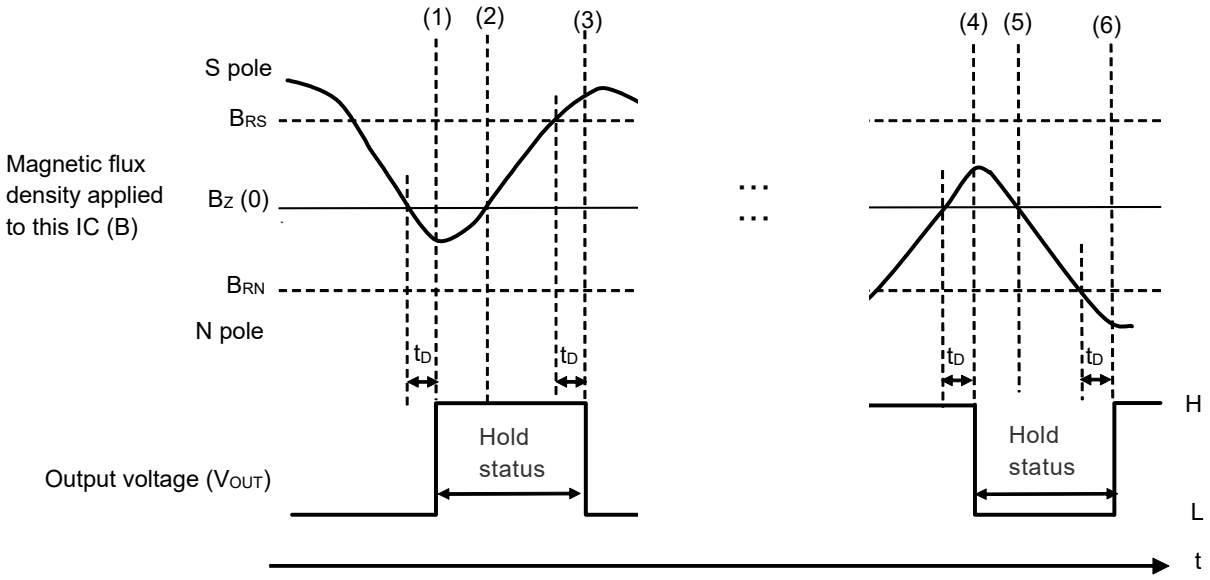


Figure 20 Product with V_{OUT} = "L" at S pole detection

(1) $B > B_Z \rightarrow B < B_Z$, and after t_D, V_{OUT} = "H" → "L", and Hold status starts
(2) During Hold status, even after $B < B_Z \rightarrow B > B_Z$, V_{OUT} = "L" is retained
(3) $B > B_Z \rightarrow B > B_{RS}$, and after t_D, Hold status is released, and V_{OUT} = "L" → "H"
(4) $B < B_Z \rightarrow B > B_Z$, and after t_D, V_{OUT} = "L" → "H", and Hold status starts
(5) During Hold status, even after $B > B_Z \rightarrow B < B_Z$, V_{OUT} = "H" is retained
(6) $B < B_Z \rightarrow B < B_{RN}$, and after t_D, Hold status is released, and V_{OUT} = "H" → "L"

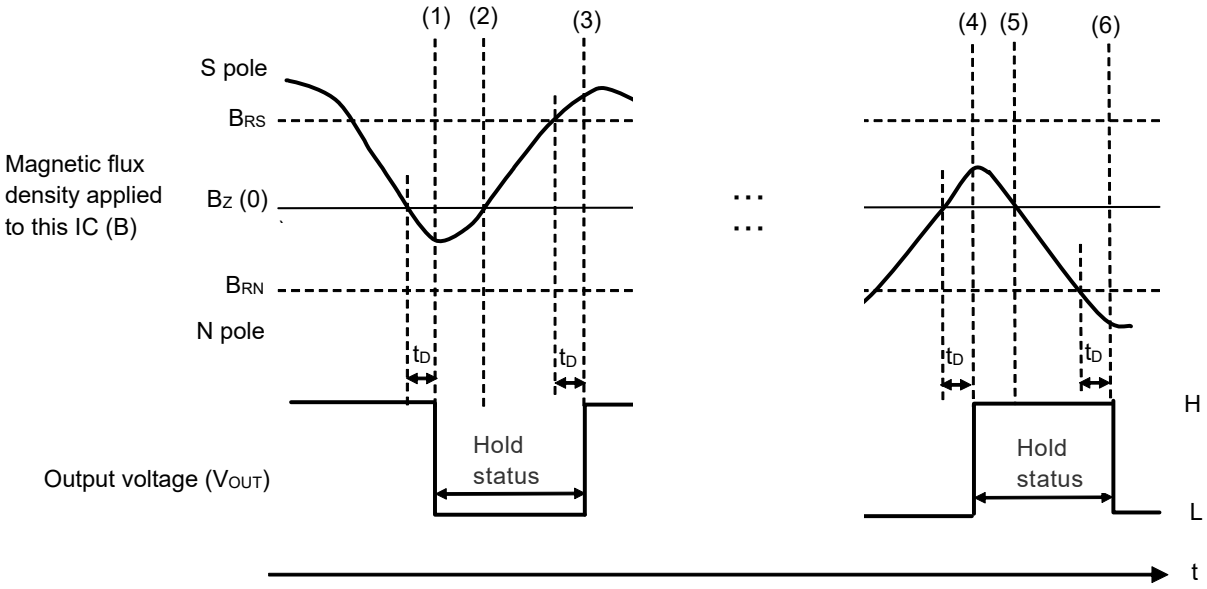


Figure 21 Product with V_{OUT} = "H" at S pole detection

4. Power-on operation

This IC requires start up time (t_{PON}) during the time immediately after power-on until V_{OUT} switches. During the t_{PON} period, V_{OUT} is "H". After t_{PON}, when B > B_{RS} or B < B_{RN} is detected, polarity changes can be detected.

4. 1 B > B_{RS} or B < B_{RN}

When the magnetic flux density applied to this IC at power-on is B > B_{RS} or B < B_{RN}, after t_{PON}, V_{OUT} switches according to the output logic at the S pole detection, and polarity changes can be detected.
Figure 22 and **Figure 23** show V_{OUT} operation immediately after power-on when B > B_{RS} or B < B_{RN}.

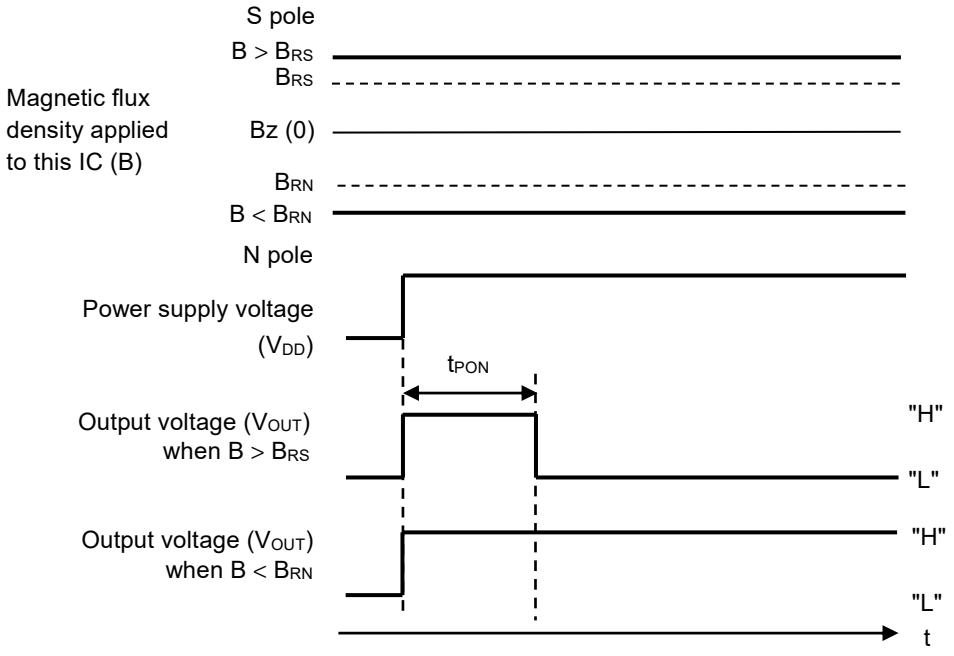


Figure 22 Product with V_{OUT} = "L" at S pole detection

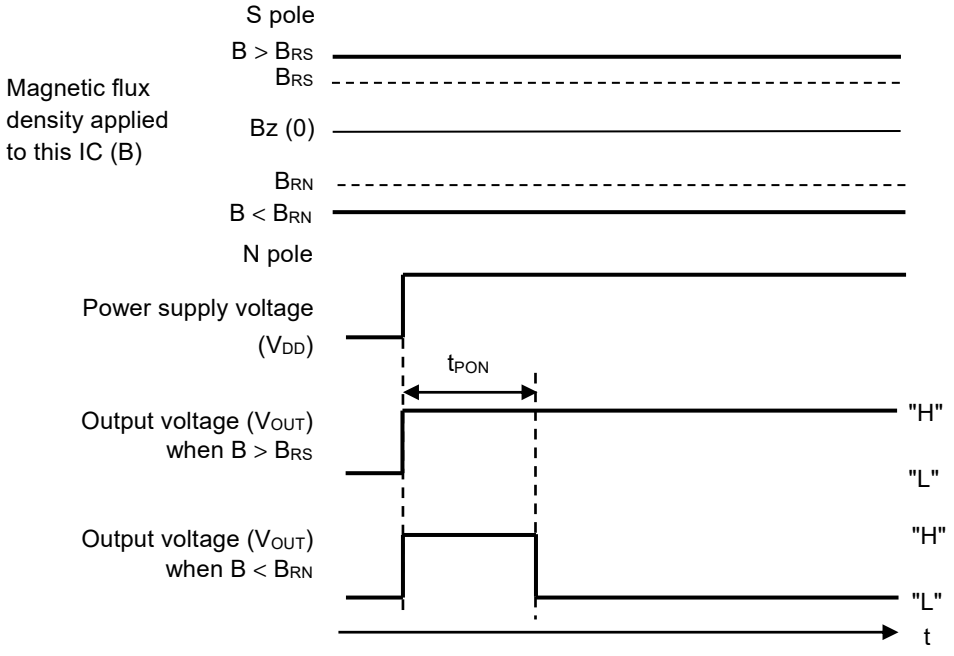


Figure 23 Product with V_{OUT} = "H" at S pole detection

4. 2 B_{RN} < B < B_{RS}

When the magnetic flux density applied to this IC at power-on is B_{RN} < B < B_{RS}, after t_{PON}, V_{OUT} continues "H". Thereafter, when the magnetic flux density changes to B > B_{RS} or B < B_{RN}, after t_D, V_{OUT} switches according to the output logic at the S pole detection and magnetic flux density, and polarity changes can be detected.
Figure 24 and **Figure 25** show V_{OUT} operation when change of B_{RN} < B < B_{RS} → B > B_{RS} or B < B_{RN} occurs after t_{PON}.

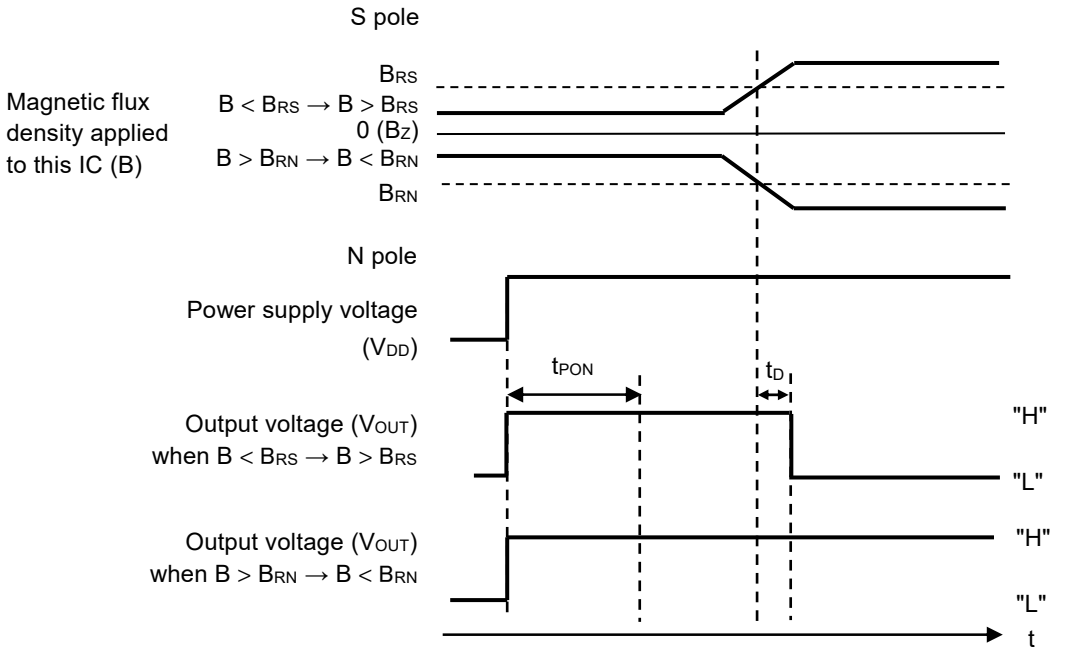


Figure 24 Product with V_{OUT} = "L" at S pole detection

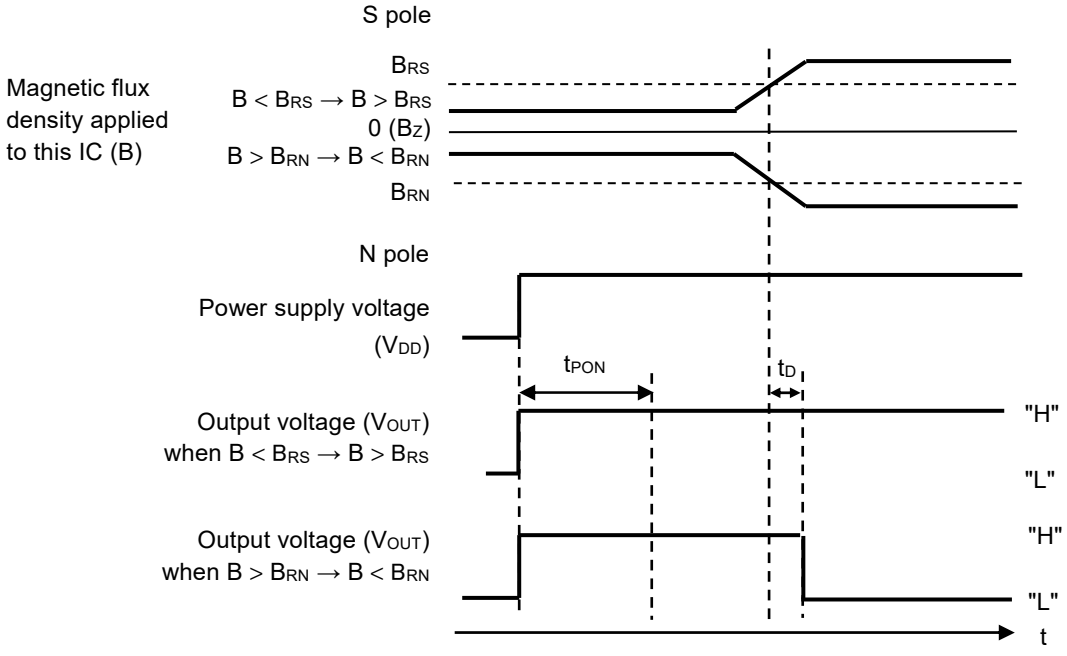


Figure 25 Product with V_{OUT} = "H" at S pole detection

■ Precautions

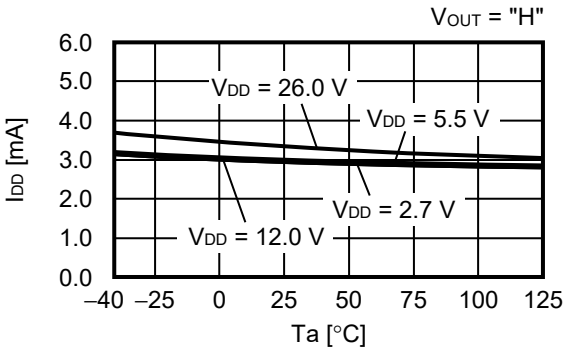
- If the impedance of the power supply is high, the IC may malfunction due to a supply voltage drop caused by feed-through current. Take care with the pattern wiring to ensure that the impedance of the power supply is low.
- Note that the IC may malfunction if the power supply voltage rapidly changes. When the IC is used under the environment where the power supply voltage rapidly changes, it is recommended to judge the output voltage of the IC by reading it multiple times.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Although this IC has a built-in output current limit circuit, it may suffer physical damage such as product deterioration under the environment where the absolute maximum ratings are exceeded.
- The application conditions for the power supply voltage, the pull-up voltage, and the pull-up resistor should not exceed the power dissipation.
- Large stress on this IC may affect the magnetic characteristics. Avoid large stress which is caused by the handling during or after mounting the IC on a board.
- Since the package heat radiation differs according to the conditions of the application, perform thorough evaluation with actual applications to confirm no problems occur.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

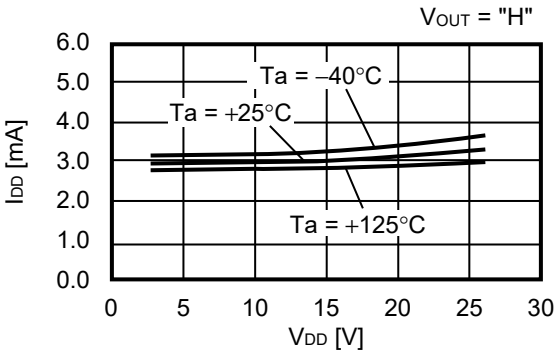
1. Electrical Characteristics

1. 1 S-576ZxxxB

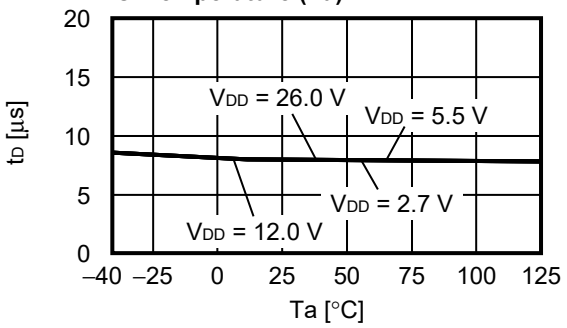
1. 1. 1 Current consumption (I_{DD}) vs. Temperature (Ta)



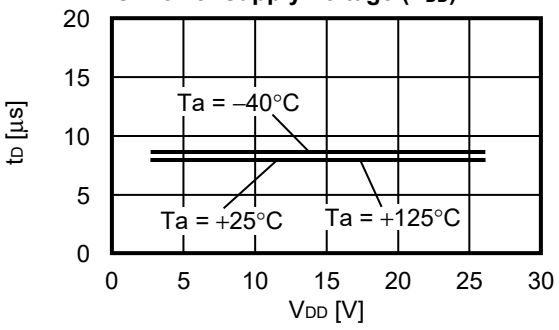
1. 1. 2 Current consumption (I_{DD}) vs. Power supply voltage (V_{DD})



1. 1. 3 Output delay time (t_D) vs. Temperature (Ta)



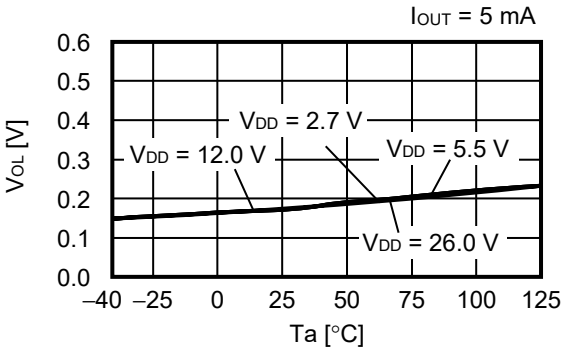
1. 1. 4 Output delay time (t_D) vs. Power supply voltage (V_{DD})



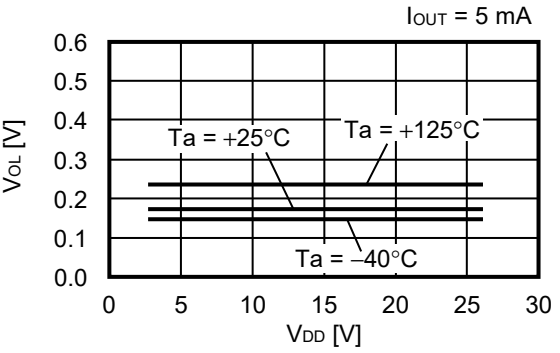
Caution V_{DD} = 2.7 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (1.2 kΩ typ.). Comply with power supply voltage range and do not exceed absolute maximum ratings.

1. 2 S-576ZNxxB

1. 2. 1 Low level output voltage (V_{OL}) vs. Temperature (Ta)

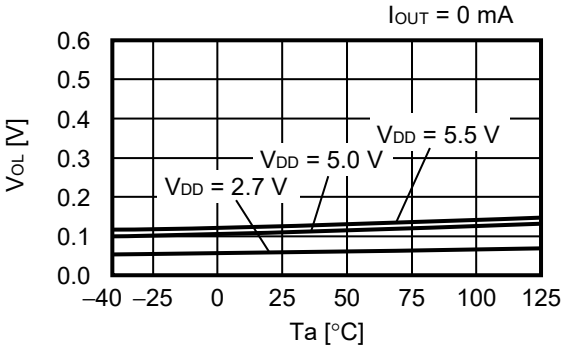


1. 2. 2 Low level output voltage (V_{OL}) vs. Power supply voltage (V_{DD})

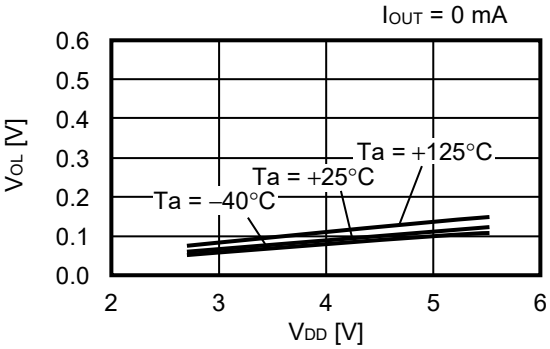


1. 3 S-576Z1xxB

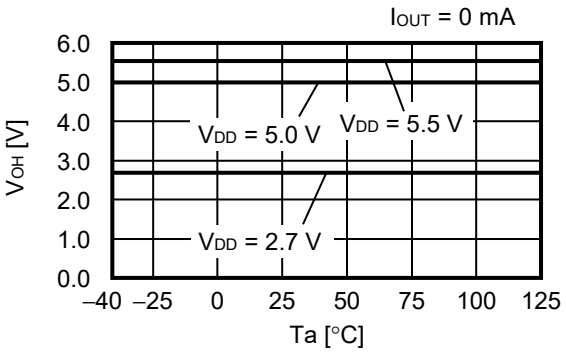
1. 3. 1 Low level output voltage (V_{OL}) vs. Temperature (Ta)



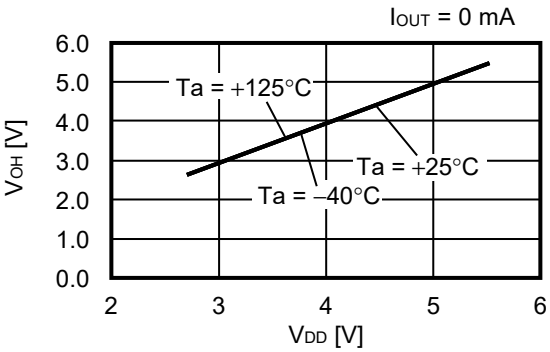
1. 3. 2 Low level output voltage (V_{OL}) vs. Power supply voltage (V_{DD})



1. 3. 3 High level output voltage (V_{OH}) vs. Temperature (Ta)



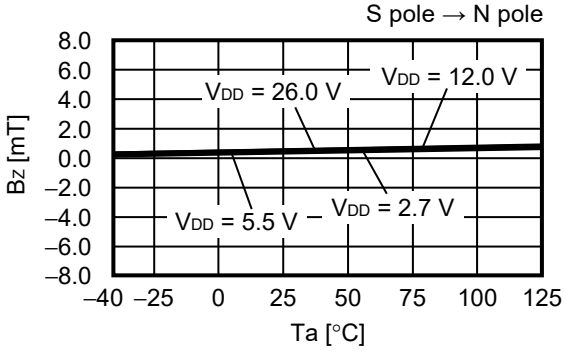
1. 3. 4 High level output voltage (V_{OH}) vs. Power supply voltage (V_{DD})



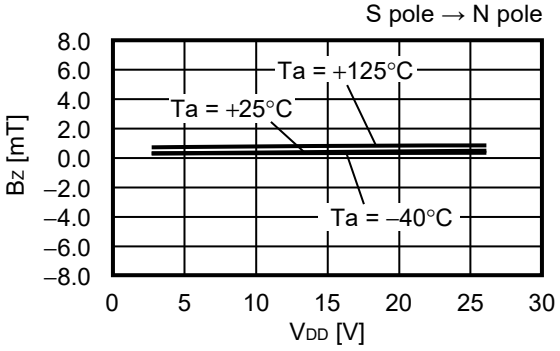
2. Magnetic Characteristics

2. 1 S-576Zxx1B-L3T2U

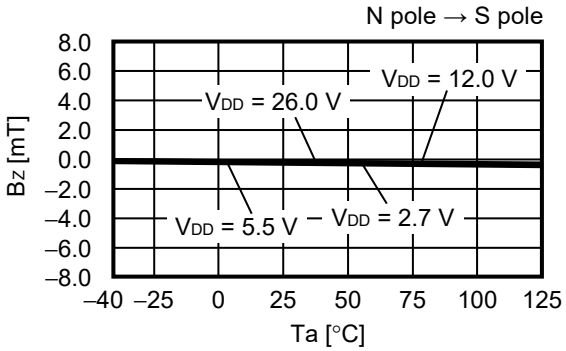
2. 1. 1 Zero crossing latch point (B_Z) vs. Temperature (Ta)



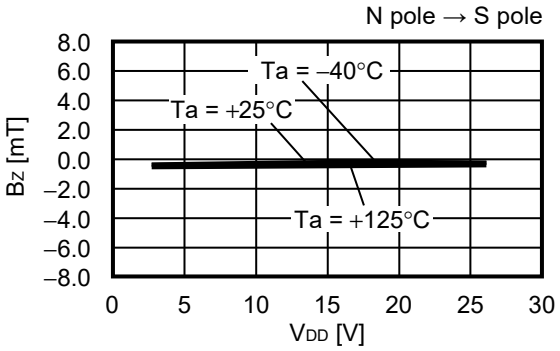
2. 1. 2 Zero crossing latch point (B_Z) vs. Power supply voltage (V_{DD})



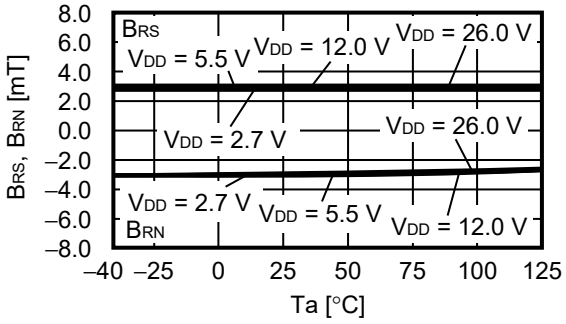
2. 1. 3 Zero crossing latch point (B_Z) vs. Temperature (Ta)



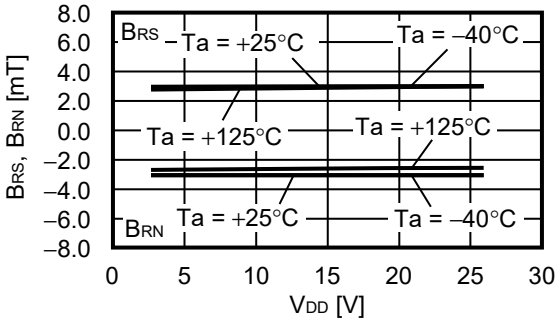
2. 1. 4 Zero crossing latch point (B_Z) vs. Power supply voltage (V_{DD})



2. 1. 5 Release point (B_{RS}, B_{RN}) vs. Temperature (Ta)



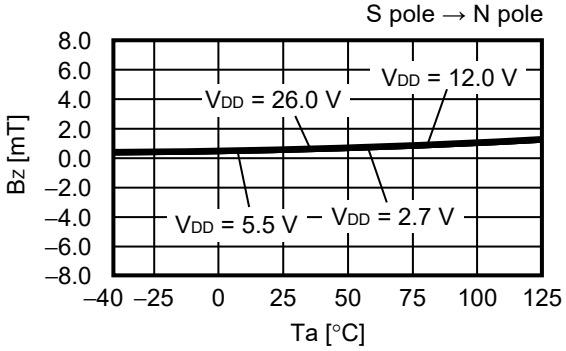
2. 1. 6 Release point (B_{RS}, B_{RN}) vs. Power supply voltage (V_{DD})



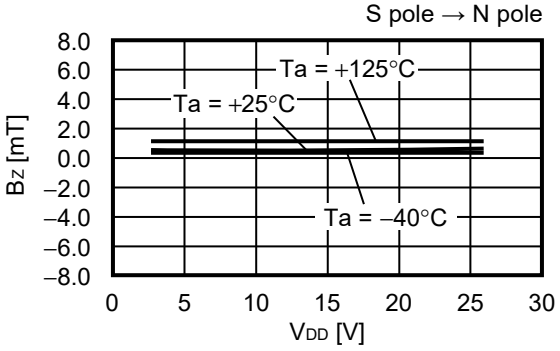
Caution **V_{DD} = 2.7 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (1.2 kΩ typ.). Comply with power supply voltage range and do not exceed absolute maximum ratings.**

2. 2 S-576Zxx2B-L3T2U

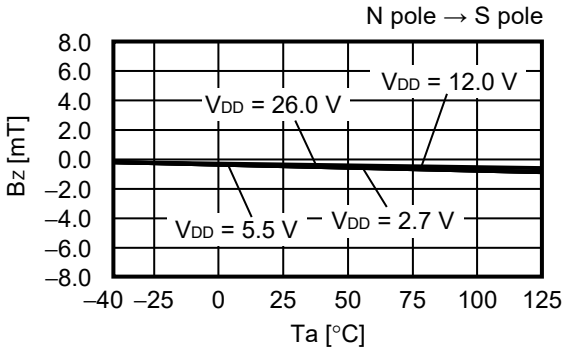
2. 2. 1 Zero crossing latch point (B_Z) vs. Temperature (Ta)



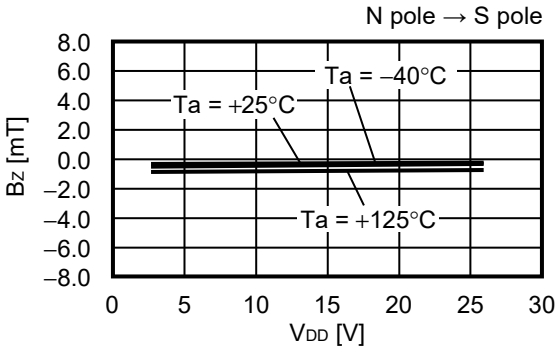
2. 2. 2 Zero crossing latch point (B_Z) vs. Power supply voltage (V_{DD})



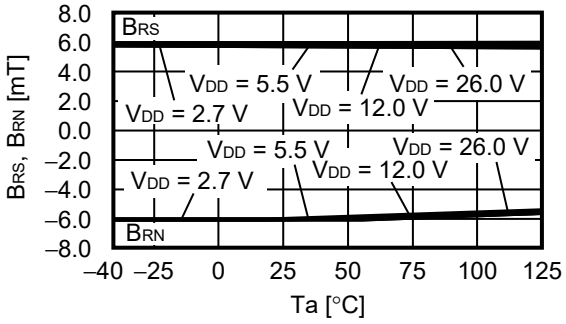
2. 2. 3 Zero crossing latch point (B_Z) vs. Temperature (Ta)



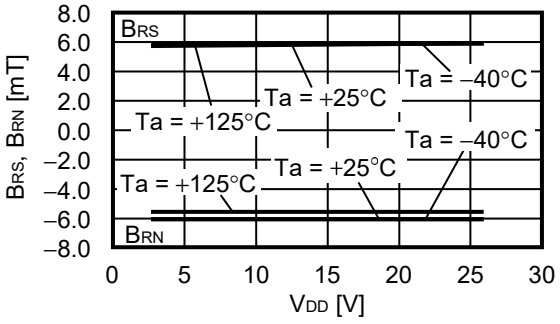
2. 2. 4 Zero crossing latch point (B_Z) vs. Power supply voltage (V_{DD})



2. 2. 5 Release point (B_{RS}, B_{RN}) vs. Temperature (Ta)



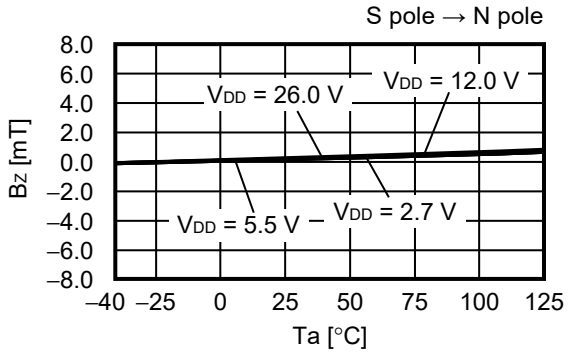
2. 2. 6 Release point (B_{RS}, B_{RN}) vs. Power supply voltage (V_{DD})



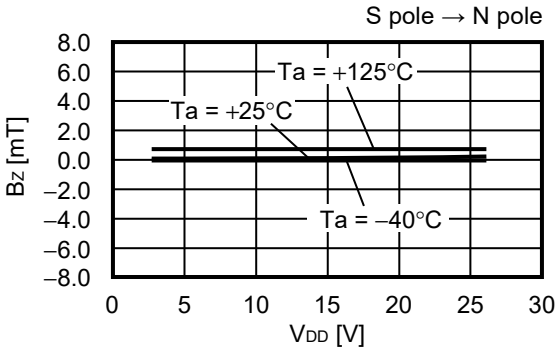
Caution V_{DD} = 2.7 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (1.2 kΩ typ.). Comply with power supply voltage range and do not exceed absolute maximum ratings.

2. 3 S-576Zxx1B-A6T8U

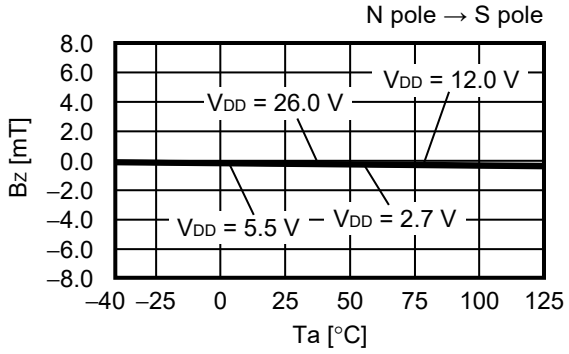
2. 3. 1 Zero crossing latch point (B_Z) vs. Temperature (Ta)



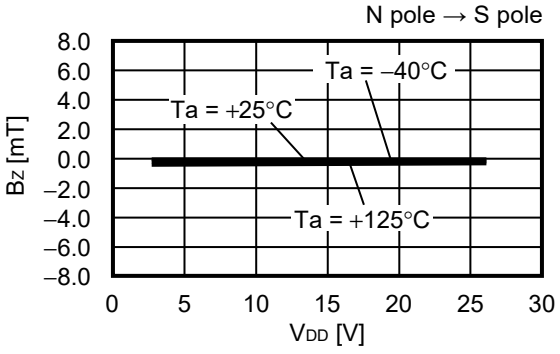
2. 3. 2 Zero crossing latch point (B_Z) vs. Power supply voltage (V_{DD})



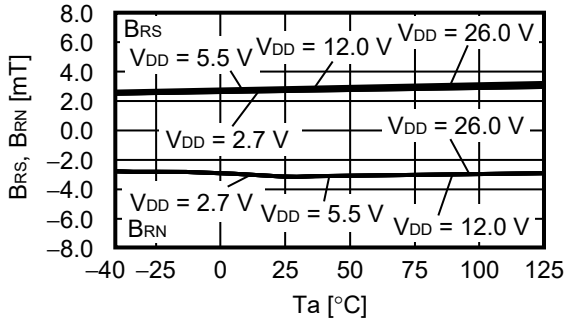
2. 3. 3 Zero crossing latch point (B_Z) vs. Temperature (Ta)



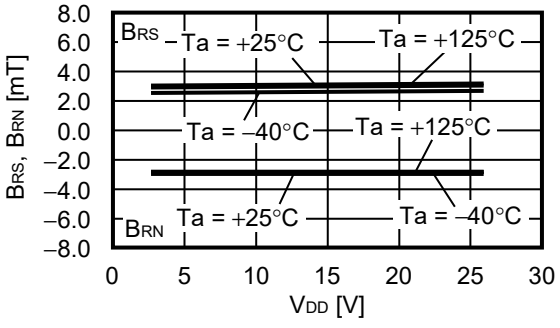
2. 3. 4 Zero crossing latch point (B_Z) vs. Power supply voltage (V_{DD})



2. 3. 5 Release point (B_{RS}, B_{RN}) vs. Temperature (Ta)



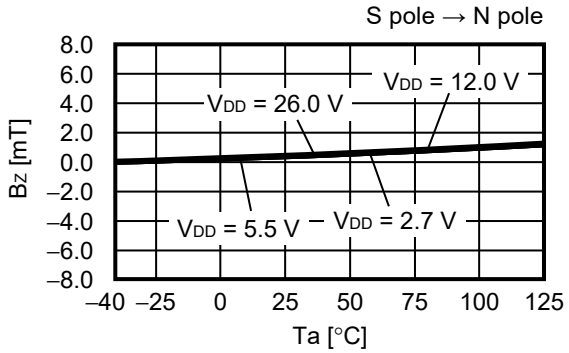
2. 3. 6 Release point (B_{RS}, B_{RN}) vs. Power supply voltage (V_{DD})



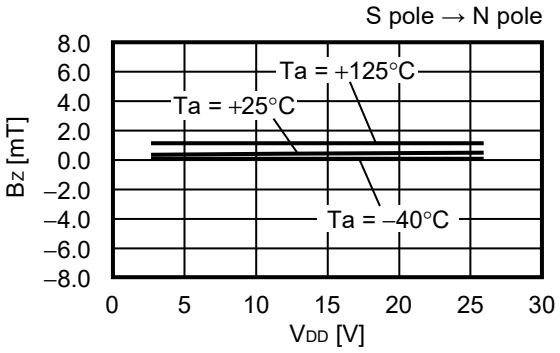
Caution **V_{DD} = 2.7 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (1.2 kΩ typ.). Comply with power supply voltage range and do not exceed absolute maximum ratings.**

2. 4 S-576Zxx2B-A6T8U

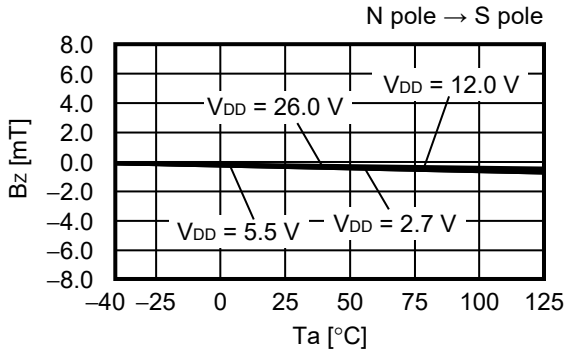
2. 4. 1 Zero crossing latch point (B_Z) vs. Temperature (Ta)



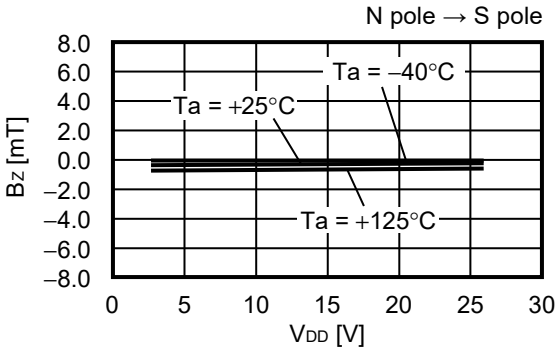
2. 4. 2 Zero crossing latch point (B_Z) vs. Power supply voltage (V_{DD})



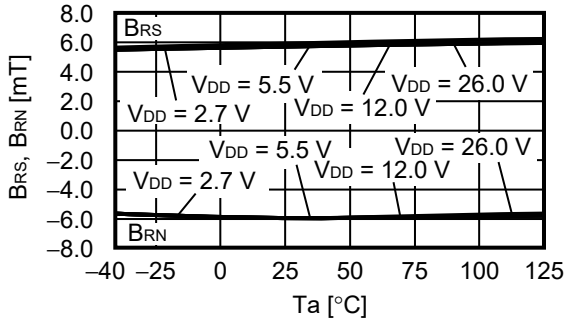
2. 4. 3 Zero crossing latch point (B_Z) vs. Temperature (Ta)



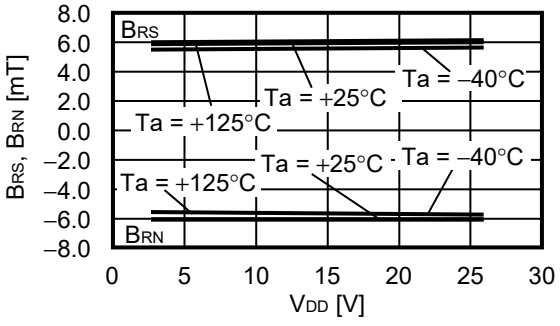
2. 4. 4 Zero crossing latch point (B_Z) vs. Power supply voltage (V_{DD})



2. 4. 5 Release point (B_{RS}, B_{RN}) vs. Temperature (Ta)



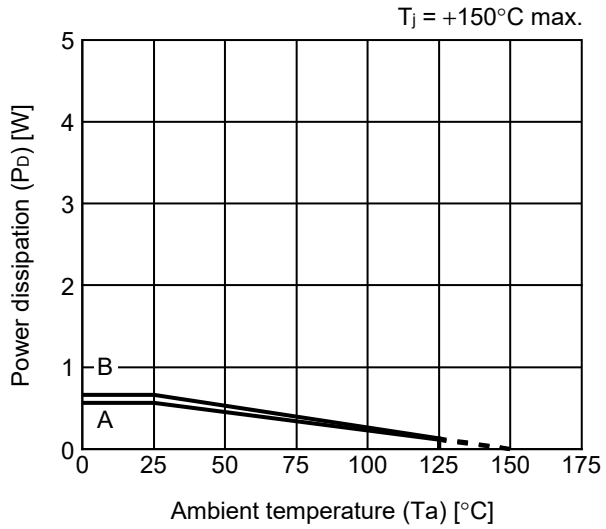
2. 4. 6 Release point (B_{RS}, B_{RN}) vs. Power supply voltage (V_{DD})



Caution V_{DD} = 2.7 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (1.2 kΩ typ.). Comply with power supply voltage range and do not exceed absolute maximum ratings.

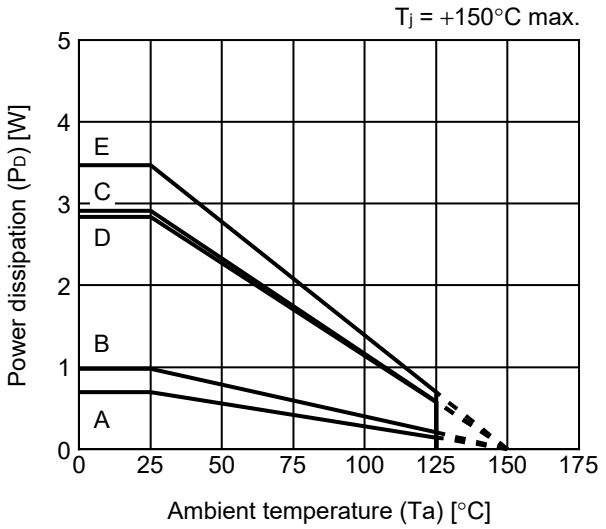
■ Power Dissipation

TSOT-23-3S



Board	Power Dissipation (P_D)
A	0.56 W
B	0.66 W
C	–
D	–
E	–

HSNT-6(2025)

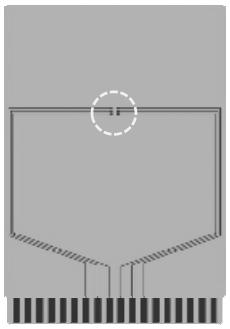


Board	Power Dissipation (P_D)
A	0.69 W
B	0.98 W
C	2.91 W
D	2.84 W
E	3.47 W

TSOT-23-3S Test Board

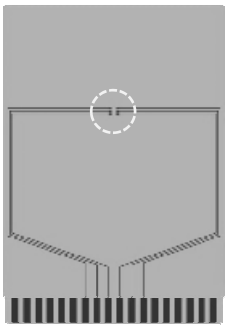
IC Mount Area

(1) Board A



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



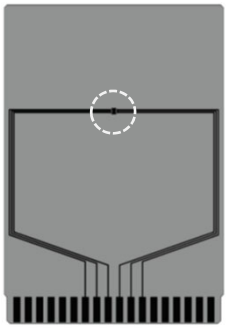
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. TSOT23x-A-Board-SD-1.0

HSNT-6(2025) Test Board

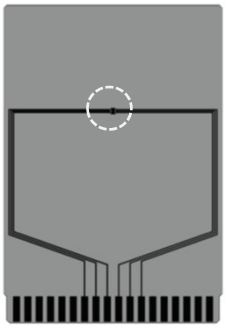
IC Mount Area

(1) Board A



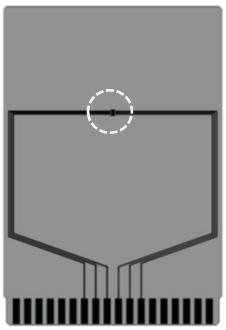
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

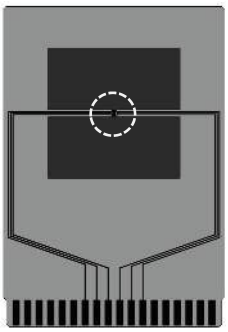
enlarged view

No. HSNT6-B-Board-SD-1.0

HSNT-6(2025) Test Board

IC Mount Area

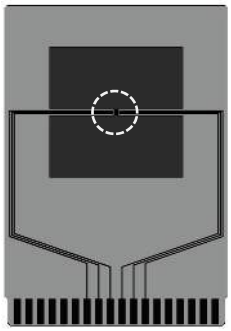
(4) Board D



enlarged view

Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

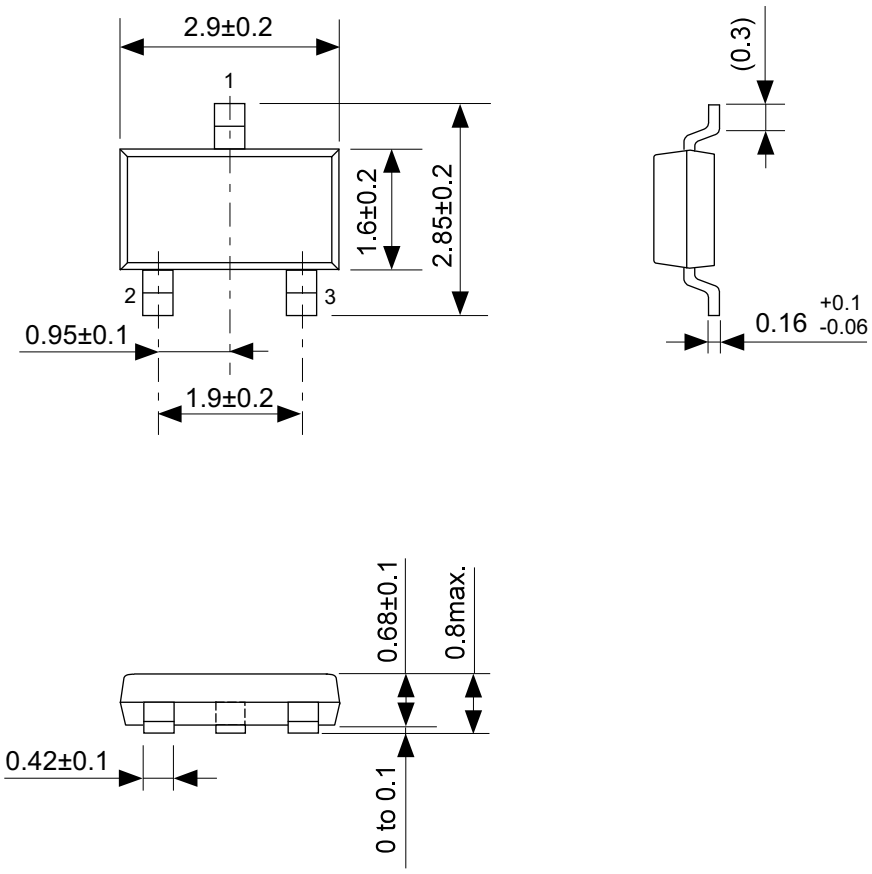
(5) Board E



enlarged view

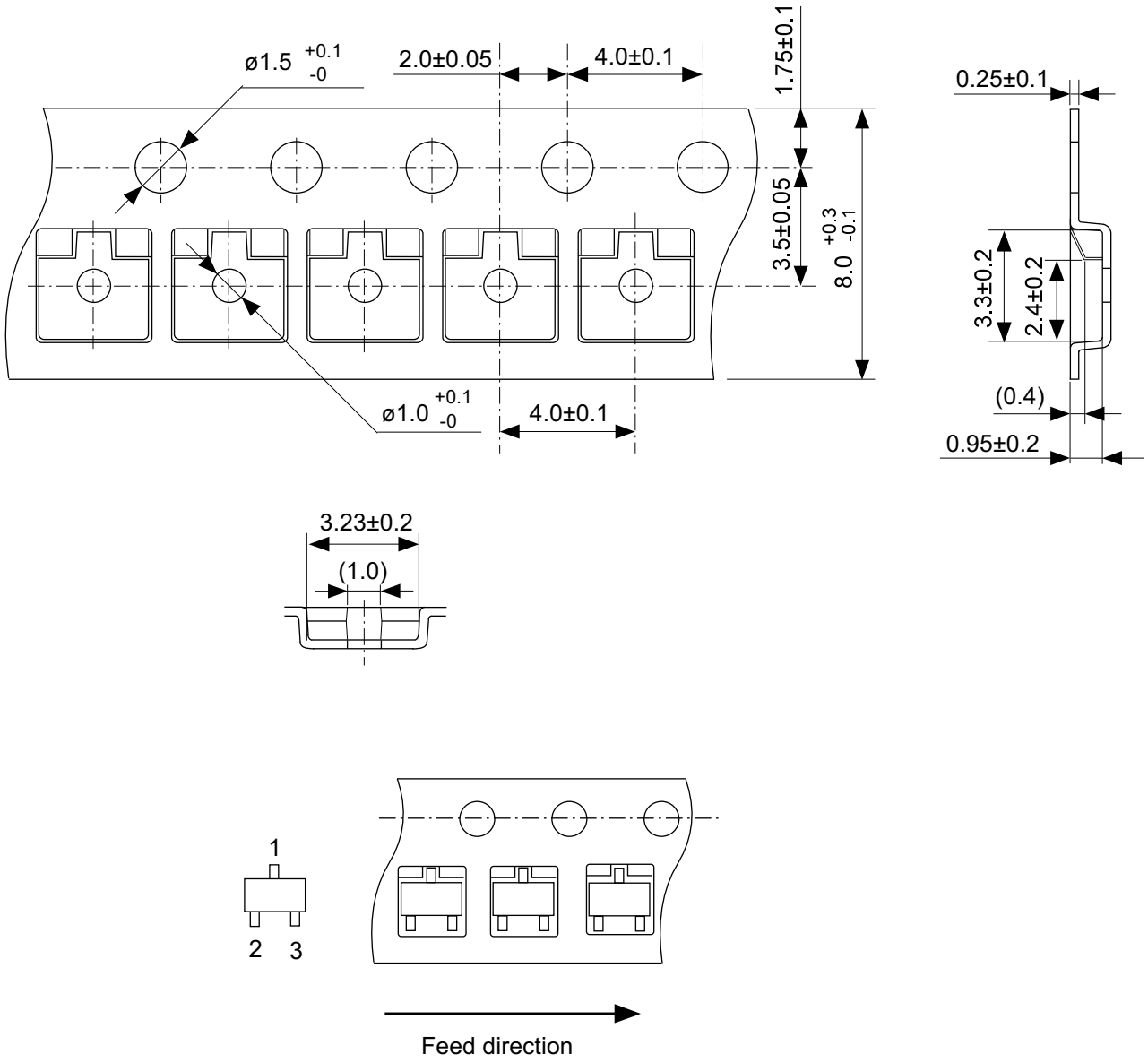
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HSNT6-B-Board-SD-1.0



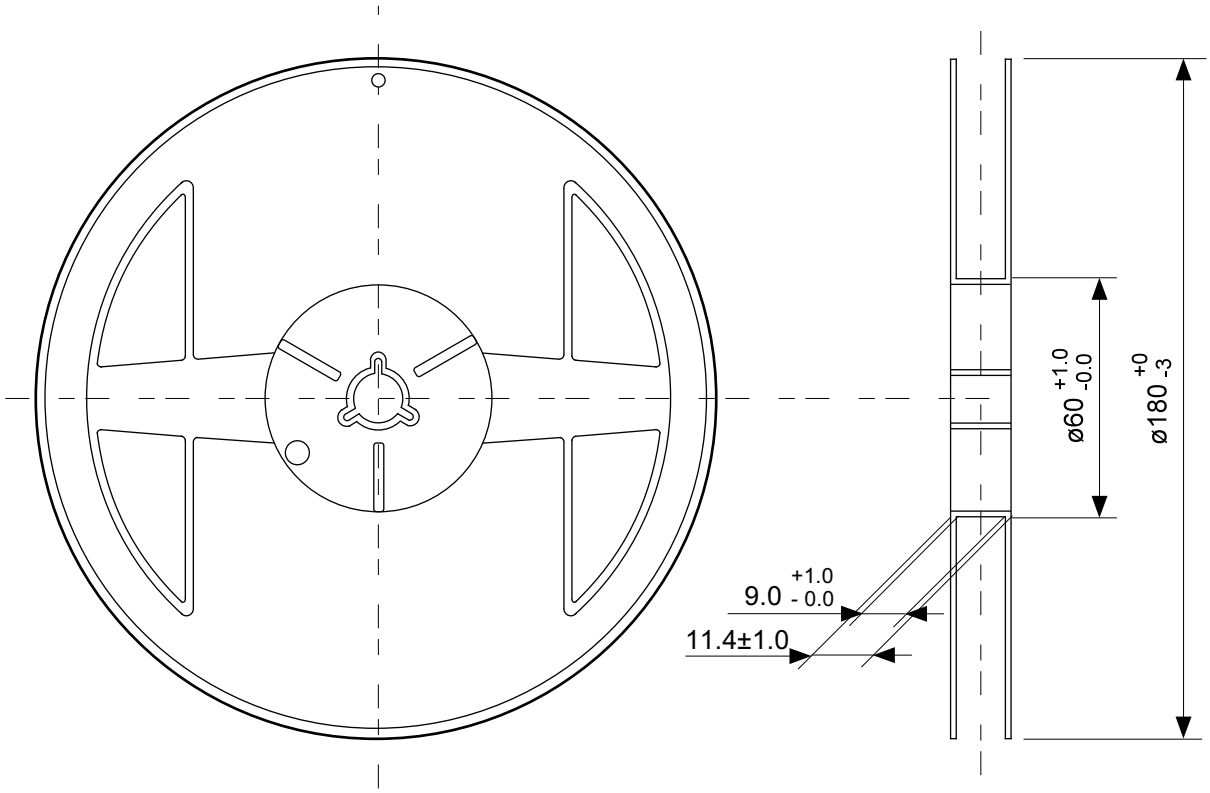
No. MP003-E-P-SD-1.0

TITLE	TSOT233S-A-PKG Dimensions
No.	MP003-E-P-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

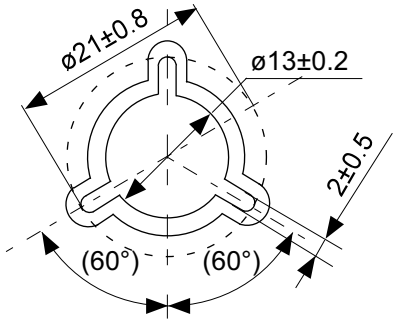


No. MP003-E-C-SD-1.0

TITLE	TSOT233S-A-Carrier Tape
No.	MP003-E-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

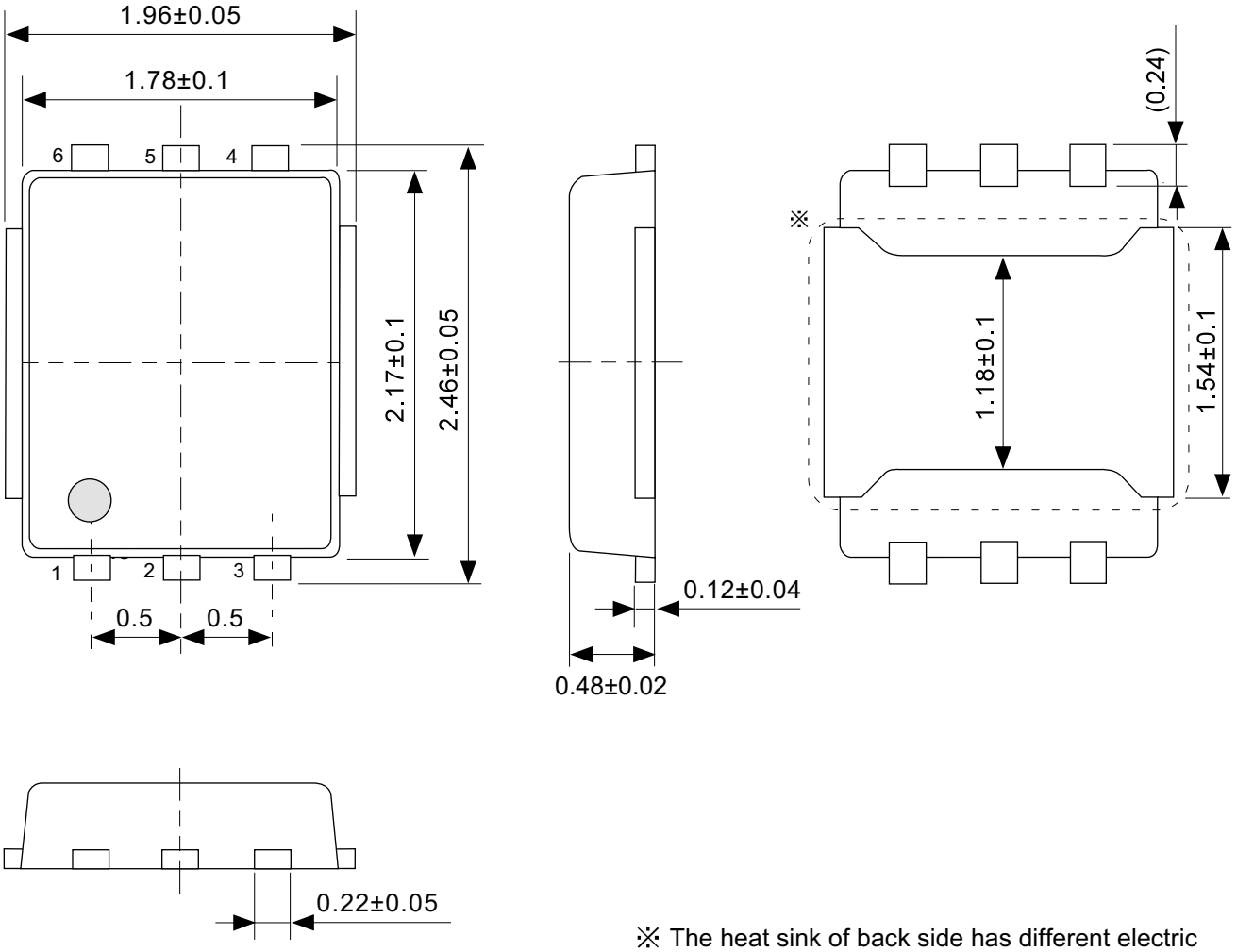


Enlarged drawing in the central part



No. MP003-E-R-SD-1.0

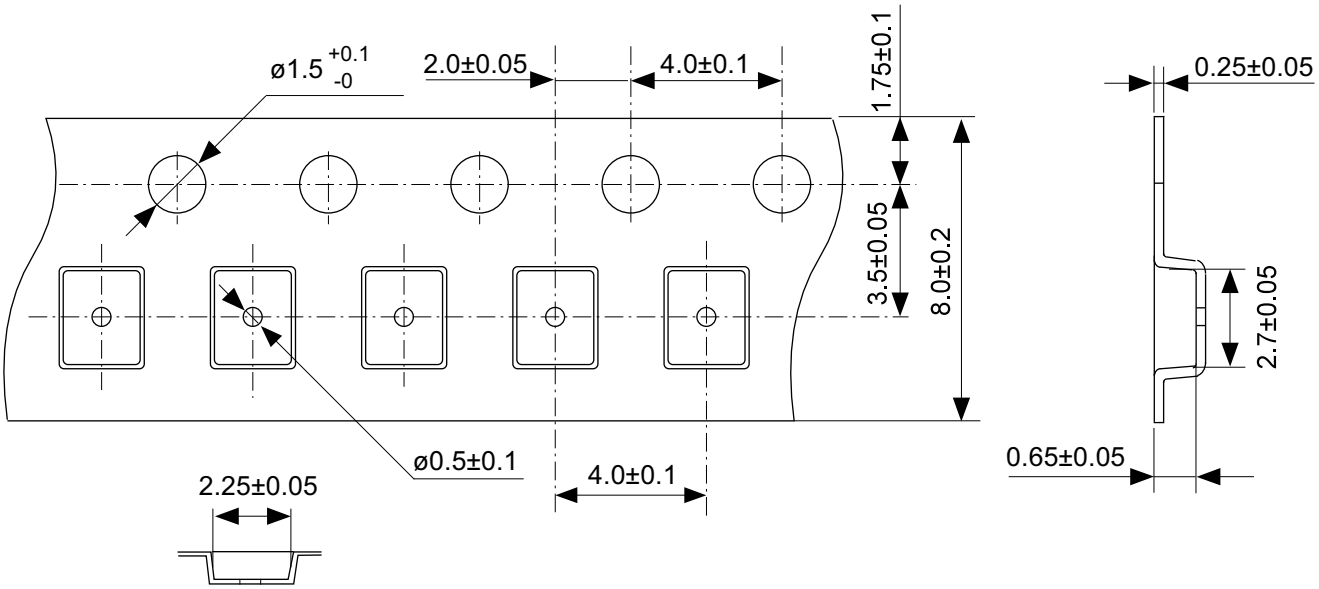
TITLE	TSOT233S-A-Reel		
No.	MP003-E-R-SD-1.0		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			

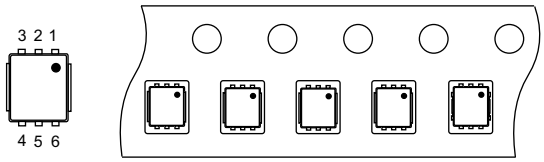


※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

No. PJ006-B-P-SD-1.0

TITLE	HSNT-6-C-PKG Dimensions
No.	PJ006-B-P-SD-1.0
ANGLE	
UNIT	mm
	ABLIC Inc.

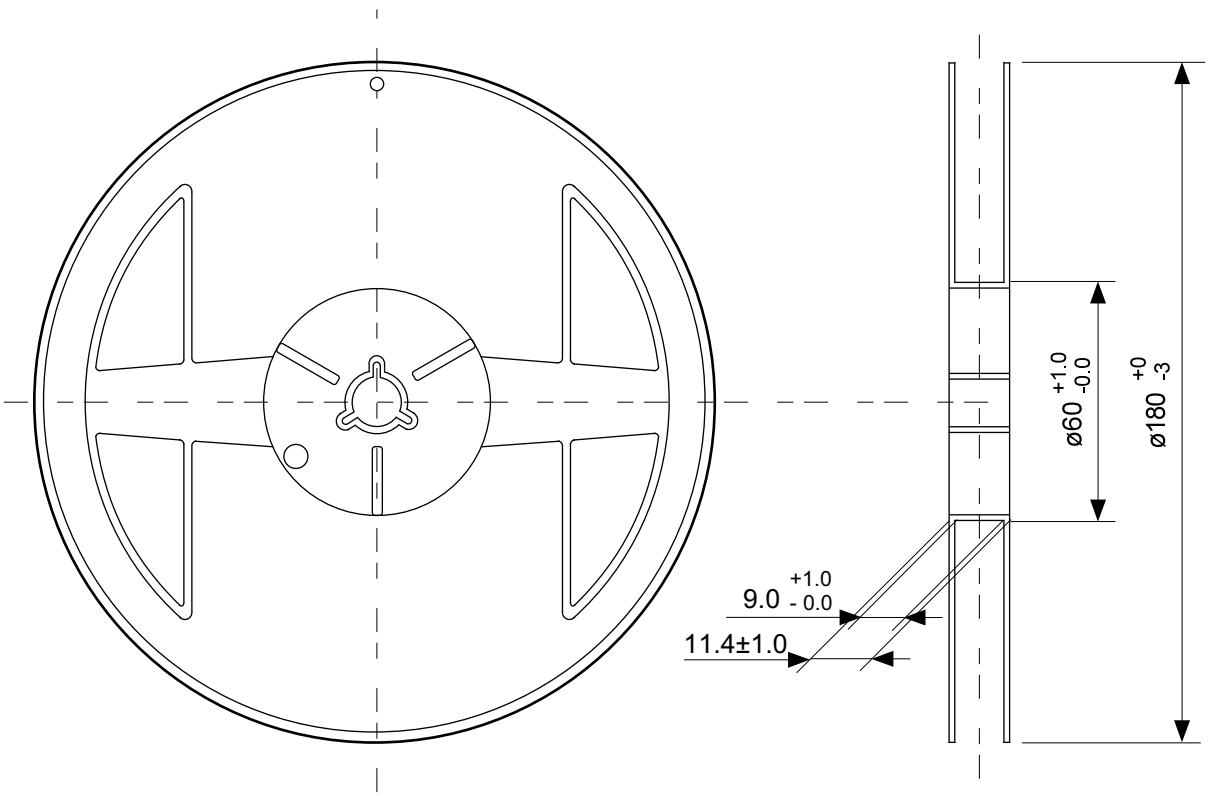




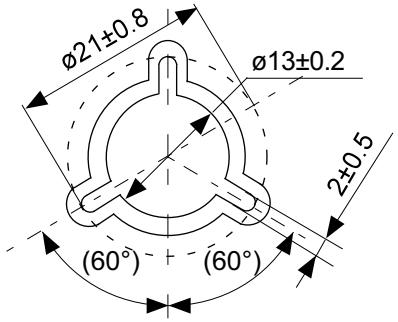
Feed direction

No. PJ006-B-C-SD-1.0

TITLE	HSNT-6-C-Carrier Tape
No.	PJ006-B-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



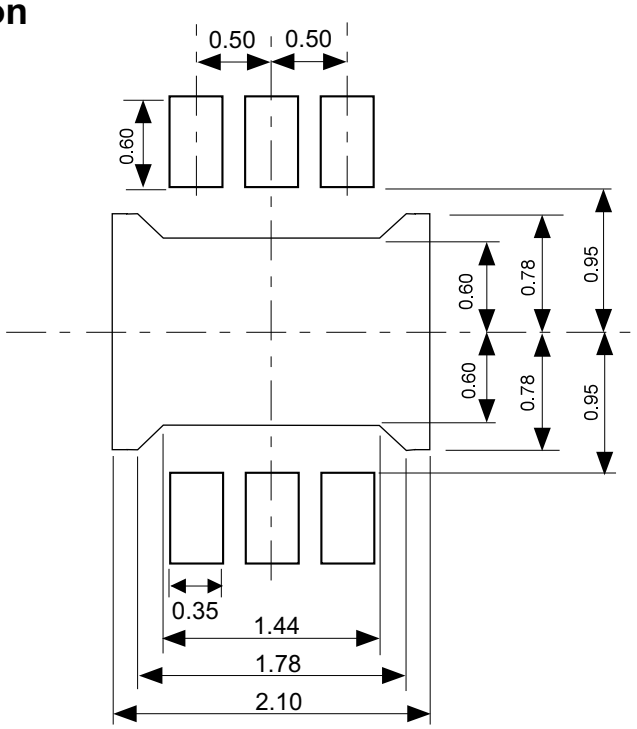
Enlarged drawing in the central part



No. PJ006-B-R-SD-1.0

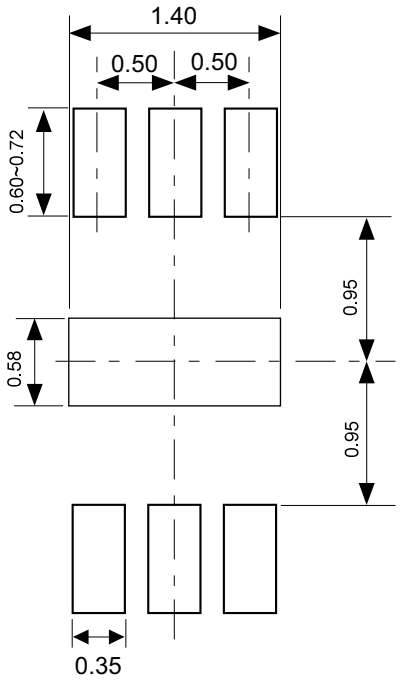
TITLE	HSNT-6-C-Reel		
No.	PJ006-B-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			

Land Recommendation



Caution It is recommended to solder the heat sink to a board in order to ensure the heat radiation.
注意　放熱性を確保する為に、PKGの裏面放熱板（ヒートシンク）を基板に半田付けする事を推奨いたします。

Stencil Opening



No. PJ006-B-LM-SD-1.0

Caution
① Mask aperture ratio of the lead mounting part is 100~120%.
② Mask aperture ratio of the heat sink mounting part is 30%.
③ Mask thickness: t0.12 mm
④ Reflow atmosphere: Nitrogen atmosphere is recommended. (Oxygen concentration: 1000ppm or less)

注意
①リード実装部のマスク開口率は100~120%です。
②放熱板実装のマスク開口率は30%です。
③マスク厚み：t0.12 mm
④リフロー雰囲気・窒素雰囲気（酸素濃度1000ppm以下）推奨

TITLE	HSNT-6-C -Land &Stencil Opening
No.	PJ006-B-LM-SD-1.0
ANGLE	
UNIT	mm
	ABLIC Inc.

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2.4-2019.07