ETHERNET TRANSCEIVERS

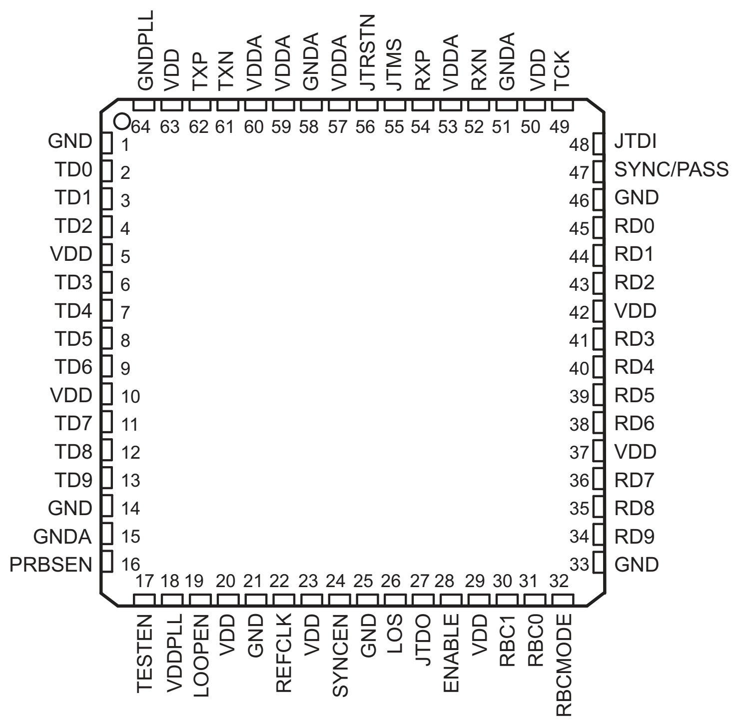
Check for Samples: TLK2211

FEATURES

- **600 mbps to 1.3 Gigabits Per Second (Gbps) Serializer/Deserializer**
- **Low Power Consumption <450 mW Typical at 1.25 Gbps**
- **LVPECL Compatible Differential I/O on High Speed Interface**
- **Single Monolithic PLL Design**
- **Support For 10 Bit Interface**
- **Receiver Differential Input Thresholds 200 mV Minimum**
- **Industrial Temperature Range From –40°C to 85°C**
- **IEEE 802.3 Gigabit Ethernet Compliant**
- **Advanced 0.25 μm CMOS Technology**
- **No External Filter Capacitors Required**
- **Comprehensive Suite of Built-In Testability**
- **IEEE 1149.1 JTAG Support**
- **3.3 V Supply Voltage for Lowest Power Operation**
- **3.3 V Tolerant on LVTTL Inputs**
- **Hot Plug Protection**
- **64 Pin VQFP With Thermally Enhanced Package (PowerPAD™)**

APPLICATIONS

- **Gigabit Ethernet Switches and Routers**
- **Fibre Channel Storage Systems**



DESCRIPTION

The TLK2211 gigabit ethernet transceiver provide for ultrahigh-speed full-duplex point-to-point data transmissions. These devices are based on the timing requirements of the 10-bit interface specification by the IEEE 802.3 Gigabit Ethernet specification. The TLK2211 supports data rates from 1.0 Gbps through 1.3 Gbps.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

The primary application of this device is to provide building blocks for point-to-point baseband data transmission over controlled impedance media of 50 Ω or 75 Ω. The transmission media can be printed-circuit board traces, copper cables or fiber-optical media. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The TLK2211 performs the data serialization, deserialization, and clock extraction functions for a physical layer interface device. The transceiver operates at 1.25 Gbps (typical), providing up to 1 Gbps of data bandwidth over a copper or optical media interface.

The TLK2211 supports a standard 10-bit interface (TBI) . In the TBI mode the serializer/deserializer (SERDES) accepts 10-bit wide 8b/10b parallel encoded data bytes. The parallel data bytes are serialized and transmitted differentially at PECL compatible voltage levels. The SERDES extracts clock information from the input serial stream and deserializes the data, outputting a parallel 10-bit data byte.

The TLK2211 provides a comprehensive series of built-in tests for self-test purposes including loopback and pseudo random binary sequence (PRBS) generation and verification. An IEEE 1149.1 JTAG port is also supported.

The TLK2211 is housed in a high performance, thermally enhanced, 64-pin VQFP PowerPAD package. Use of the PowerPAD package does not require any special considerations except to note that the PowerPAD, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. It is recommended that the TLK2211 PowerPADs be soldered to the thermal land on the board.

The TLK2211 is characterized for operation from –40°C to 85°C.

The TLK2211 use a 3.3-V supply. The I/O section is 3.3-V compatible. With the 3.3-V supply the chipset is very power-efficient, dissipating less than 600 mW typical power when operating at 1.25 Gbps.

The TLK2211 is designed to be hot plug capable. A power-on reset causes RBC0, RBC1, the parallel output signal terminals, TXP, and TXN to be held in high-impedance state.

Differences Between TLK2211, and TNETE2201

The TLK2211 is a functional equivalent of the TNETE2201. There are several differences between the devices as noted below. Refer to Figure 10 in the application information section for an example of a typical application circuit.

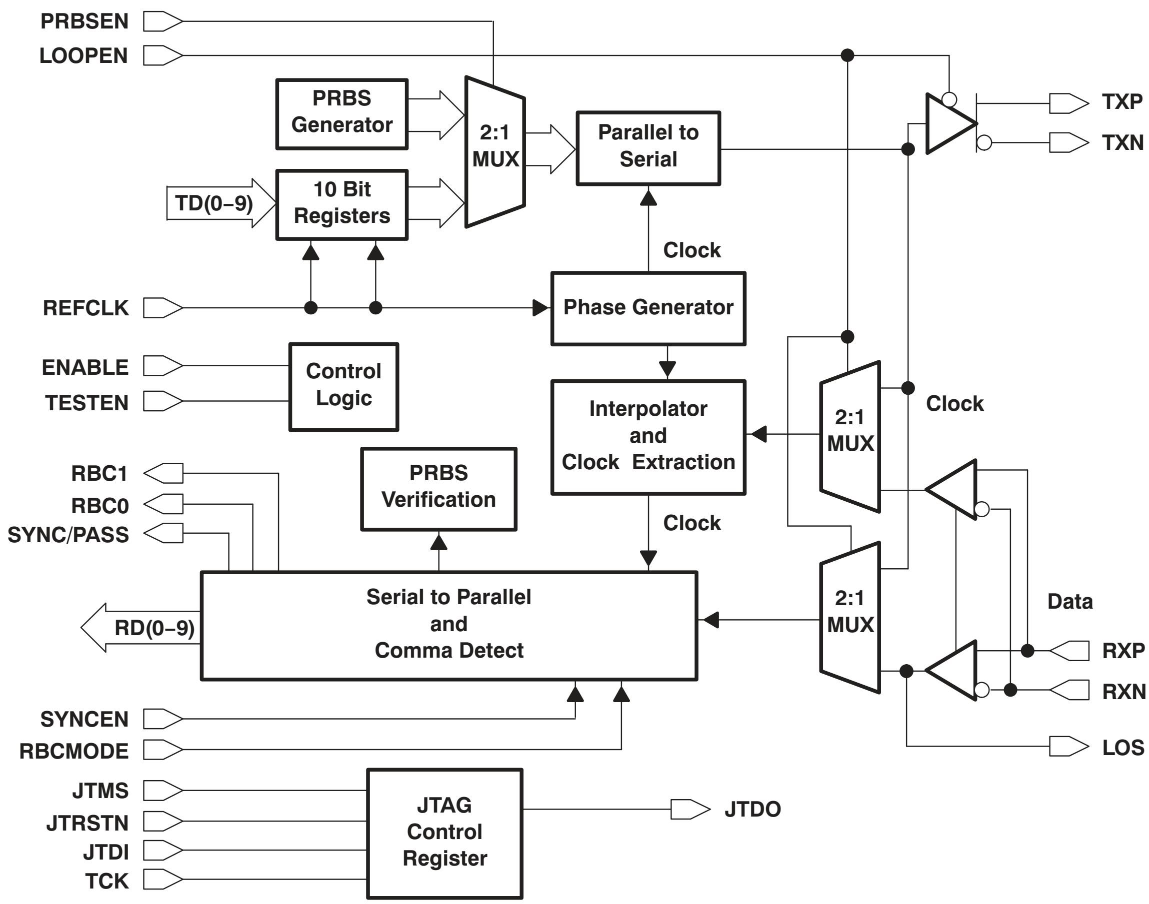
- The PLL filter capacitors on pins 16, 17, 48, and 49 of the TNETE2201 are no longer required. The TLK2211 uses these pins to provide added test capabilities. The capacitors, if present, do not affect the operation of the device.
- No pulldown resistors are required on the TXP/TXN outputs.

AVAILABLE OPTIONS

T_A	PACKAGE[(1)]
	PLASTIC QUAD FLAT PACK (RCP)
–40°C to 85°C	TLK2211RCP
	TLK2211RCPR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
SIGNAL			
TXP TXN	62 61	PECL O	Differential output transmit. TXP and TXN are differential serial outputs that interface to a copper or an optical I/F module. TXP and TXN are put in a high-impedance state when LOOPEN is high and are active when LOOPEN is low.
RXP RXN	54 52	PECL I	Differential input receive. RXP and RXN together are the differential serial input interface from a copper or an optical I/F module.
REFCLK	22	I	Reference clock. REFCLK is an external input clock that synchronizes the receiver and transmitter interface (100 MHz to 160 MHz). The transmitter uses this clock to register the input data (TD0-TD9) for serialization. The data (TDx) is registered on the rising edge of REFCLK.
TD0–TD9	2–4, 6–9, 11–13	I	Transmit data. During normal operation these inputs carry 10-bit parallel data output from a protocol device to the transceiver for serialization and transmission. This 10-bit parallel data is clocked into the transceiver on the rising edge of REFCLK and transmitted as a serial stream with TD0 sent as the first bit.
RD0–RD9	45, 44, 43, 41, 40, 39, 38, 36, 35, 34	O	Receive data. These outputs carry 10-bit parallel data output from the transceiver to the protocol layer. The data is referenced to terminals RBC0 and RBC1, depending on the receive clock mode selected. RD0 is the first bit received.

TERMINAL FUNCTIONS (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RBC0 RBC1	31 30	O	Receive byte clock. RBC0 and RBC1 are recovered clocks used for synchronizing the 10-bit output data on RD0-RD9. The operation of these clocks is dependent upon the receive clock mode selected. In the half-rate mode, the 10-bit output data words are valid on the rising edges of RBC0 and RBC1. These clocks are adjusted to half-word boundaries in conjunction with synchronous detect. The clocks are always expanded during data realignment and never slivered or truncated. RBC0 registers bytes 1 and 3 of received data. RBC1 registers bytes 0 and 2 of received data.
RBCMODE	32	I P/D(1)	RBCMODE must be held low for normal operation (TBI Half Rate Mode).
SYNCEN.	24	I P/U(2)	Synchronous function enable. When SYNCEN is high, the internal synchronization function is activated. When this function is activated, the transceiver detects the K28.5 comma character (0011111 negative beginning disparity) in the serial data stream and realigns data on byte boundaries if required. When SYNCEN is low, serial input data is unframed in RD0–RD9.
SYNC/PASS	47	O	Synchronous detect. The SYNC output is asserted high upon detection of the comma pattern in the serial data path. SYNC pulses are output only when SYNCEN is activated (asserted high). In PRBS test mode (PRBSEN=high), SYNC/PASS outputs the status of the PRBS test results (high=pass).
LOS	26	O	Loss of signal. Indicates a loss of signal on the high-speed differential inputs RXP and RXN. If magnitude of RXP–RXN > 150 mV, LOS = 1, valid input signal If magnitude of RXP–RXN < 150 mV and >50 mV, LOS is undefined If magnitude of RXP–RXN < 50 mV, LOS = 0, loss of signal
TEST			
LOOPEN	19	I (P/D)	Loop enable. When LOOPEN is high (active), the internal loop-back path is activated. The transmitted serial data is directly routed to the inputs of the receiver. This provides a self-test capability in conjunction with the protocol device. The TXP and TXN outputs are held in a high-impedance state during the loop-back test. LOOPEN is held low during standard operational state with external serial outputs and inputs active.
TCK	49	I	Test clock. IEEE1149.1 (JTAG)
JTDI	48	I (P/D)	Test data input. IEEE1149.1 (JTAG)
JTDO	27	O	Test data output. IEEE1149.1 (JTAG)
JTRSTN	56	I P/U(2)	Reset signal. IEEE1149.1 (JTAG)
JTMS	55	I P/U(2)	Test mode select. IEEE1149.1 (JTAG)
ENABLE	28	I P/U(2)	When this terminal is low, the device is disabled for Iddq testing. RD0 - RD9, RBCn, TXP, and TXN are high impedance. The pullup and pulldown resistors on any input are disabled. When ENABLE is high, the device operates normally.
PRBSEN	16	I P/D(1)	PRBS enable. When PRBSEN is high, the PRBS generation circuitry is enabled. The PRBS verification circuit in the receive side is also enabled. A PRBS signal can be fed to the receive inputs and checked for errors, that are reported by the SYNC/PASS terminal indicating low.
TESTEN	17	I P/D(1)	Manufacturing test terminal
POWER			
VDD	5, 10, 20, 23, 29, 37, 42, 50, 63	Supply	Digital logic power. Provides power for all digital circuitry and digital I/O buffers.
VDDA	53, 57, 59, 60	Supply	Analog power. VDDA provides power for the high-speed analog circuits, receiver, and transmitter.
VDDPLL	18	Supply	PLL power. Provides power for the PLL circuitry. This terminal requires additional filtering.
GROUND			
GNDA	15, 51,58	Ground	Analog ground. GNDA provides a ground for the high-speed analog circuits, RX and TX.
GND	1, 14, 21, 25, 33, 46	Ground	Digital logic ground. Provides a ground for the logic circuits and digital I/O buffers.
GNDPLL	64	Ground	PLL ground. Provides a ground for the PLL circuitry.

(1) P/D = Internal pulldown
(2) P/U = Internal pullup

DETAILED DESCRIPTION

DATA TRANSMISSION

This device supports the standard 10-bit interface (TBI) parallel bus.

In the TBI mode, the transmitter portion registers incoming 10-bit wide data words (8b/10b encoded data, TD0-TD9) on the rising edge of REFCLK. The REFCLK is also used by the serializer, which multiplies the clock by a factor of 10, providing a signal that is fed to the shift register. The 8b/10b encoded data is transmitted sequentially bit 0 through 9 over the differential high-speed I/O channel.

TRANSMISSION LATENCY

Data transmission latency is defined as the delay from the initial 10-bit word load to the serial transmission of bit 9. The minimum latency in TBI mode is 19 bit times. The maximum latency in TBI mode is 20 bit times.

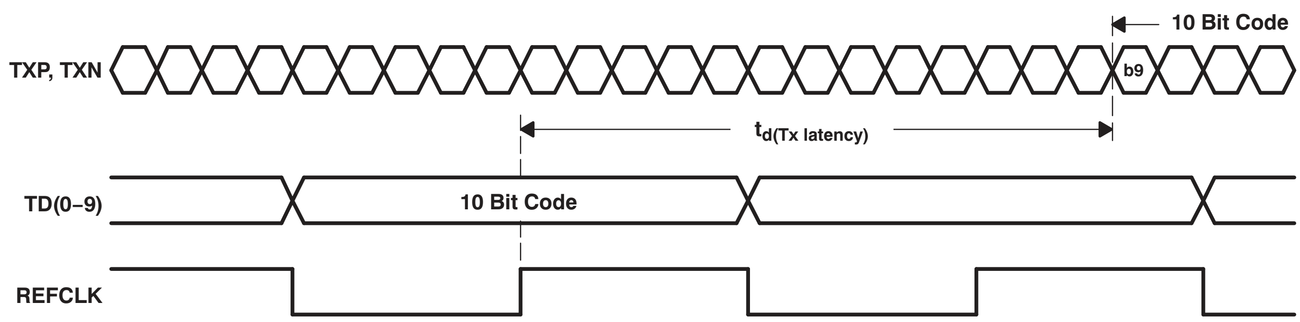


Figure 1. Transmitter Latency

DATA RECEPTION

The receiver portion deserializes the differential serial data. The serial data is retimed based on an interpolated clock generated from the reference clock. The serial data is then aligned to the 10-bit word boundaries and presented to the protocol controller along with receive byte clocks (RBC0, RBC1).

RECEIVER CLOCK SELECT MODE

There is only one mode of operation for the parallel busses that is the 10-bit (TBI) mode. In TBI mode, the supported clock mode is half-rate clocks on RBC0 and RBC1. Table 1.

Table 1. Mode Selection

RBCMODE	MODE	FREQUENCY (TLK2211)
0	TBI half-rate	60–130 MHz

In this mode, two receive byte clocks (RBC0 and RBC1) are 180 degrees out of phase and operate at one-half the data rate. The clocks are generated by dividing down the recovered clock. The received data is output with respect to the two receive byte clocks (RBC0, RBC1) allowing a protocol device to clock the parallel bytes using the RBC0 and RBC1 rising edges. The outputs to the protocol device, byte 0 of the received data valid on the rising edge of RBC1. See the timing diagram shown in Figure 2.

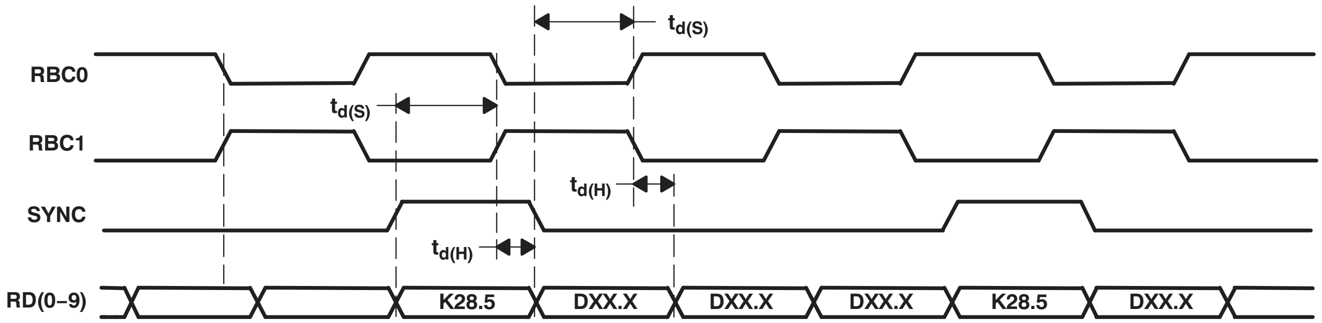


Figure 2. Synchronous Timing Characteristics Waveforms (TBI half-rate mode)

The receiver clock interpolator can lock to the incoming data without the need for a lock-to-reference preset. The received serial data rate (RXP and RXN) is at the same baud rate as the transmitted data stream, ±0.02% (200 PPM) for proper operation.

RECEIVER WORD ALIGNMENT

These devices use the IEEE 802.3 Gigabit Ethernet defined 10-bit K28.5 character (comma character) word alignment scheme. The following sections explain how this scheme works and how it realigns itself.

Comma Character on Expected Boundary

These devices provide 10-bit K28.5 character recognition and word alignment. The 10-bit word alignment is enabled by forcing the SYNCEN terminal high. This enables the function that examines and compares serial input data to the seven bit synchronization pattern. The K28.5 character is defined by the 8-bit/10-bit coding scheme as a pattern consisting of 0011111010 (a negative number beginning with disparity) with the 7 MSBs (0011111), referred to as the comma character. The K28.5 character was implemented specifically for aligning data words. As long as the K28.5 character falls within the expected 10-bit boundary, the received 10-bit data is properly aligned and data realignment is not required. Figure 2 shows the timing characteristics of RBC0, RBC1, SYNC and RD0-RD9 while synchronized. (Note: the K28.5 character is valid on the rising edge of RBC1).

Comma Character Not on Expected Boundary

If synchronization is enabled and a K28.5 character straddles the expected 10-bit word boundary, then word realignment is necessary. Realignment or shifting the 10-bit word boundary truncates the character following the misaligned K28.5, but the following K28.5 and all subsequent data is aligned properly as shown in Figure 3. The RBC0 and RBC1 pulse widths are stretched or stalled in their current state during realignment. With this design the maximum stretch that occurs is 20 bit times. This occurs during a worst case scenario when the K28.5 is aligned to the falling edge of RBC1 instead of the rising edge. Figure 3 shows the timing characteristics of the data realignment.

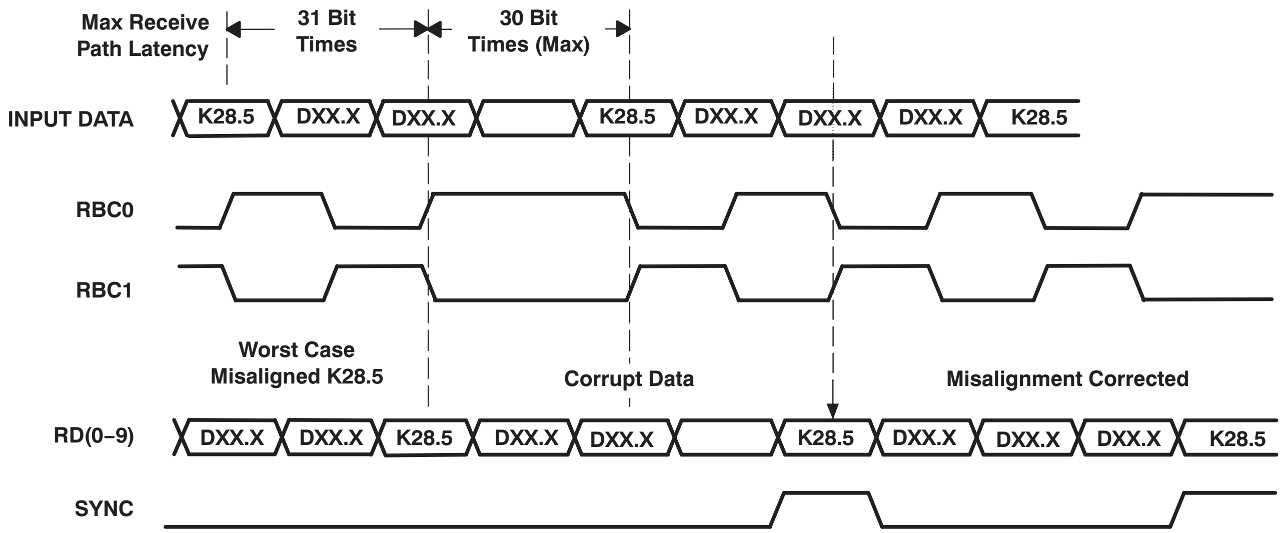


Figure 3. Word Realignment Timing Characteristics Waveforms

Systems that do not require framed data may disable byte alignment by tying SYNCEN low.

When a SYNC character is detected, the SYNC signal is brought high and is aligned with the K28.5 character. The duration of the SYNC pulse is equal to the duration of the data when in TBI mode.

DATA RECEPTION LATENCY

The serial to parallel data latency is the time from when the first bit arrives at the receiver until it is output in the aligned parallel word with RD0 received as first bit. The minimum latency in TBI mode is 21 bit times and the maximum latency is 31 bit times.

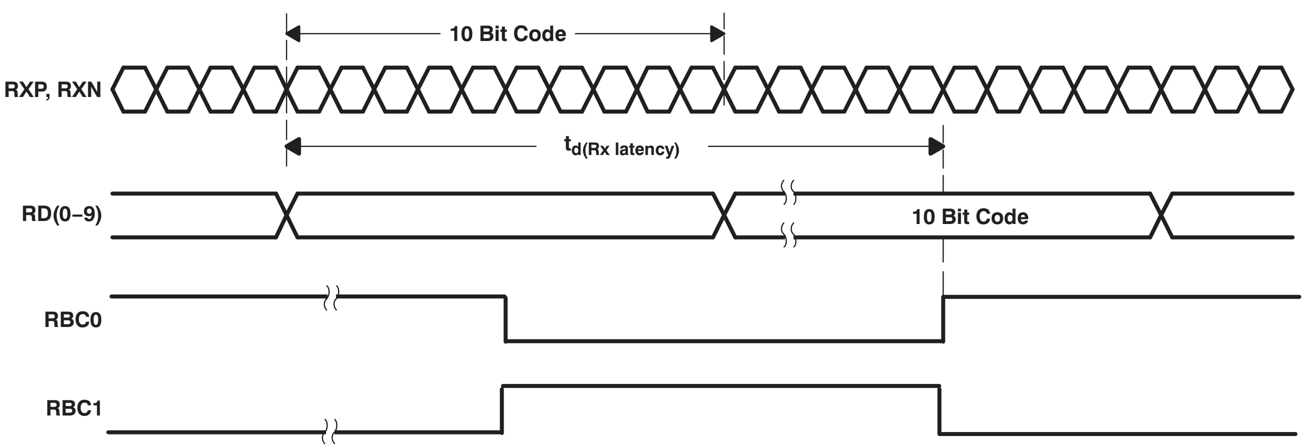


Figure 4. Receiver Latency – TBI Half-Rate Mode Shown

LOSS OF SIGNAL DETECTION

These devices have a loss of signal (LOS) detection circuit for conditions where the incoming signal no longer has sufficient voltage level to keep the clock recovery circuit in lock. The LOS is intended to be an indication of gross signal error conditions, such as a detached cable or no signal being transmitted, and not an indication of signal coding health. Under a PRBS serial input pattern, LOS is high for signal amplitudes greater than 150 mV. The LOS is low for all amplitudes below 50 mV. Between 50 mV and 150 mV, LOS is undetermined.

TESTABILITY

The loopback function provides for at-speed testing of the transmit/receive portions of the circuitry. The enable function allows for all circuitry to be disabled so that an Iddq test can be performed. The PRBS function also allows for a BIST(built-in self test). The terminal setting, TESTEN high, enables the test mode. The terminal TESTEN has an internal pulldown resistor, so it defaults to normal operation. The TESTEN is only used for factory testing, and is not intended for the end-user.

LOOPBACK TESTING

The transceiver can provide a self-test function by enabling (LOOPEN to high level) the internal loopback path. Enabling this function causes serial transmitted data to be routed internally to the receiver. The parallel data output can be compared to the parallel input data for functional verification. (The external differential output is held in a high-impedance state during the loopback testing.)

ENABLE FUNCTION

When held low, ENABLE disables all quiescent power in both the analog and digital circuitry. This allows an ultralow-power idle state when the link is not active.

PRBS FUNCTION

These devices have a built-in 2^7-1 PRBS function. When the PRBSEN control bit is set high, the PRBS test is enabled. A PRBS is generated and fed into the 10-bit parallel transmitter input bus. Data from the normal parallel input source is ignored during PRBS test mode. The PRBS pattern is then fed through the transmit circuitry as if it were normal data and sent out to the transmitter. The output can be sent to a bit error rate tester (BERT) or to the receiver of another TLK2211. Since the PRBS is not really random and is really a predetermined sequence of ones and zeros, the data can be captured and checked for errors by a BERT. These devices also have a built-in BERT function on the receiver side that is enabled by PRBSEN. It can receive a PRBS pattern and check for errors, and then reports the errors by forcing the SYNC/PASS terminal low. The PRBS testing supports two modes (normal and latched), which are controlled by the SYNCEN input. When SYNCEN is low, the result of the PRBS bit error rate test is passed to the SYNC/PASS terminal. When SYNCEN is high the result of the PRBS verification is latched on the SYNC/PASS output (i.e., a single failure forces SYNC/PASS to remain low).

JTAG

The TLK2211 supports an IEEE1149.1 JTAG function while maintaining compatibility with the industry standard 64 pin QFP package footprint. In this way, the TLK2211 installed on a board layout that was designed for the industry standard footprint such as for the TNETE2211. The JTAG pins on the TLK2211 are chosen to either be on the ‘vender-unique’ pins of the industry standard footprint, or are on pins that were previously power or ground. The TRSTN pin has been placed on pin 56, which is a ground on the industry standard footprint. In this way, a TLK2211 installed onto the older footprint has the JTAG tap controller held in reset, and thus disabled. If the JTAG function is desired, then the 5 JTAG pins TRSTN, TMS, TCK, TDI, and TDO can be used in the usual manner for a JTAG function. If the JTAG function is not desired, then connecting TRSTN to ground is recommended. TMS and TDI have internal pullup resistors, and can thus be left unconnected if not used. TDO is an output and should be left unconnected if JTAG is not used. TCK does not have an internal pullup, and can be tied to GND or PWR if not used, but with TRSTN low, this input is not used, and thus can be left unconnected.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V_{DD}	Supply voltage(2)		–0.3 to 3.6	V
V_I	Input voltage range at TTL terminals		–0.5 to 4	V
	Input voltage range at any other terminal		–0.3 to V_{DD} +0.3	V
T_{stg}	Storage temperature		–65 to 150	°C
	Electrostatic discharge	CDM	1	kV
		HDM	2	kV
	Characterized free-air operating temperature range	TLK2211	–40 to 85	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

THERMAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board-mounted, no air flow, high conductivity TI recommended test board, chip soldered or greased to thermal land; Assumes High K Board		21.47		°C/W
		Board-mounted, no air flow, high conductivity TI recommended test board with thermal land but no solder or grease thermal connection to thermal land		42.20		
		Board-mounted, no air flow, JEDEC test board		75.83		
$R_{\theta JC}$	Junction-to-case-thermal resistance	Board-mounted, no air flow, high conductivity TI recommended test board, chip soldered or greased to thermal land		0.38		°C/W
		Board-mounted, no air flow, high conductivity TI recommended test board with thermal land but no solder or grease thermal connection to thermal land		0.38		
		Board-mounted, no air flow, JEDEC test board		7.8		

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
V_{DD}, $V_{DD(A)}$	Supply voltage			3	3.3	3.6	V
I_{DD}, $I_{DD(A)}$	Total supply current	Frequency = 1.25 Gbps,	PRBS pattern		140		mA
		Frequency = 1.25 Gbps,	Worst case pattern(1)			230	
P_D	Total power dissipation	Frequency = 1.25 Gbps,	PRBS pattern		460		mW
		Frequency = 1.25 Gbps,	Worst case pattern(1)			850	
I_{DD}, $I_{DD(A)}$	Total shutdown current	Enable = 0,	$V_{DD(A)}$, V_{DD} = 3.6V			75	μA
PLL	Startup lock time	V_{DD}, $V_{DD(A)}$ = 3.3 V, EN↑ to PLL acquire				500	μs
T_A	Operating free-air temperature			–40		85	°C

(1) Worst case pattern is a pattern that creates a maximum transition density on the serial transceiver.

TLK2211 REFERENCE CLOCK (REFCLK) TIMING REQUIREMENTS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency	Minimum data rate	TYP–0.01%	60	TYP–0.01%	MHz
Frequency	Maximum data rate	TYP–0.01%	130	TYP–0.01%	MHz
Accuracy		–100		100	ppm
Duty cycle		40%	50%	60%	
Jitter	Random plus deterministic			40	ps

TTL ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –400 μA		V_{DD} –0.2	3.2		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA		GND	0.25	0.5	V
V_{IH}	High-level input voltage			2		3.6	V
V_{IL}	Low-level input voltage					0.8	V
I_{IH}	Input high current	V_{DD} = 3 V,	V_{IN} = 2 V			40	μA
I_{IL}	Input low current	V_{DD} = 3 V,	V_{IN} = 0.4 V	–40			μA
C_{IN}	Input capacitance					4	pF

TRANSMITTER/RECEIVER CHARACTERISTICS

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Vod = |TxP–TxN|		R_t = 50 Ω	1000	1600	2000	mV
			R_t = 75 Ω	1300	1900	2800	
$V_{(cm)}$	Transmit common mode voltage range		R_t = 50 Ω	1400	1600	1850	mV
			R_t = 75 Ω	1400	1600	1800	
	Receiver Input voltage requirement, Vid = |RxP - RxN|			200		1600	mV
	Receiver common mode voltage range, (RxP + RxN)/2			1400	1590	1785	mV
C_I	Receiver input capacitance					2	pF
$t_{(TJ)}$	Serial data total jitter (peak-to-peak)		Differential output jitter, Random + deterministic, PRBS pattern, R_ω = 125 MHz			0.24	UI
$t_{(DJ)}$	Serial data deterministic jitter (peak-to-peak)		Differential output jitter, PRBS pattern, R_ω = 125 MHz			0.10	UI
t_r, t_f	Differential signal rise, fall time (20% to 80%)		R_L = 50 Ω, C_L = 4 pF, See Figure 5 and Figure 6	80		305	ps
	Serial data jitter tolerance minimum required eye opening, (per IEEE-802.3 specification)		Differential input jitter, Random + deterministic, R_ω = 125 MHz	0.25			UI
	Receiver data acquisition lock time from powerup					500	µs
	Data relock time from loss of synchronization				3750		Bit times
	Data relock time from LOOPEN rising edge		IDLE Pattern (K28.5, D16.2)			100	ms
$t_{d(Tx\ latency)}$	Tx latency	TBI modes	See Figure 1	19		24	UI
$t_{d(Rx\ latency)}$	Rx latency	TBI modes	See Figure 4	25		35	UI

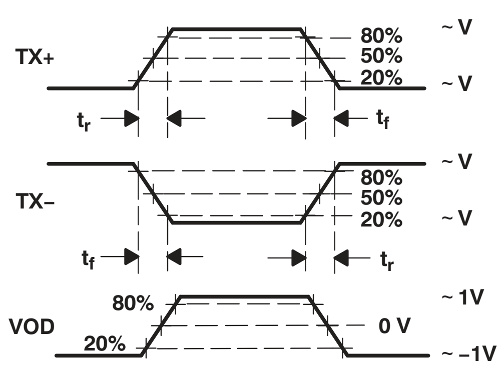


Figure 5. Differential and Common-Mode Output Voltage Definitions

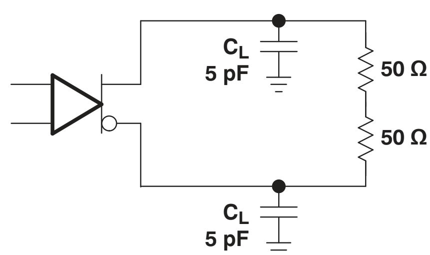


Figure 6. Transmitter Test Setup

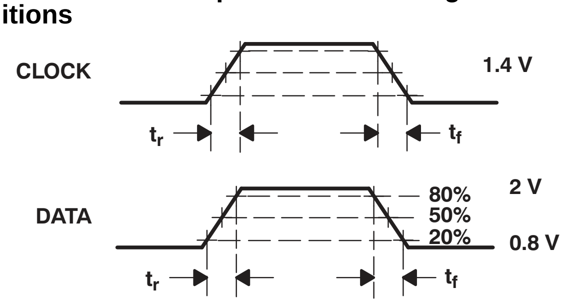


Figure 7. TTL Data I/O Valid Levels for AC Measurement

LVTTL OUTPUT SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r(RBC)}$	Clock rise time	80% to 20% output voltage, C = 5 pF (see Figure 7)	0.3		1.9	ns
$t_{f(RBC)}$	Clock fall time		0.3		1.9	
t_r	Data rise timer		0.3		2.25	ns
t_f	Data fall time		0.3		2.25	
$t_{su(D3)}$	Data setup time (RD0..RD9)	TBI half-rate mode, R_ω = 125 MHz (see Figure 2)	2.5			ns
$t_{h(D3)}$	Data hold time (RD0..RD9)	TBI half-rate mode, R_ω = 125 MHz (see Figure 2)	1.5			ns

TRANSMITTER TIMING REQUIREMENTS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{su(D4)}$	Data setup time (TD0..TD9)	TBI modes	1.6			ns
$t_{h(D4)}$	Data hold time (TD0..TD9)		1			
t_r, t_f	TD[0,9] Data rise and fall time	See Figure 7			2	ns

APPLICATION INFORMATION

8B/10B TRANSMISSION CODE

The PCS maps GMII signals into ten-bit code groups and vice versa, using an 8b/10b block coding scheme. The PCS uses the transmission code to improve the transmission characteristics of information to be transferred across the link. The encoding defined by the transmission code ensures that sufficient transitions are present in the PHY bit stream to make clock recovery possible in the receiver. Such encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. The 8b/10b transmission code specified for use has a high transition density, is run length limited, and is dc-balanced. The transition density of the 8b/10b symbols ranges from 3 to 8 transitions per symbol. The definition of the 8b/10b transmission code is specified in IEEE 802.3 Gigabit Ethernet and ANSI X3.230-1994 (FC−PH), clause 11.

8b/10b transmission code uses letter notation describing the bits of an unencoded information octet. The bit notation of A,B,C,D,E,F,G,H for an unencoded information octet is used in the description of the 8b/10b transmission code-groups, where A is the LSB. Each valid code group has been given a name using the following convention: /Dx.y/ for the 256 valid data code-groups and /Kx.y/ for the special control code-groups, where y is the decimal value of bits EDCBA and x is the decimal value of bits HGF (noted as K<HGF.EDCBA>). Thus, an octet value of FE representing a code-group value of K30.7 would be represented in bit notation as 111 11110.

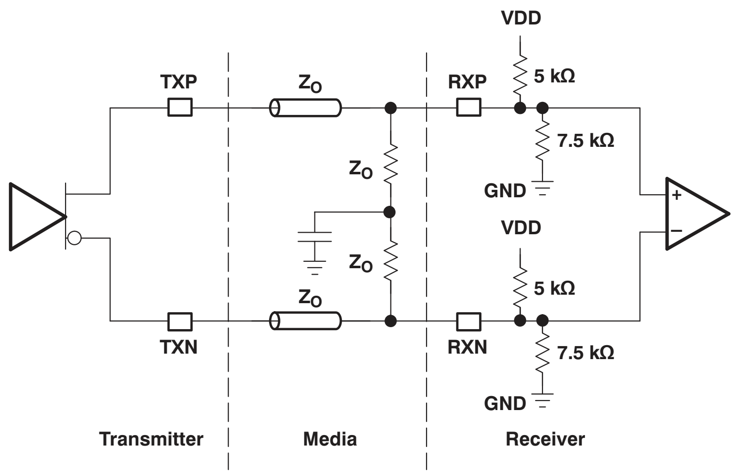


Figure 8. High-Speed I/O Directly-Coupled Mode

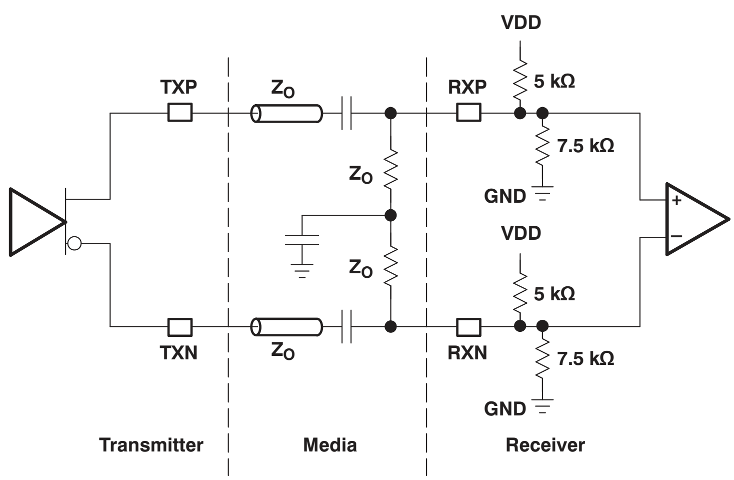


Figure 9. High-Speed I/O AC-Coupled Mode

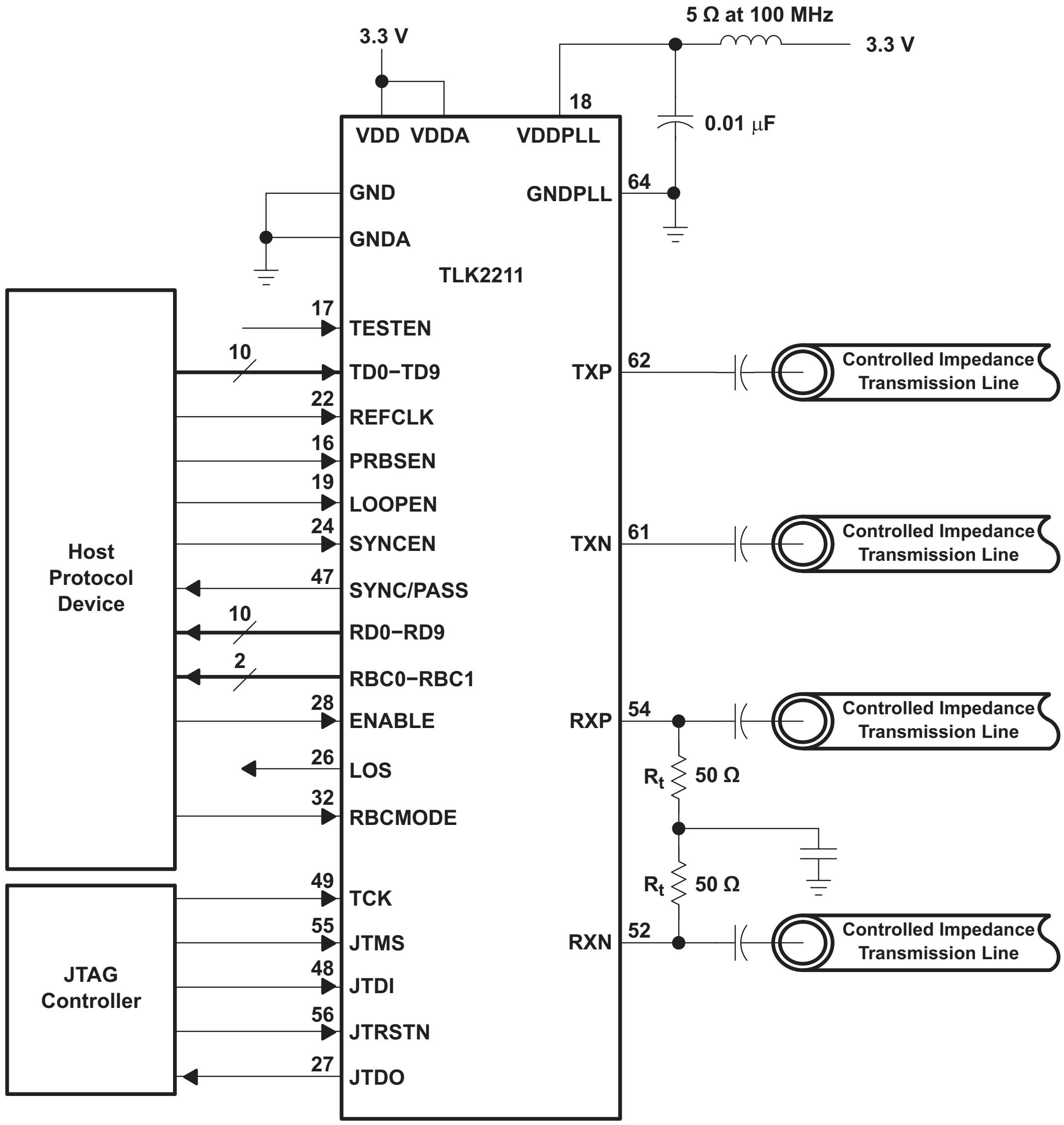


Figure 10. Typical Application Circuit (AC Mode)

DESIGNING WITH PowerPAD

The TLK2211 is housed in a high performance, thermally enhanced, 64-pin VQFP (RCP64) PowerPAD package. Use of the PowerPAD package does not require any special considerations except to note that the PowerPAD, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. Therefore, if not implementing PowerPAD PCB features, the use of solder masks (or other assembly techniques) may be required to prevent any inadvertent shorting by the exposed PowerPAD of connection etches or vias under the package. It is strongly recommended that the PowerPAD be soldered to the thermal land. The recommended convention, however, is to not run any etches or signal vias under the device, but to have only a grounded thermal land as explained below. Although the actual size of the exposed die pad may vary, the minimum size required for the keep out area for the 64-pin PFP PowerPAD package is 8 mm × 8 mm.

It is recommended that there be a thermal land, which is an area of solder-tinned-copper, underneath the PowerPAD package. The thermal land varies in size depending on the PowerPAD package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land may or may not contain numerous thermal vias depending on PCB construction.

Other requirements for thermal lands and thermal vias are detailed in the TI application note *PowerPAD Thermally Enhanced Package Application Report* (SLMA002), available via the TI Web pages beginning at URL: http://www.ti.com.

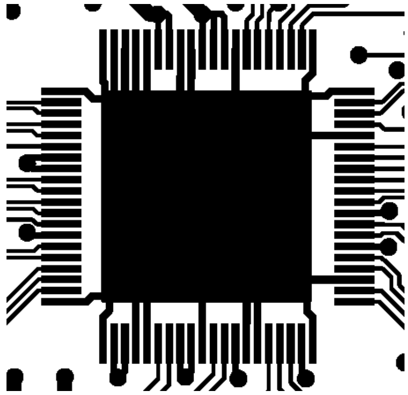


Figure 11. Example of a Thermal Land

For the TLK2211, this thermal land must be grounded to the low-impedance ground plane of the device. This improves not only thermal performance but also the electrical grounding of the device. It is also recommended that the device ground pin landing pads be connected directly to the grounded thermal land. The land size must be as large as possible without shorting device signal pins. The thermal land may be soldered to the exposed PowerPAD using standard reflow soldering techniques.

While the thermal land may be electrically floated and configured to remove heat to an external heat sink, it is recommended that the thermal land be connected to the low-impedance ground plane for the device. More information may be obtained from the TI application note *PHY Layout* (SLLA020).

REVISION HISTORY

Note: Page numbers of current version may differ from previous versions

Changes from Revision C (October 2008) to Revision D **Page**

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