

T-66-21-51



# 54F/74F352 Dual 4-Input Multiplexer

## General Description

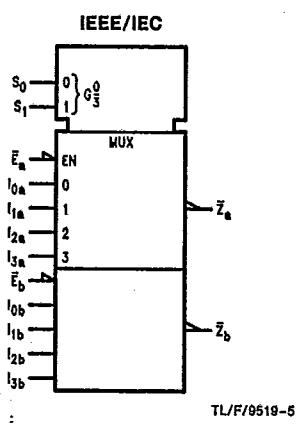
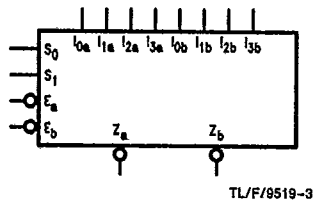
The 'F352 is a very high-speed dual 4-input multiplexer with common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The 'F352 is the functional equivalent of the 'F153 except with inverted outputs.

## Features

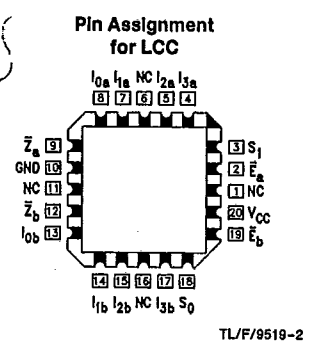
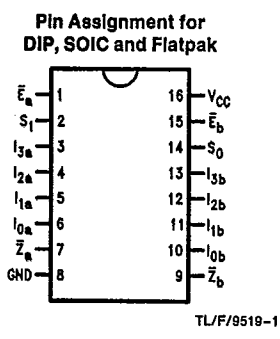
- Inverted version of 'F153
- Separate enables for each multiplexer
- Input clamp diode limits high speed termination effects

**Ordering Code:** See Section 5

## Logic Symbols



## Connection Diagrams



**Unit Loading/Fan Out:** See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$I_{0a}-I_{3a}$	Side A Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$I_{0b}-I_{3b}$	Side B Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$S_0-S_1$	Common Select Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\bar{E}_a$	Side A Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\bar{E}_b$	Side B Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$Z_a, Z_b$	Multiplexer Outputs (Inverted)	50/33.3	-1 mA/20 mA



7-66-21-51

### Functional Description

The 'F352 is a dual 4-input multiplexer. It selects two bits of data from up to four sources under the control of the common Select inputs ( $S_0, S_1$ ). The two 4-input multiplexer circuits have individual active LOW Enables ( $\bar{E}_a, \bar{E}_b$ ) which can be used to strobe the outputs independently. When the Enables ( $\bar{E}_a, \bar{E}_b$ ) are HIGH, the corresponding outputs ( $Z_a, Z_b$ ) are forced HIGH.

The 'F352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The 'F352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

The logic equations for the outputs are shown below:

$$Z_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot S_0 + I_{3a} \cdot S_1 \cdot \bar{S}_0)$$

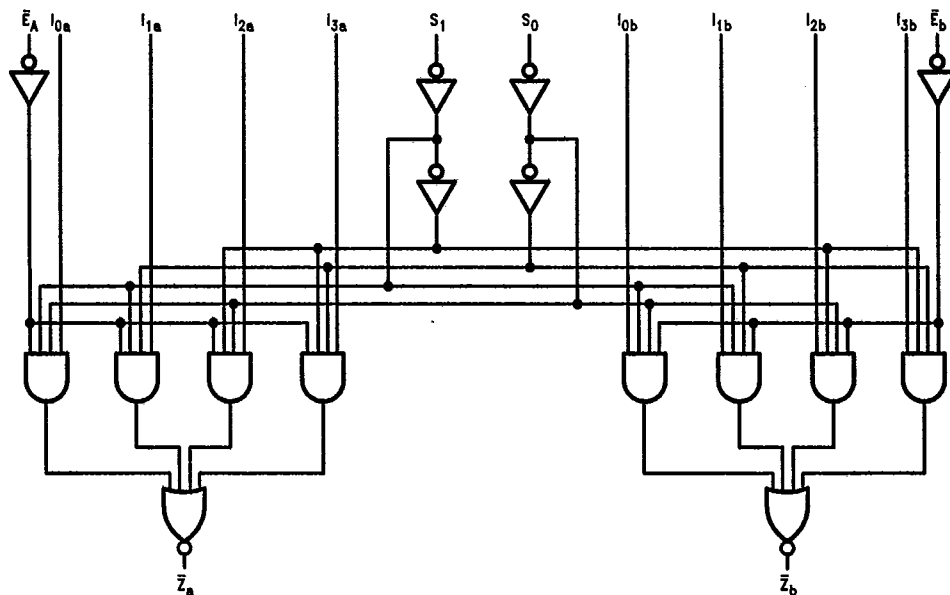
$$Z_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot S_0 + I_{3b} \cdot S_1 \cdot \bar{S}_0)$$

### Truth Table

Select Inputs		Inputs (a or b)					Output
$S_0$	$S_1$	$\bar{E}$	$I_0$	$I_1$	$I_2$	$I_3$	$Z$
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

### Logic Diagram



TL/F/9519-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

352

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE <sup>®</sup> Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

7-66-21-51

**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				
		74F 5% V <sub>CC</sub>	2.7				
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		9.3	14	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		13.3	20	mA	Max	V <sub>O</sub> = LOW

4

352

T-66-21-51

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S <sub>n</sub> to Z <sub>n</sub>	4.0	8.0	11.0	3.5	14.0	3.5	12.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay E <sub>n</sub> to Z <sub>n</sub>	3.0	4.5	6.0	2.5	8.0	2.5	7.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Z <sub>n</sub>	2.0	5.2	7.0	2.0	9.0	2.0	8.0	ns	2-3