

SN54BCT544, SN74BCT544 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS039B – NOVEMBER 1988 – REVISED NOVEMBER 1993

- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Power-Up High-Impedance State
- 3-State Inverting Outputs
- Back-to-Back Registers for Storage
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Plastic and Ceramic 300-mil DIPs (JT, NT)

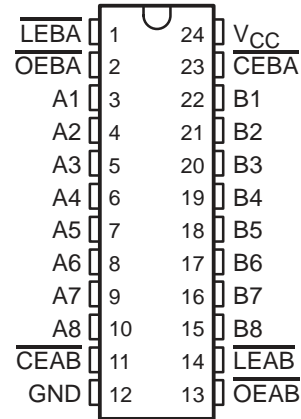
description

The 'BCT544 octal registered transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (\overline{LEAB} or \overline{LEBA}) and output-enable (\overline{OEAB} or \overline{OEBA}) inputs are provided for each register to permit independent control in either direction of data flow.

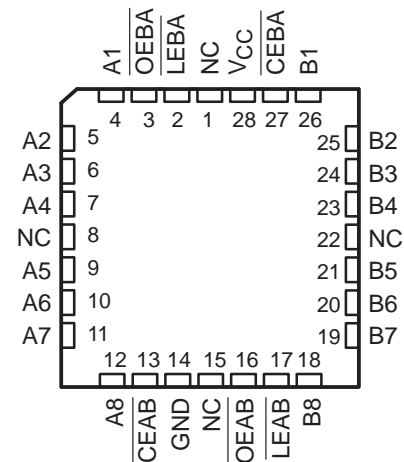
The A-to-B enable (\overline{CEAB}) input must be low in order to enter data from A or to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent; a subsequent low-to-high transition of \overline{LEAB} puts the A latches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the inverted data present at the output of the A latches. Data flow from B to A is similar, but requires using the \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs.

The SN54BCT544 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74BCT544 is characterized for operation from 0°C to 70°C .

SN54BCT544 . . . JT OR W PACKAGE
SN74BCT544 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54BCT544 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE†

INPUTS				OUTPUT
\overline{CEAB}	\overline{LEAB}	\overline{OEAB}	A	B
H	X	X	X	Z
L	X	H	X	Z
L	H	L	X	B_0^{\ddagger}
L	L	L	L	H
L	L	L	H	L

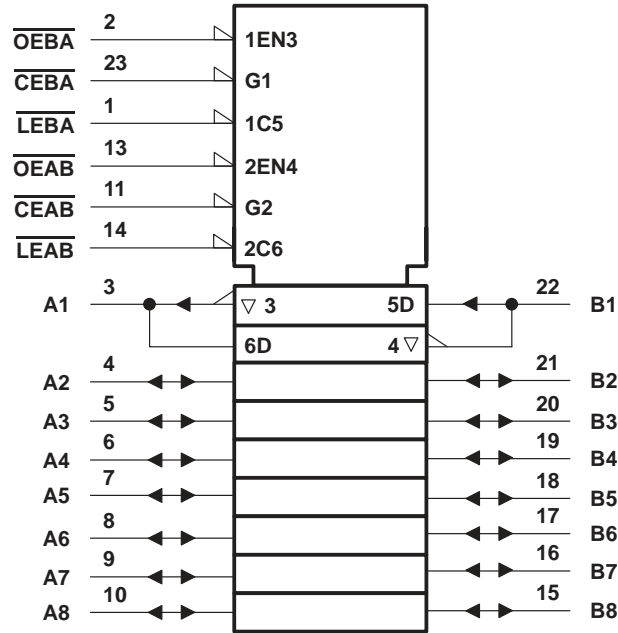
† A-to-B data flow is shown; B-to-A flow control is the same except that it uses \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} .

‡ Output level before the indicated steady-state input conditions were established.

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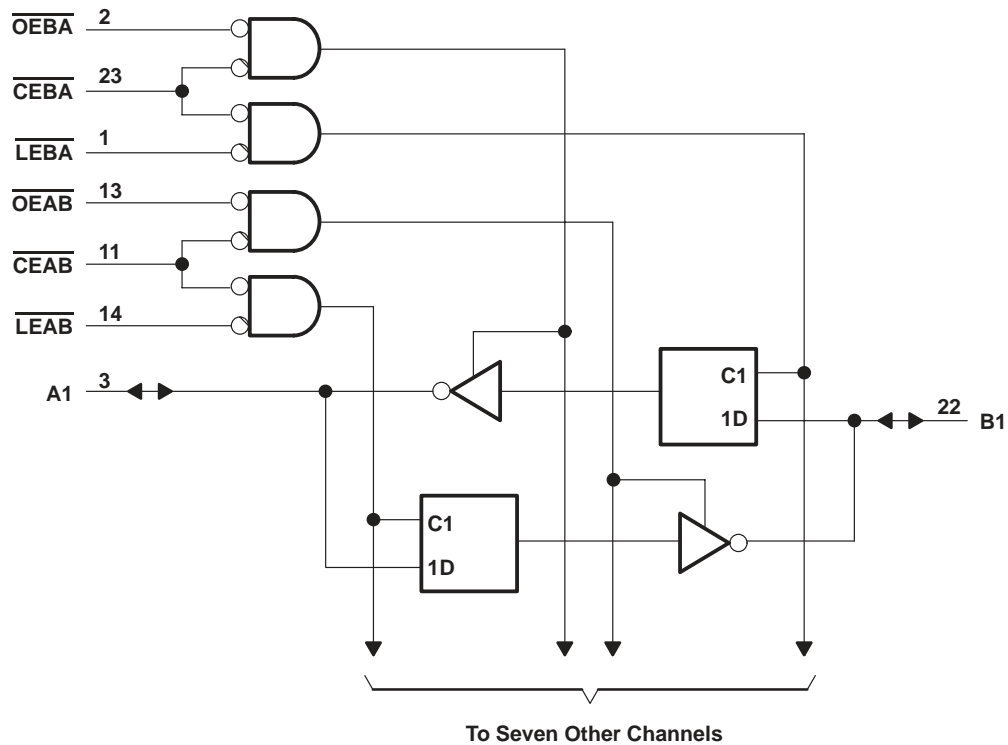
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	– 0.5 V to 7 V
Input voltage range: Control inputs (see Note 1)	– 0.5 V to 7 V
I/O ports (see Note 1)	– 0.5 V to 5.5 V
Voltage range applied to any output in the disabled or power-off state, V_O	– 0.5 V to 7 V
Voltage range applied to any output in the high state, V_O	– 0.5 V to V_{CC}
Input clamp current	– 30 mA
Current into any output in the low state: SN54BCT544	96 mA
SN74BCT544	128 mA
Operating free-air temperature range: SN54BCT544	– 55°C to 125°C
SN74BCT544	0°C to 70°C
Storage temperature range	– 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp-current rating is observed.

recommended operating conditions

		SN54BCT544			SN74BCT544			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			–18			–18	mA
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	–55		125	0		70	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT544		SN74BCT544		UNIT		
			MIN	TYP†	MAX	MIN		TYP†	MAX
V_{IK}	$V_{CC} = 4.5 V$,	$I_I = -18 mA$			-1.2		-1.2	V	
V_{OH}	$V_{CC} = 4.5 V$	$I_{OH} = -3 mA$	2.4	3.3		2.4	3.3	V	
		$I_{OH} = -12 mA$	2	3.2					
		$I_{OH} = -15 mA$				2	3.1		
	$V_{CC} = 4.75 V$,	$I_{OH} = -3 mA$				2.7			
V_{OL}	$V_{CC} = 4.5 V$	$I_{OL} = 48 mA$		0.38	0.55			V	
		$I_{OL} = 64 mA$					0.42		0.55
I_I	$V_{CC} = 5.5 V$,	$V_I = 5.5 V$			0.4		0.4	mA	
I_{IH}^{\ddagger}	$V_{CC} = 5.5 V$,	$V_I = 2.7 V$			20		20	μA	
I_{IL}^{\ddagger}	$V_{CC} = 5.5 V$,	$V_I = 0.5 V$			-0.6		-0.6	mA	
I_{OS}^{\S}	$V_{CC} = 5.5 V$,	$V_O = 0$	-100		-225	-100		-225	mA
I_{CCH}	$V_{CC} = 5.5 V$			7	11		7	11	mA
I_{CCL}	$V_{CC} = 5.5 V$			43	68		43	68	mA
I_{CCZ}	$V_{CC} = 5.5 V$			9	15		9	15	mA
C_i	$V_{CC} = 5 V$,	$V_I = 2.5 V$ or $0.5 V$		6			6		pF
C_{io}	$V_{CC} = 5 V$,	$V_O = 2.5 V$ or $0.5 V$		16			16		pF

† All typical values are at $V_{CC} = 5 V$, $T_A = 25^\circ C$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		$V_{CC} = 5 V$, $T_A = 25^\circ C$		SN54BCT544		SN74BCT544		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, \overline{LEAB} or \overline{LEBA} low	7		8		7		ns
t_{su}	Setup time, data before \overline{LEAB} or $\overline{LEBA}^{\uparrow}$	5		5.5		5		ns
t_h	Hold time, data after \overline{LEAB} or $\overline{LEBA}^{\uparrow}$	1		1		1		ns

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$ (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$		SN54BCT544		SN74BCT544		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.4	7.6	2.4	10.3	2.4	9.7	ns
t_{PHL}			3	7.6	3	8.9	3	8.5	
t_{PLH}	\overline{LEBA}	A	3.5	10.3	3.5	14.2	3.5	13.3	ns
t_{PHL}			4.8	10.2	4.8	12.7	4.8	12.3	
t_{PLH}	\overline{LEAB}	B	3.5	10.3	3.5	14.4	3.5	13.4	ns
t_{PHL}			4.8	10.3	4.8	12.8	4.8	12.4	
t_{PZH}	\overline{OE} or \overline{CE}	A or B	3	10.1	3	13.1	3	12.7	ns
t_{PZL}			5.1	11.8	5.1	14.2	5.1	13.9	
t_{PHZ}	\overline{OE} or \overline{CE}	A or B	2.8	7.5	2	8.9	2.8	8.5	ns
t_{PLZ}			2.3	7.2	2.3	9	2.3	8.2	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74BCT544DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	0 to 70		
SN74BCT544DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	0 to 70		
SN74BCT544NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
SNJ54BCT544FK	OBSOLETE	LCCC	FK	28		TBD	Call TI	Call TI	-55 to 125		
SNJ54BCT544JT	OBSOLETE	CDIP	JT	24		TBD	Call TI	Call TI	-55 to 125		
SNJ54BCT544W	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54BCT544, SN74BCT544 :

- Catalog: [SN74BCT544](#)
- Military: [SN54BCT544](#)

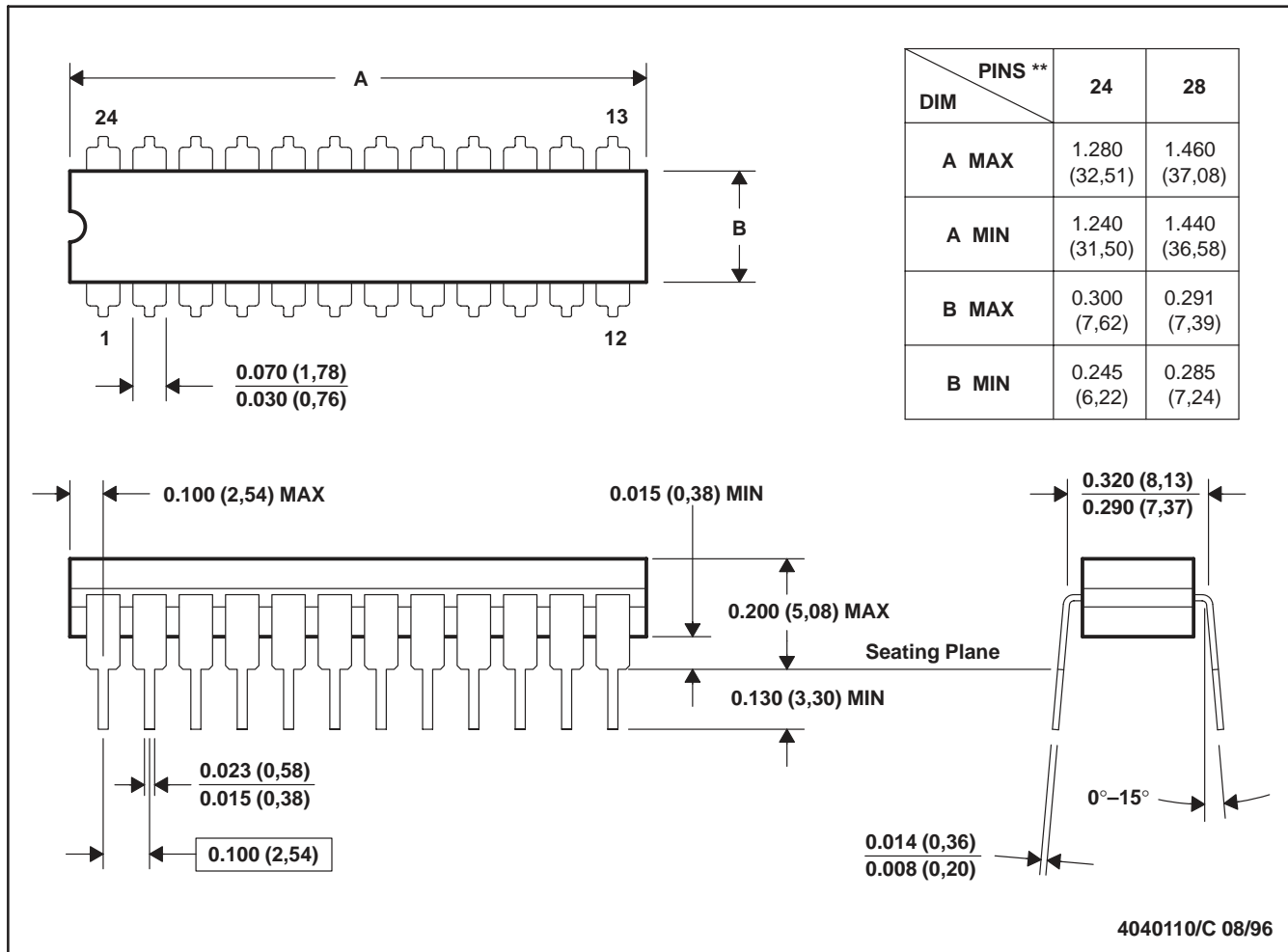
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

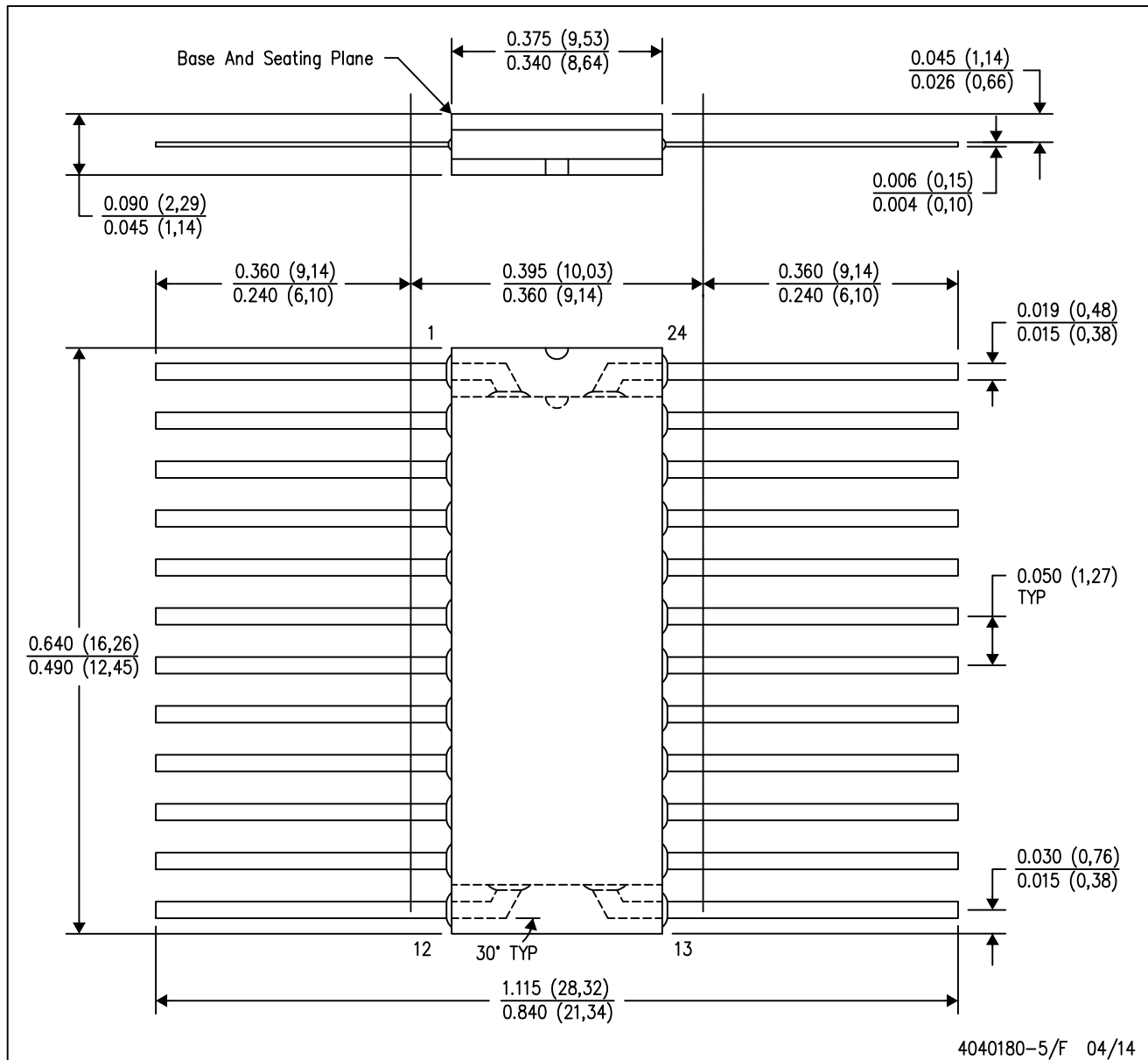
24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK

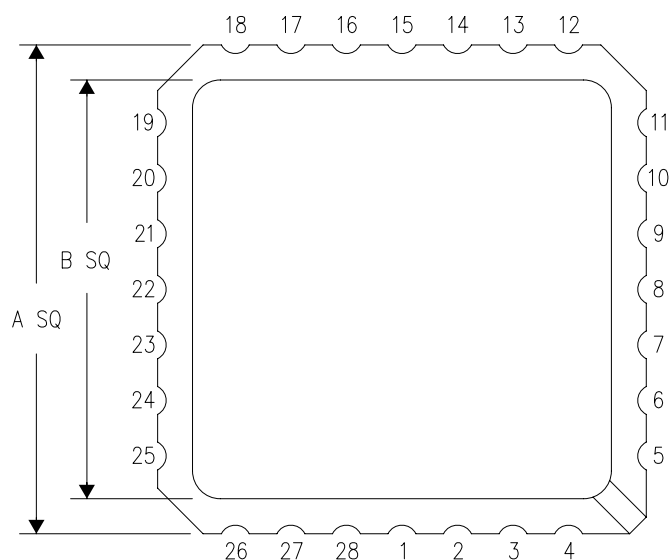


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

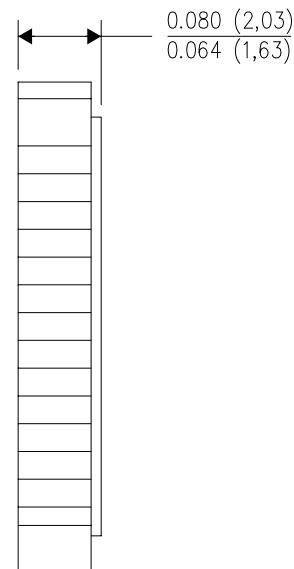
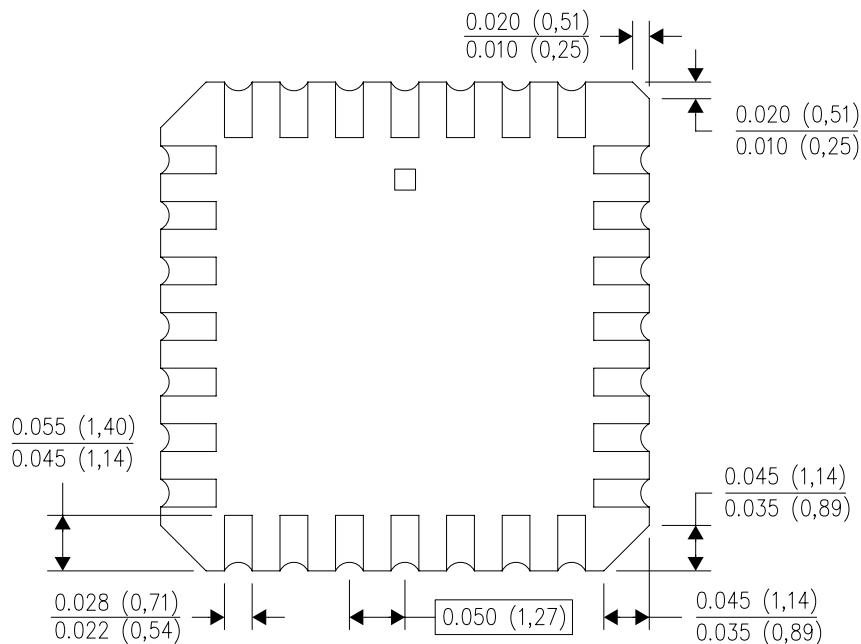
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



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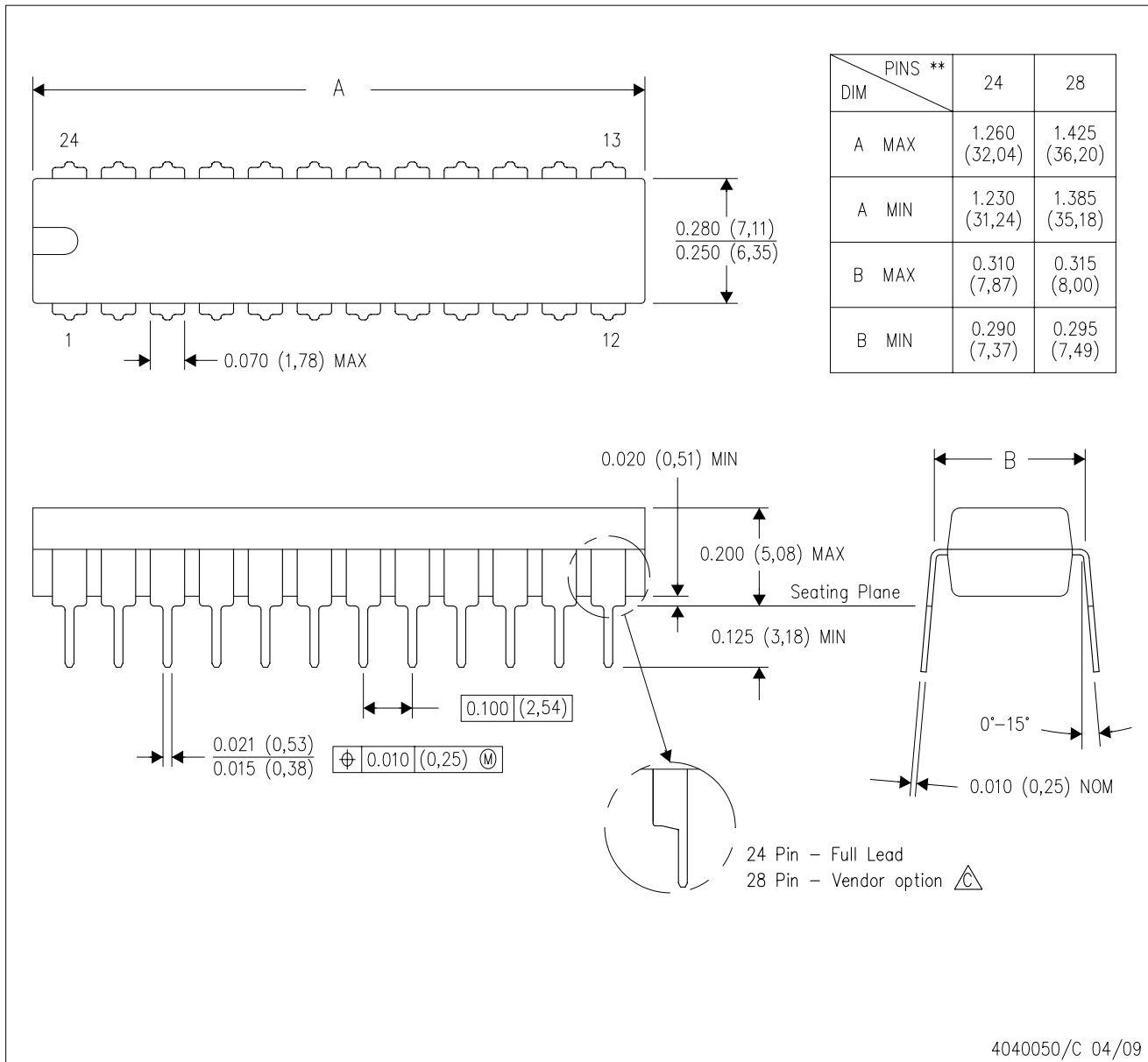
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. Falls within JEDEC MS-004

MECHANICAL DATA

NT (R-PDIP-T**)


PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



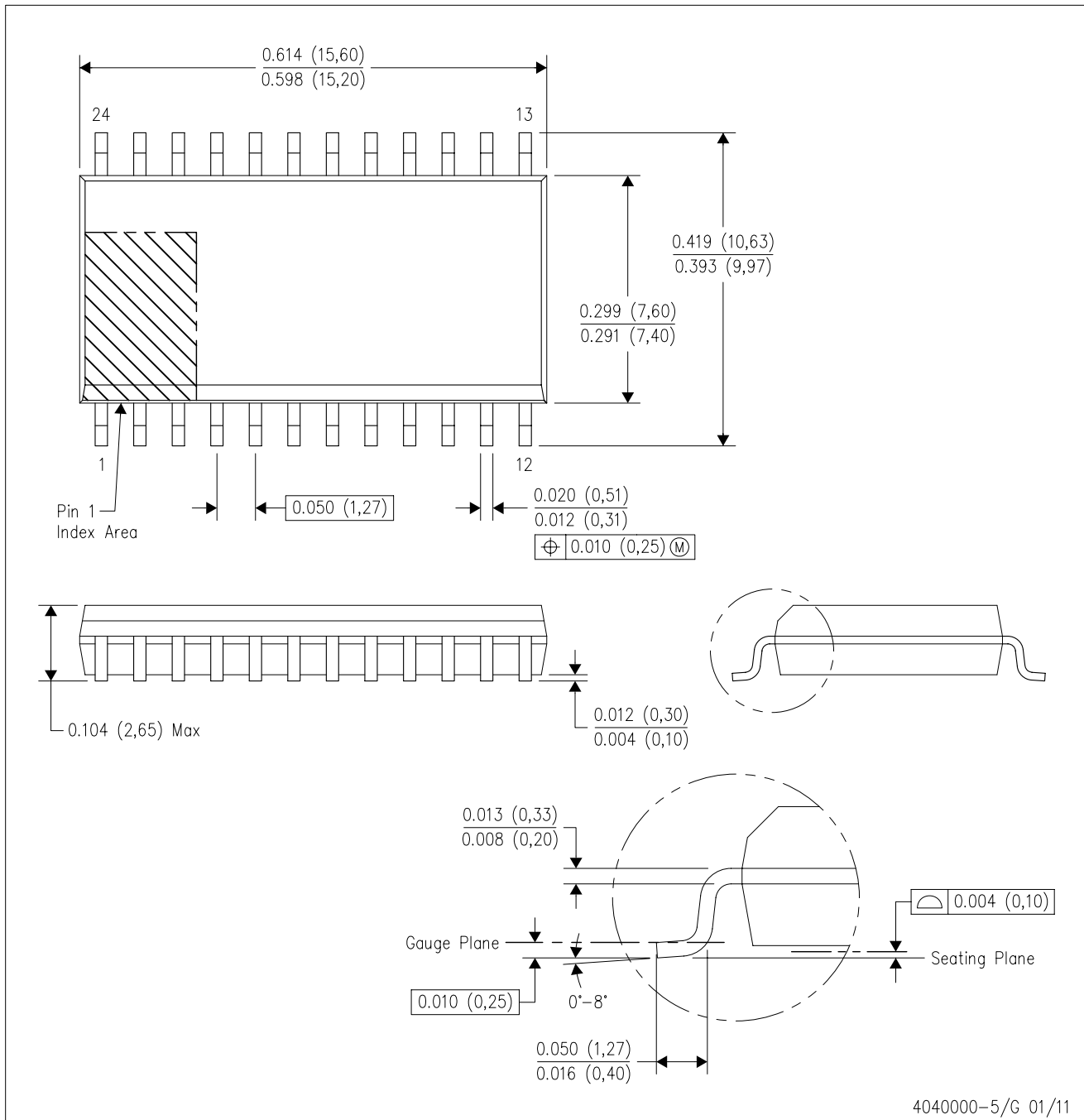
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

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