TEXAS INSTRUMENTS

TL5002EVM-180

DDR Power Supply EVM Using TL5002 (Synchronous Buck Controller)

User's Guide

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Power Management Products

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Preface

About This Manual

This user's guide describes the SLVP180C synchronous buck converter evaluation module.

How to Use This Manual

- ❏ Chapter 1 Introduction
- ❏ Chapter 2 Design Procedure
- ❏ Chapter 3 Test Results

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation

1) Electronic Industries Alliance, JEDEC Solid State Technologies Division, EIA/JEDEC STANDARD; STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2), EIA/JESD8–0, September 1998

2) Texas Instruments application report *Designing With The TL5001 PWM Controller* (literature number SLVA034A)

3) Texas Instruments data sheet TL5002 (literature number SLVS304)

4) Texas Instruments data sheet TL5001 (literature number SLVS84E)

5) Bob Mammano, *Fueling the Megaprocessor Empowering Dynamic Energy Management,* power supply design seminar (SEM–1200), Unitrode application note 1997

6) Larry Spaziani, *Fueling the Megaprocessor – A DC/DC Converter Design Review Featuring The UC3886 and UC3910*, Unitrode application note U–157, 1997

7) Abraham I. Pressman, *Switching Power Supply Design*, second edition, McGraw Hill

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Chapter 1

Introduction

The TL5002EVM–180 synchronous buck converter evaluation module (SLVP180C) provides a reference design for evaluating the performance of a double data rate (DDR) power supply using the TL5002 pulse-width-modulation (PWM) controller coupled with a TPS2837 MOSFET driver. The device contains all of the circuitry necessary to control a switch-mode power supply in a voltage-mode configuration. This manual explains how to construct basic power conversion circuits including the design of the control chip functions and the basic loop.

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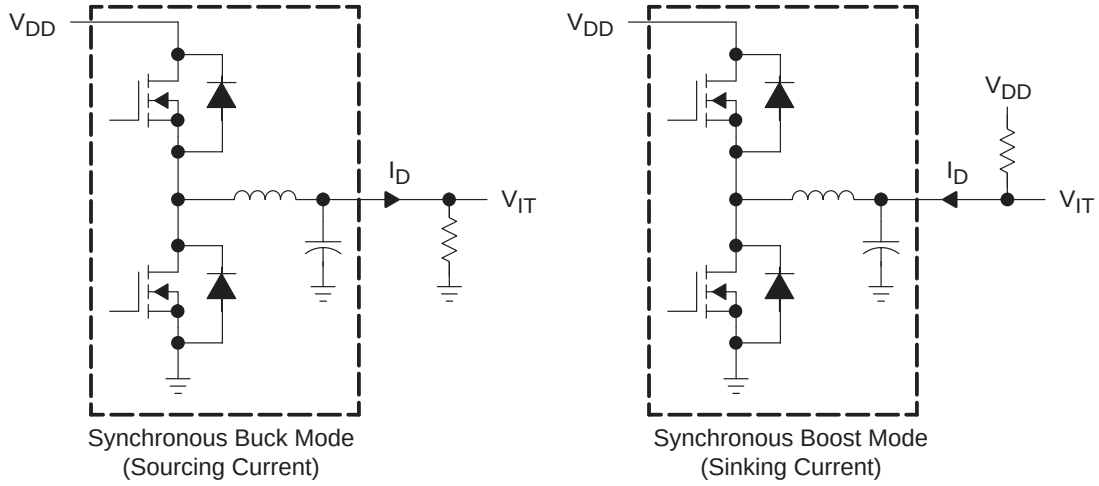
1.1 DDR Power Supply Operation

This user's guide presents an example DDR design of 12 A of output current with voltage outputs between 0.9 V and 1.5 V. This solution is provided for the power supply operating as a traditional buck power stage in the sourcing mode as well as operation as a synchronous boost regulator in the sinking mode. Figure 1–1 shows the power supply topology for DDR Bus termination power requirements. Depending on output current demands, the circuit operates in two modes. With a sourcing requirement, the circuit operates as a synchronous buck power stage taking input power from the source and providing it to the load. However, with a sinking requirement, the circuit operates as a synchronous boost power stage taking power from the output and returning it to the input. These two different operating modes create challenges in maintaining good efficiency and good transient response.

Figure 1–1. Two Operating Modes of the DDR Power Supply



1.2 Operating Specifications

This section summarizes the performance specifications of the SLVP180C converter. Table 1–1 lists the operating specifications for the SLVP180C.

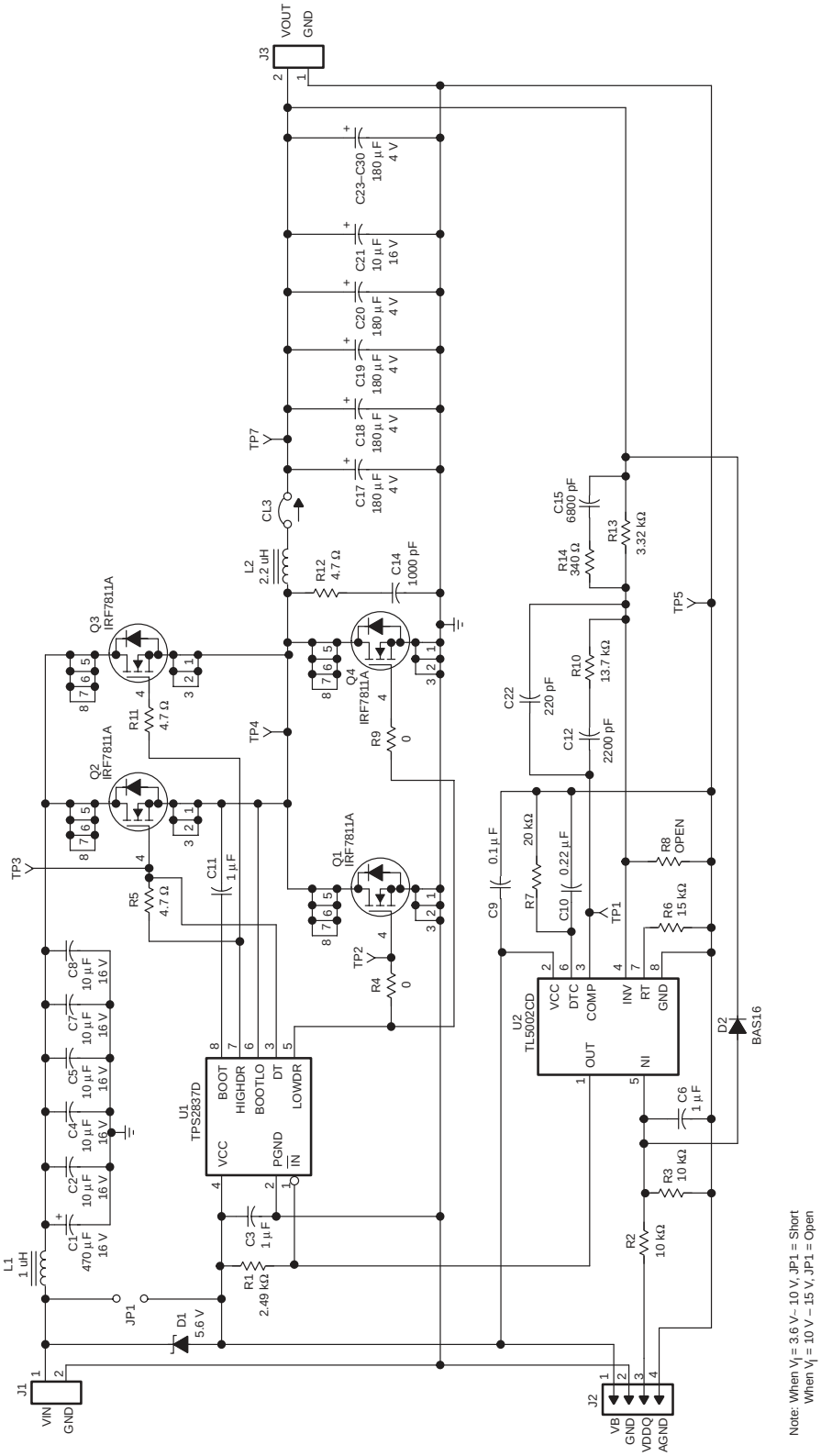
Table 1–1. Operating Specifications

Specification	Min	Typ	Max	Units
Input voltage range	3.6	5	15	V
V_{DDQ} voltage range	1.8	2.5	3	V
Output voltage range	$\frac{V_{DDQ}}{2}$ –40 mV	$\frac{V_{DDQ}}{2}$	$\frac{V_{DDQ}}{2}$ + 40 mV	V
Output current range	-12		12	A
Operating frequency		400		kHz
Output ripple (steady state)			5†	mV
Output ripple (at load transient of 0.4 A/μs)	–35‡		35‡	mV
Efficiency		85%§	86.3%§	

† V_I= 5 V, V_O = 1.25 V, I_O = 12 A
‡ V_I= 5 V, V_O = 1.25 V, I_O = ±12 A
§ V_I= 5 V, V_O = 1.25 V, I_O = 4.6 A

1.3 SLVP180C Schematic

Figure 1–2. Schematic Diagram



1.4 SLVP180C Bill of Materials

Table 1–2 lists materials required for the SLVP180C EVM.

Table 1–2. SLVP180C EVM Bill of Materials

Ref Des	Qty	Part Number	Description	Size	MFG
C1	1	UUD1C47MNR1GS	Capacitor, Aluminum, 470 μF, 16 V, 170 mΩ, 20%	E7	Nichicon
C2, C4, C5, C7, C8, C21	6	EMK325BJ106MN	Capacitor, Ceramic, 10 μF, 16 V, X5R, ±20%	1210	Taiyo Yuden
C3, C6, C11	3	GRM40X7R105K16	Capacitor, Ceramic, 1 μF, 16 V, X7R, 10%	805	Murata
C9	1	GRM39X7R104K16	Capacitor, Ceramic, 0.1 μF, 16 V, X7R, 10%	603	Murata
C10	1	GRM40X7R224K16	Capacitor, Ceramic, 0.22 μF, 16 V, X7R, 10%	805	Murata
C12	1	GRM40X7R222K25	Capacitor, Ceramic, 2200 pF, 16 V, X7R, 10%	805	Murata
C13	1	Open			
C14	1	GRM40X7R102K25	Capacitor, Ceramic, 1000 pF, 25 V, X7R, 10%	805	Murata
C15	1	GRM40X7R682K25	Capacitor, Ceramic, 6800 pF, 25 V, X7R, 10%	805	Murata
C17 – C20, C23, C30	12	EEF–UE0G181R	Capacitor, Aluminum, 180 μF, 4 V, 10% (CD Series)	7343	Panasonic
C22	1	GRM40COG221J50	Capacitor, Ceramic, 220 pF, 16 V, X7R, 10%	805	Murata
CL3	1	N/A	Current loop, 0.060 inch holes		N/A
D1	1	1SMB5919BTS	Diode, zener, 5.6 V, 3 W	SMB	On Semi
D2	1	BAS16	Diode, Switching, 10 mA, 85 V, 350 mW	SOT23	Vishay-Liteon
J1, J3	2	ED1609	Terminal block, 2-pin, 15 A, 5.1 mm		OST
J2	1	PTC36SAAN	Header, 4-pin, 100 mil spacing, (36-pin strip)		Sullins
JP1	1	PTC36SAAN	Header, 2-pin, 100 mil spacing, (36-pin strip)		Sullins
L1	1	UP2B–1R0	Inductor, SMT, 1 μH, 9.3 A, 6.5 mΩ	UP2B	Coiltronics
L2	1	UP4B–2R2	Inductor, SMT, 2.2 μH, 12 A, 4.8 mΩ	UP4B	Coiltronics
Q1–Q4		IRF7811A	MOSFET, N-ch, 30 V, 11 A, 10 mΩ	SO8	IR
R1	1	Std	Resistor, 2.49 kΩ, 1/16-W,1%	603	Std

Table 1–2. SLVP180C EVM Bill of Materials (Continued)

Ref Des	Qty	Part Number	Description	Size	MFG
R2, R3	2	Std	Resistor, 10 kΩ, 1/16-W,5%	603	Std
R4, R9	2	Std	Resistor, 0 Ω, 1/10-W,5%	805	Std
R5, R11, R12	3	Std	Resistor, 4.7 Ω, 1/10-W,5%	805	Std
R6	1	Std	Resistor, 15 kΩ, 1/16-W,1%	603	Std
R7	1	Std	Resistor, 20 kΩ, 1/16-W,5%	603	Std
R8	1	Open			
R10	1	Std	Resistor, 13.7 kΩ, 1/10-W,1%	805	Std
R13	1		Resistor, 3.32 kΩ, 1/10-W,1%	805	Std
R14	1	Std	Resistor, 340 Ω, 1/10-W,1%	805	Std
R16	1	Open			
TP5		240-333	Test point, black, 1 mm		Farnell
TP1 – TP4, TP7		240-345	Test point, red, 1 mm		Farnell
U1		TPS2837D	IC, MOSFET Driver	SO8	Texas Instruments
U2		TL5002CD	IC, Low-Cost PWM Controller With Open-Collector Output	SO8	Texas Instruments
U3		Open			

1.5 EVM Board Layout

Figure 1–3. Top Silk Screen With Top Copper Layer

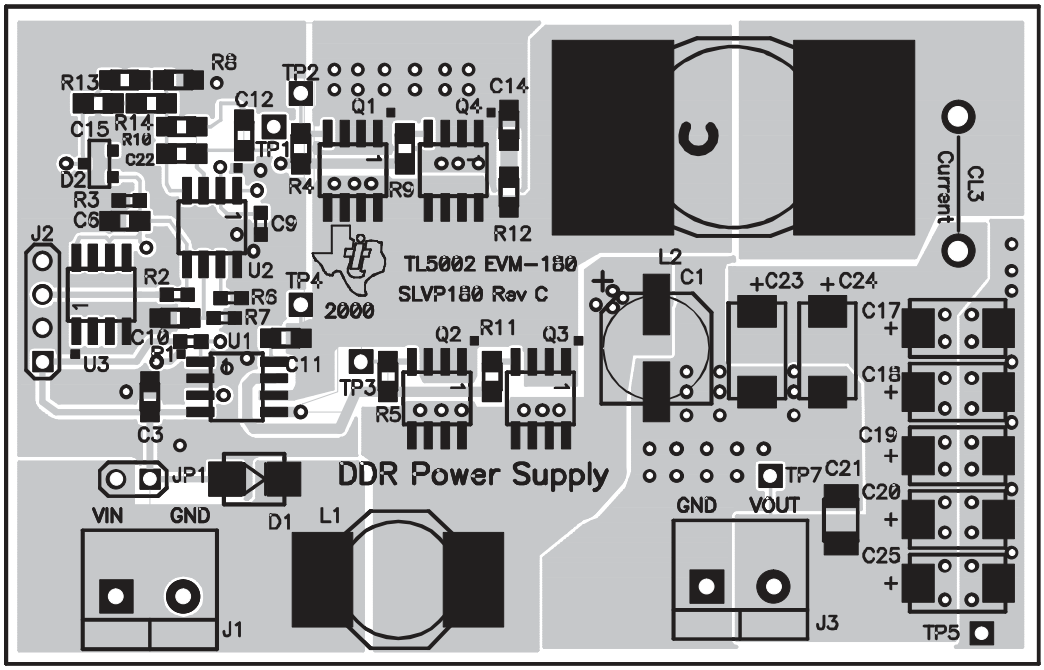


Figure 1–4. Bottom Silk Screen With Bottom Copper Layer

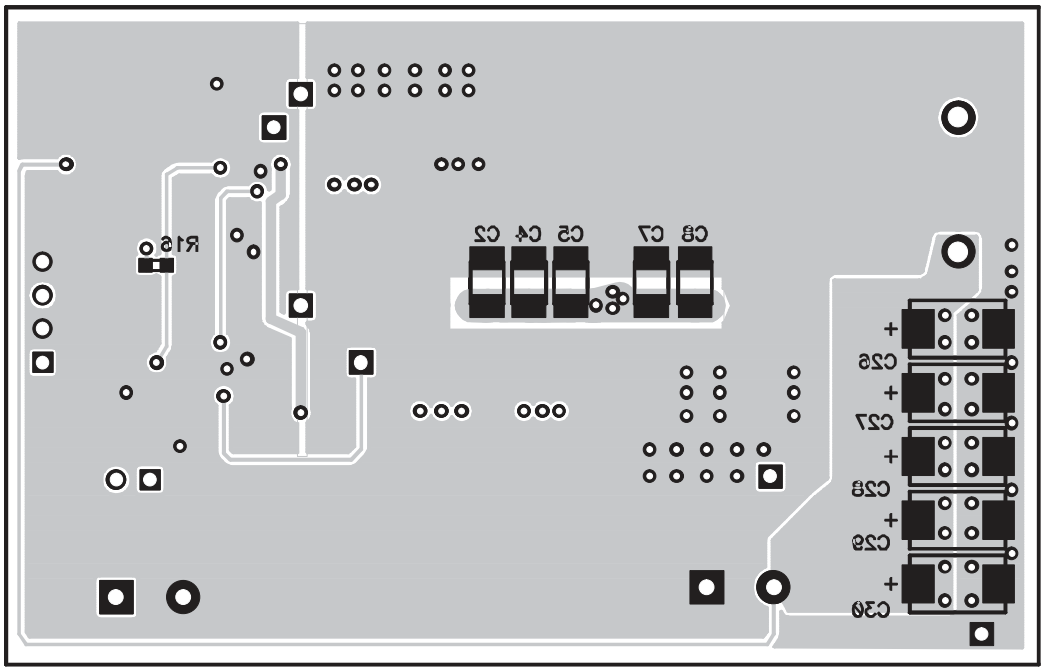


Figure 1–5. Top Layer Copper

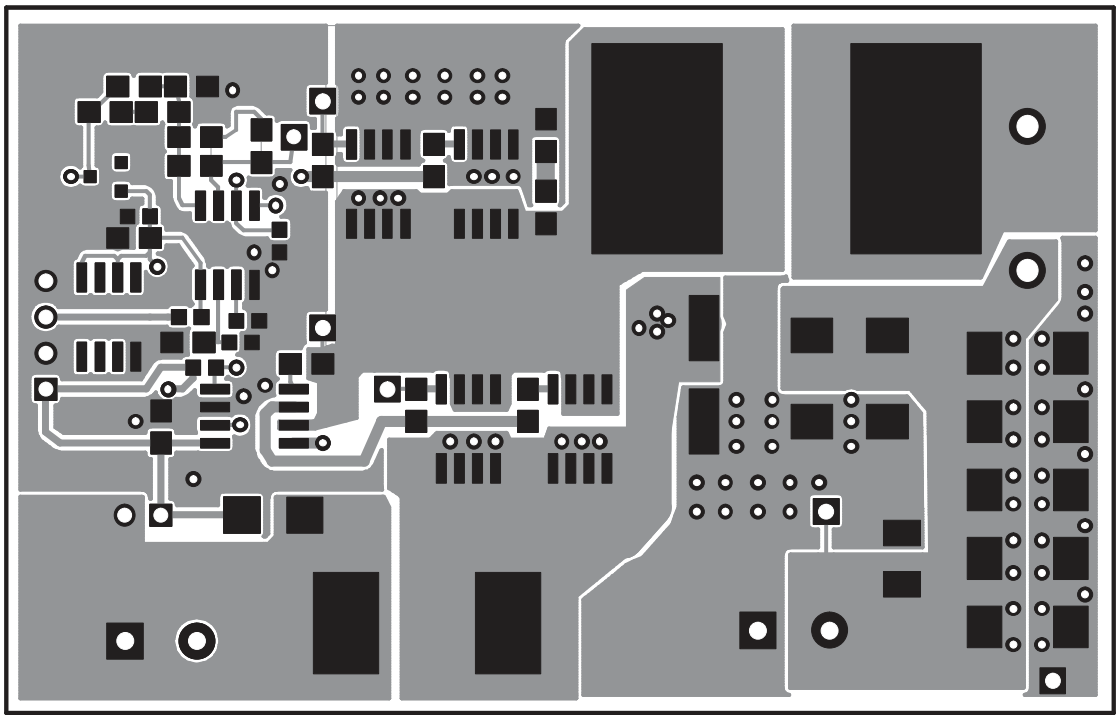


Figure 1–6. Bottom Layer Copper

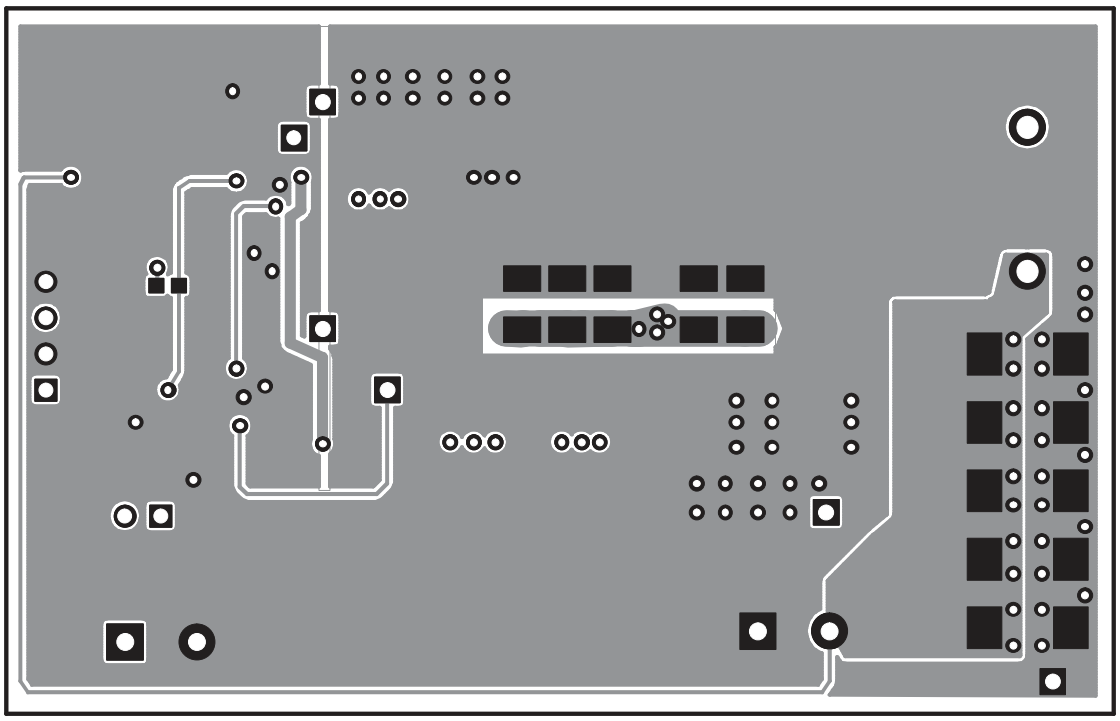


Figure 1–7. Layer 2 (Internal) Copper

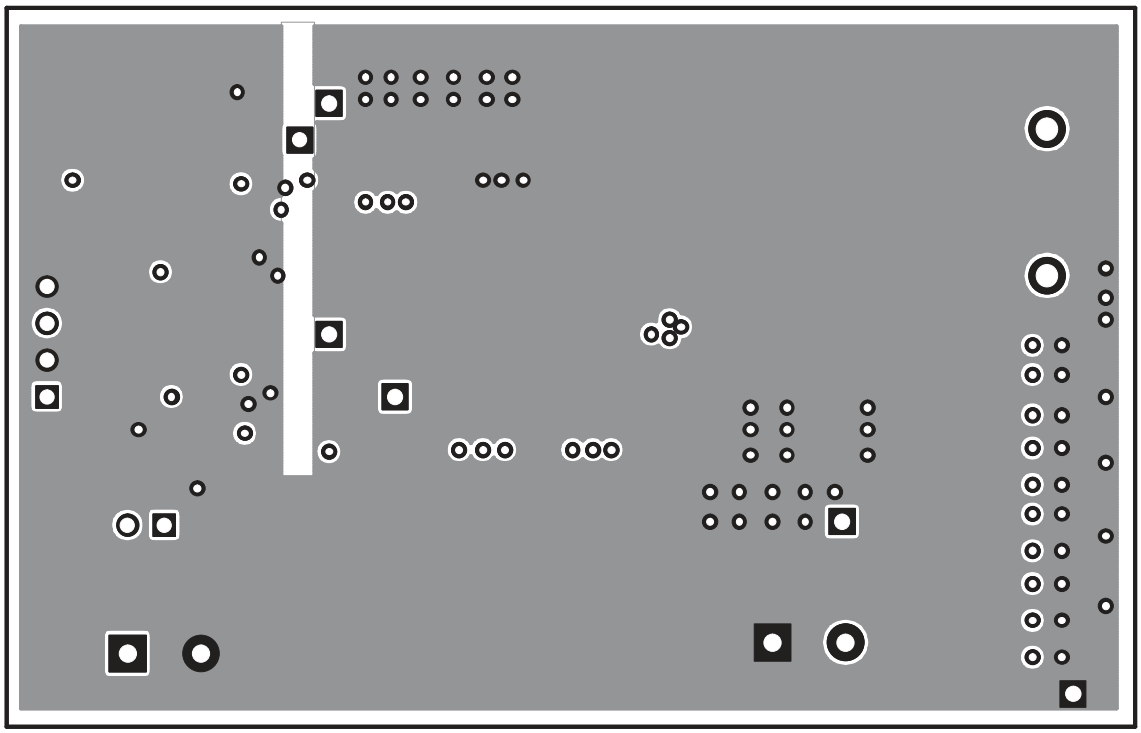
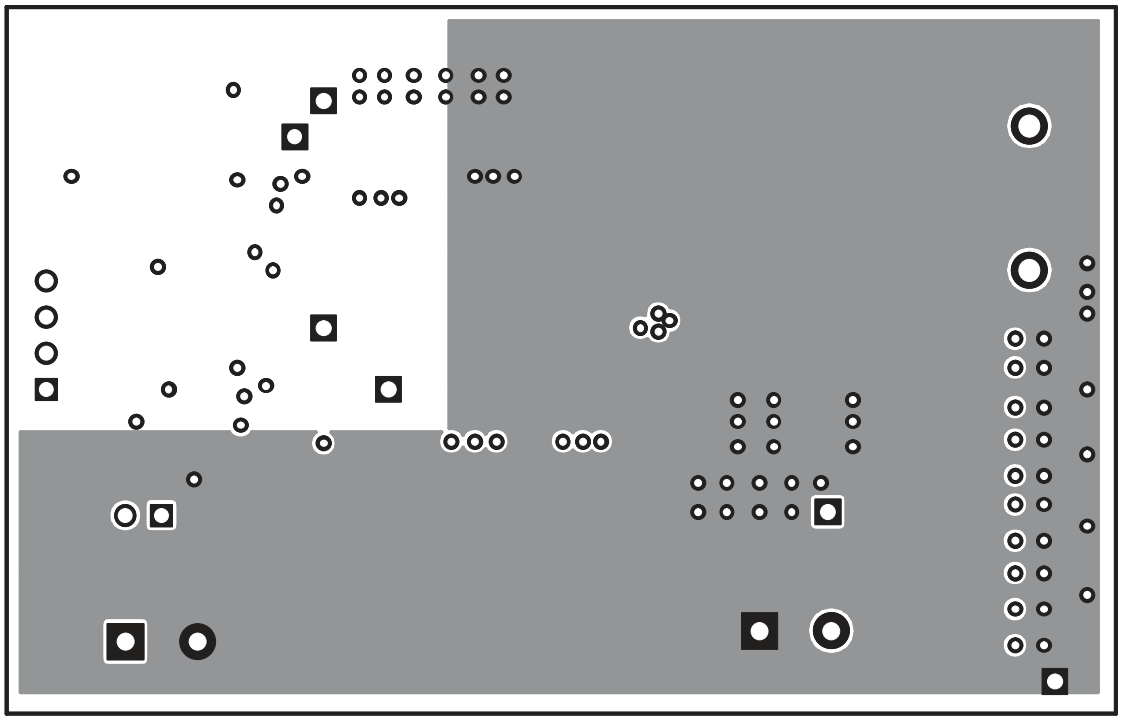


Figure 1–8. Layer 3 (Internal) Copper



Chapter 2

Design Procedures

This chapter shows the procedure used in the design of the SLVP180C.

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2.1 Duty Cycle Estimate

The duty cycle for a continuous mode stepdown converter is approximately:

$$D = \frac{V_O}{V_I} = \frac{1.25}{5} = 0.25 \quad (2–1)$$

2.2 Output Filter

A synchronous buck converter uses a single-stage LC output filter. Choose an inductor to maintain continuous mode operation down to 5% of the rated output load:

$$\Delta I_o = 2 \times 0.05 \times I_o = 0.1 \times 12 = 1.2A \quad (2–2)$$

2.2.1 Inductor Value

$$L = \frac{\left(V_O + I_{O(max)} \times r_{ds(max)}\right) \times (1–D)}{f_{(sw)} \times \Delta I_O} = \frac{(1.25 + 12 \times 0.012)0.75}{400000 \times 1.2} \approx 2.2\ \mu H \quad (2–3)$$

2.2.2 Capacitor Value

Normally, the output capacitor is selected to limit ripple voltage to the level required by the specification. This power supply is designed for a worst-case load step of full sinking load (–12A) to full sourcing load (12A) with a slew rate of 0.4A/μs. Assuming the capacitor is very large, the ESR needed to limit the ripple to 40 mV for steady state is:

$$ESR < \frac{\Delta V_O}{\Delta I_O} = \frac{0.04}{1.2} = 33\ m\Omega \quad (2–4)$$

The desired output capacitance to meet $\Delta V_O < 40$ mV under the load transient (0.4A/μs) is obtained with this approximated equation:

$$\Delta V_O \le \Delta V_{ESR(peak)} + \Delta V_{ESL(peak)} + \Delta V_{C_O} < 40\ mV \quad (2–5)$$

The output voltage drops caused by capacitor ESR, ESL, and capacitance are as follows, respectively:

$$\Delta V_{ESR(peak)} = ESR \times I_O\left[1–\frac{SR(I_L)}{SR(I_O)}\right] = ESR \times 12 \times \left(1–\frac{0.32}{0.4}\right) = 2.4 \times ESR \quad (2–6)$$

$$\Delta V_{ESL(peak)} = ESL \times \left[SR(I_O)–SR(I_L)\right] = 10\ nH \times (0.4–0.32) \times 10^6 = 0.8\ mV \quad (2–7)$$

$$\Delta V_{C_O} = \frac{I_O^2}{2 \times C_O}\left[\frac{1}{SR(I_L)}–\frac{1}{SR(I_O)}\right] = \frac{144}{2 \times C_O}\left(\frac{10^{–6}}{0.32}–\frac{10^{–6}}{0.4}\right) = \frac{0.045\ mV}{C_O} \quad (2–8)$$

where $SR(I_L)$ is the slew rate of converter loop response and $SR(I_O)$ is the slew rate of load transient, assume that ESL=10nH.

Therefore, approximated total output voltage drop responded to load step is obtained as follows:

$$\Delta V_O \leq 2.4\ ESR + 0.8\ mV + \frac{0.045\ mV}{C_O} < 40\ mV \qquad (2\text{–}9)$$

Panasonic EEF–UE0G181R has a 180 μF with 25 mΩ of ESR at 400 kHz. Thus, twelve 180 μF capacitors in parallel are chosen to meet the above equation.

2.3 Controller Functions

The controller functions, oscillator frequency, softstart, dead-time-control, short-circuit protection, and sense-divider-network are discussed in this section.

2.3.1 Oscillator Frequency

The oscillator frequency is set by selecting the resistance value from the graph in Figure 8 of the TL5002 data sheet. For 400 kHz, a value of 15 kΩ, R6, is selected.

2.3.2 Dead Time Control

Dead time control provides a maximum on-time for the power switch in each cycle. Set this time by connecting a resistor between DTC and GND. For this design, a maximum duty cycle of 80% is chosen. Then, R7 is calculated as:

$$R7 = (R6 + 1.25) \times 10^3 \times \left[D\left(V_{O(100\%)} - V_{O(0\%)}\right) + V_{O(0\%)}\right] \qquad (2\text{–}10)$$

$$= (15 + 1.25) \times 10^3 \times [0.8 \times (1.5\text{–}0.4) + 0.4] = 20.8\ k\Omega \Rightarrow 20\ k\Omega$$

2.3.3 Softstart Timing

Softstart is added to reduce power-up transients. This is implemented by adding a capacitor across the dead-time resistor. In this design, a softstart time of 4.4 ms is used.

$$C10 = \frac{T_r}{R7} = \frac{4.4\ ms}{20\ k\Omega} = 0.22\ \mu F \qquad (2\text{–}11)$$

2.3.4 Output Voltage

The external reference voltage (V_{DDQ}) sets the output voltage, V_{OUT} in EVM schematic. The output voltage, V_{OUT} (or V_O), represents the termination voltage, V_{TT} shown in Figure 1–1.

$$V_O\left(\text{or } V_{tt}\right) = \left(1 + \frac{R13}{R8}\right) \times V_{ref} = (1 + 0) \times \left(\frac{R3}{R2 + R3}\right) \times V_{DDQ} \qquad (2\text{–}12)$$

$$= \left(\frac{10\ k\Omega}{10\ k\Omega + 10\ k\Omega}\right) \times 2.5\ V = 1.25\ V$$

$$\text{Where } V_{ref} = \left(\frac{R3}{R2 + R3}\right) \times V_{DDQ}$$

2.4 Loop Compensation

Loop compensation is necessary to stabilize the converter over the full range of load and line conditions. This evaluation converter is designed to maintain greater than 40 degree of phase margin over all input/output conditions. In addition, sufficient bandwidth must be designed into the circuit to ensure that the converter has good transient response. Both of these requirements are achieved by adding compensation components around the error amplifier to modify the overall loop response.

The loop compensation design procedure consists of shaping the error amplifier frequency response with external components to stabilize the dc/dc converter feedback control loop without destroying the control loop ability to respond to line and/or load transients. A detailed treatment of dc/dc converter stability analysis and design is well beyond the scope of this report. The following is a simplified approach to designing networks to stabilize continuous mode buck converters.

Ignoring the error amplifier frequency response, the response of the pulse width modulator and power switch operating in continuous mode can be modeled as a simple gain block. The magnitude of the gain is the change in output voltage for a change in the pulse width modulator input voltage (error amplifier COMP voltage). Typically, increasing the COMP voltage from 0.4 V to 1.5 V increases the duty cycle from 0 to 100% and the output voltage from 0 V to $V_{I(max)}$ at the nominal input voltage. The gain $A_{(PWM)}$ is:

$$A_{(PWM)} = \frac{V_{I(max)}}{\Delta V_{O(COMP)}} = \frac{5.5}{1.5–0.4} = 5 \Rightarrow 14 \text{ dB} \qquad (2–13)$$

Similarly, the gain is 10 dB at low line and 23 dB at high line. Converters with wider input ranges need to check for stability at several line voltages to ensure that gain variation does not cause a stability problem.

The output filter is a LC filter and functions accordingly. The inductor and capacitor produce an underdamped complex-pole pair at the filter resonant frequency and the capacitor ESR (R_{ESR}) puts a zero in the response above the resonant frequency. The double pole is located at:

$$\frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{2.2\ \mu H \times 180\ \mu F \times 12}} = 2.3 \text{ kHz} \qquad (2–14)$$

The zero is located at:

$$\frac{1}{2\pi R_{ESR} C} = \frac{1}{2\pi \times 0.003 \times 180\ \mu F \times 12} = 24.6 \text{ kHz} \qquad (2–15)$$

Figure 2–1 and Figure 2–2 show power stage gain and phase plots.

Figure 2–1. Power Stage Gain

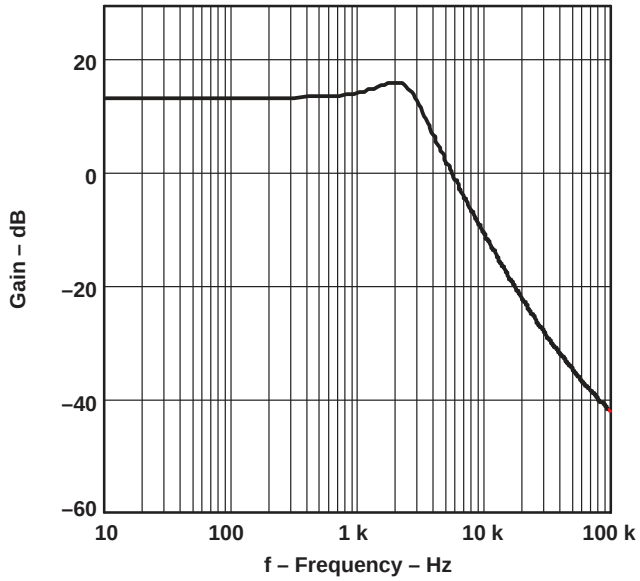
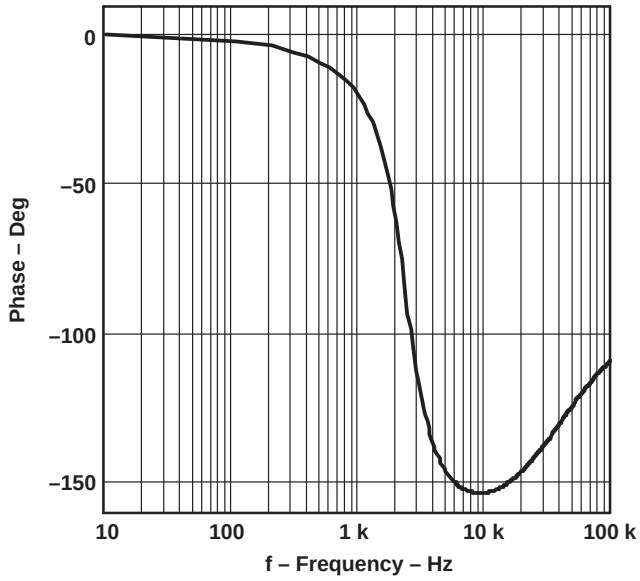
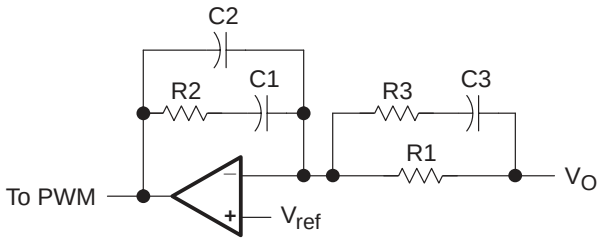


Figure 2–2. Power Stage Phase



Unless the designer is trying to meet an unusual requirement, such as very wide band response, many of the decisions regarding gains, compensation pole and zero locations, and unity-gain bandwidth are largely arbitrary. Generally, the gain at low frequencies is very high to minimize error in the output voltage; compensation zeros are added near the filter poles to correct for the sharp change in phase encountered near the filter resonant frequency; and an open loop unity gain frequency is selected well beyond the filter resonant frequency but 10% or less than the converter operating frequency. In this instance, a unity gain frequency of approximately 20 kHz is chosen to provide good transient response. Figure 2–3 shows a standard compensation network chosen for this example.

Figure 2–3. Compensation Circuit



The total phase lag through the compensated error amplifier is calculated with this equation:

$$\theta_{ea} = 270° - 2\ \tan^{-1}K + 2\ \tan^{-1}\left(\frac{1}{K}\right) \qquad (2\text{–}16)$$

Where : $K = \dfrac{f_{(bw)}}{f_{(z)}} = \dfrac{f_{(p)}}{f_{(bw)}}$

$f_{(bw)}$ = desired cross over frequency
$f_{(p)}$ = error amplifier pole frequency
$f_{(z)}$ = error amplifier zero frequency

Assuming an ideal amplifier, the transfer function is:

$$A_{(ea)}(s) = \left[\frac{1}{sR1\ (C1 + C2)}\right] \times \frac{[s(R1 + R3)C3 + 1](sR2C1 + 1)}{(sR3C3 + 1)\left[sR2(C2//C1) + 1\right]} \qquad (2\text{–}17)$$

The location of the double-zero and double-pole frequencies is fixed by the K factor, which yields the desired phase margin. From the transfer function (equation 2–17) and equation 2–16, the R and C values that set the zero and pole frequencies at the desired points are determined.

To obtain the desired phase margin (45 degree) at cross over frequency (BW=20 kHz), the total phase lag (total phase lag = power stage phase + error amp phase) should be equal to the desired phase lag. As shown in Figure 2–2 (power stage phase), the power stage phase lag at 20 kHz is recorded as about 150°. Thus, K factor is obtained using equation 2–11 (K = 3.15).

Then, two zeros and poles are calculated as:

$$f_{(z1)} = f_{(z2)} = \frac{f_{(bw)}}{K} = \frac{20000}{3.15} = 6.3\ \text{kHz} \qquad (2\text{–}18)$$

$$f_{(p1)} = f_{(p2)} = K \times f_{(bw)} = 63\ \text{kHz} \qquad (2\text{–}19)$$

Now, the components around the error amplifier can be calculated using the following equations:

A first zero of

$$f_{(z1)} = \frac{1}{2\pi R2C1} \quad (2\text{–}20)$$

A second zero of

$$f_{(z2)} = \frac{1}{2\pi(R1 + R3)C3} \quad (2\text{–}21)$$

A first pole of

$$f_{(p1)} = \frac{1}{2\pi R3C3} \quad (2\text{–}22)$$

A second pole of

$$f_{(p2)} = \frac{C1 + C2}{2\pi R2(C1C2)} \quad (2\text{–}23)$$

If higher value of R1 is chosen, the compensation capacitor values becomes smaller so that the component values may be less than a parasitic value. Thus, R1 is chosen to calculate the component values as follows:

$$R1 = 3.32\ k\Omega \quad (2\text{–}24)$$

Then calculate using equations (2–20) to (2–23):

$$C3 = \frac{\frac{1}{f(z2)} - \frac{1}{f(p1)}}{2\pi R1} = 6800\ pF \Rightarrow \text{Use } 7200\ pF \quad (2\text{–}25)$$

$$R3 = \frac{1}{2\pi C3\ f_{(p1)}} = 372\ \Omega \Rightarrow \text{Use } 330\ \Omega \quad (2\text{–}26)$$

The first zero (at 6.3 kHz) occurs when R2 = X_{C1} and the error amplifier gain at that frequency is approximately R2 ÷ R1. Thus, from Figure 2-1, power stage gain, the error amplifier gain at 6.3 kHz should be 12 dB. The gain of 12 dB translates to a voltage of 4 V. Therefore, R2 is obtained as follows:

$$R2 = 4 \times R1 = 13.3\ k\Omega \Rightarrow \text{Use } 13.7\ k\Omega \quad (2\text{–}27)$$

$$C2 = \frac{1}{2\pi R2\ f_{(p2)}} = 190\ pF \Rightarrow \text{Use } 220\ pF \quad (2\text{–}28)$$

$$C1 = \frac{1}{2\pi R2\ f_{(z1)}} = 1890\ pF \Rightarrow \text{Use } 2200\ pF \quad (2\text{–}29)$$

Figure 2–4 and Figure 2–5 show the bode plot for the compensation network. Figure 2–6 and Figure 2–7 show the overall loop response.

Figure 2–4. Compensation Gain

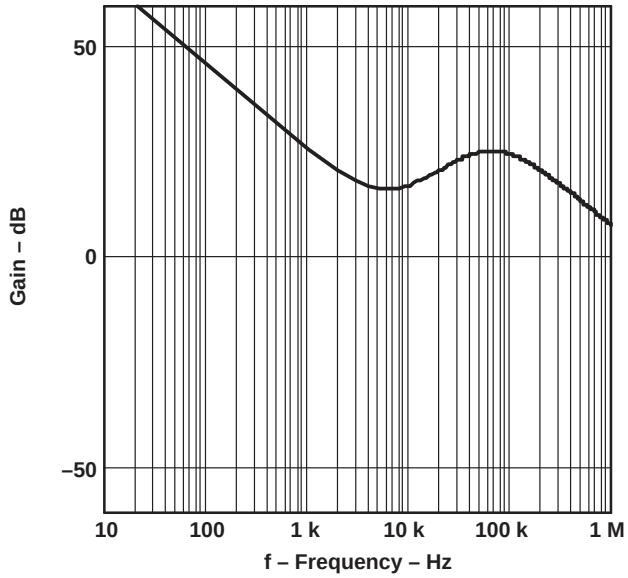


Figure 2–5. Compensation Phase

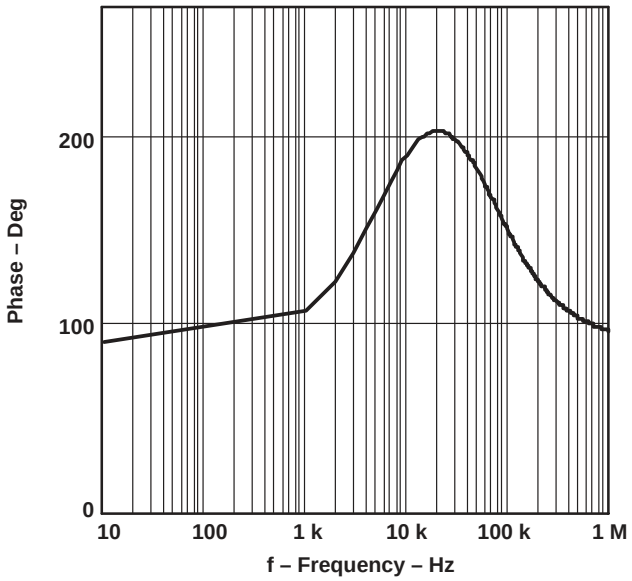


Figure 2–6. Overall Loop Gain Response

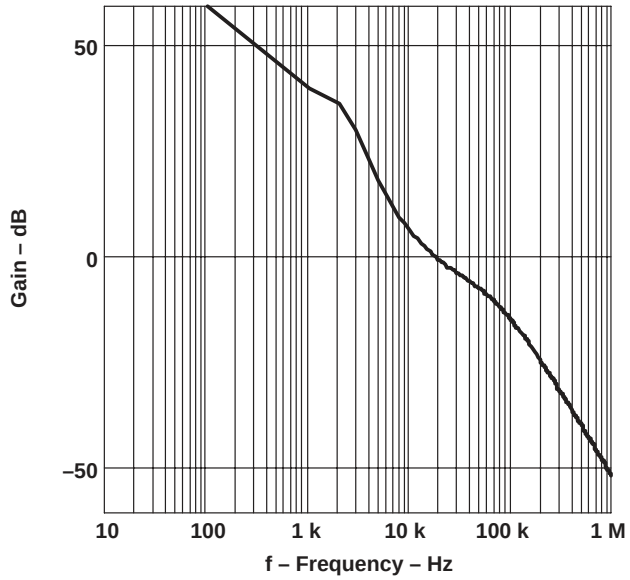
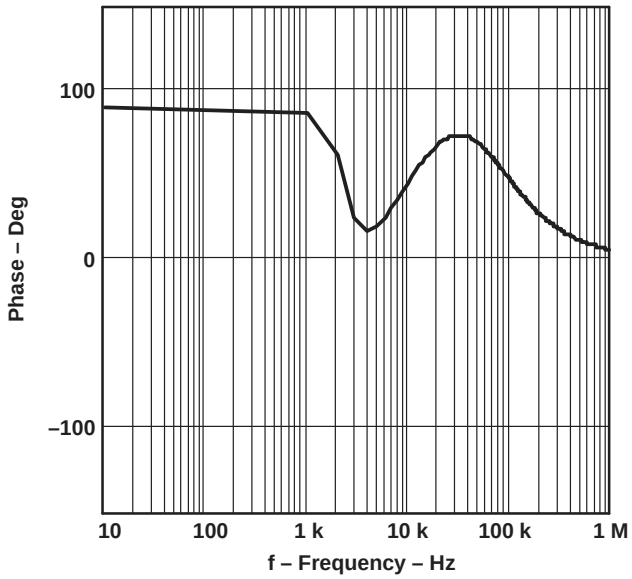


Figure 2–7. Overall Loop Phase Response



Note from the overall response shown in Figure 2–6 and Figure 2–7 that the minimum phase margin is 45 degrees and the bandwidth is 20 kHz under nominal operating conditions.

Chapter 3

Test Results

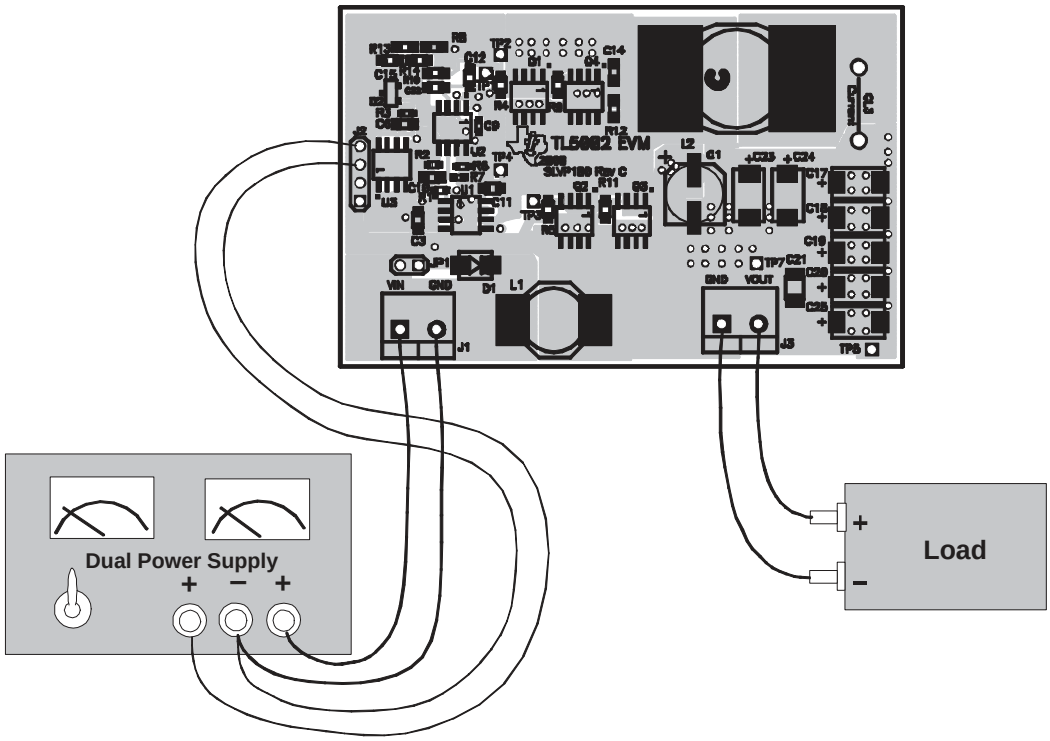
A dual power supply that has a power capability of 15 V/13 A is required for this test. However, two individual power supplies that have a 15 V/13 A and a 6 V/5 A respectively can be used.

Topic **Page**

3.1 Test Setup

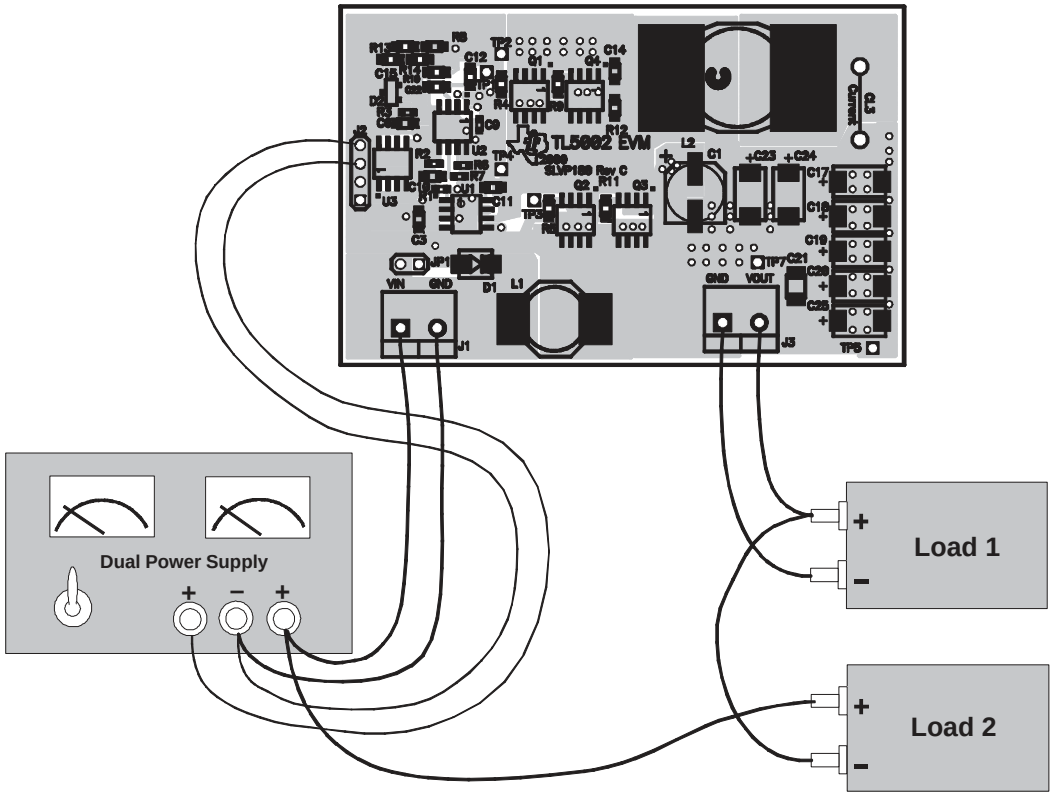
Figure 3–1 and 3–2 show the input/output connections to the SLVP180C.

Figure 3–1. Test Setup for Sourcing Mode



Note: All wire pairs should be twisted.

Figure 3–2. Test Setup for Sinking Mode



Test Set-UP (Sinking Mode)

Note: All wire pairs should be twisted.

Notes: 1) The electronic load 2 must be capable of floating above ground since the negative output sits at 1.25 V and not 0 V dc.

2) The loads must be electronic loads.

3.2 Test Results

Figures 3–3 through figure 3–8 show the test results for the SLVP180C.

Figure 3–3. Efficiency Graph

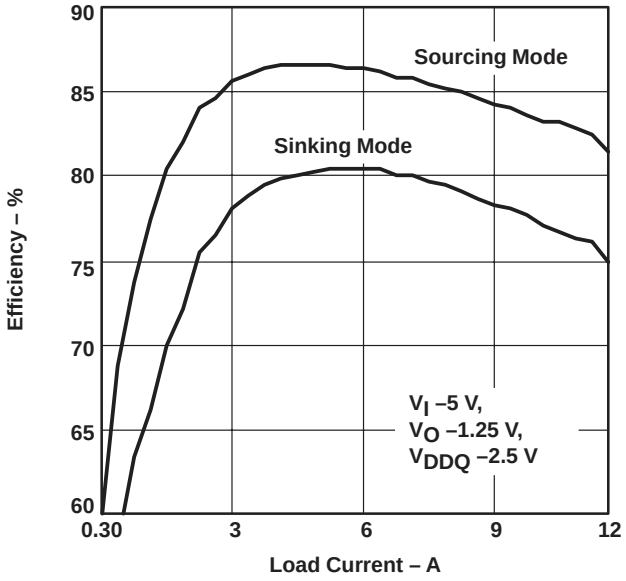


Figure 3–4. Output Voltage (Upper Trace) and Output Current

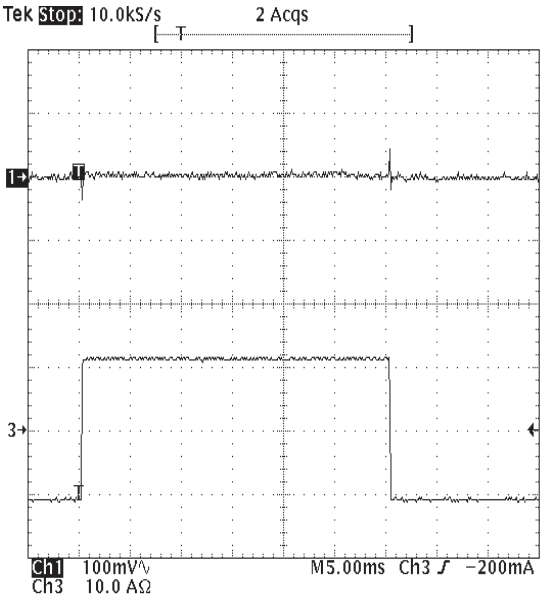


Figure 3–5. Output Voltage (Upper Trace) and Phase Voltage (Sourcing Mode)

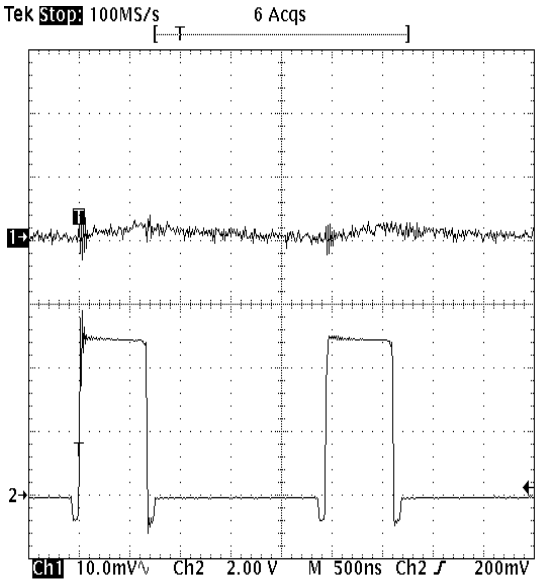


Figure 3–6. Output Voltage (Upper Trace) and Phase Voltage (Sinking Mode)

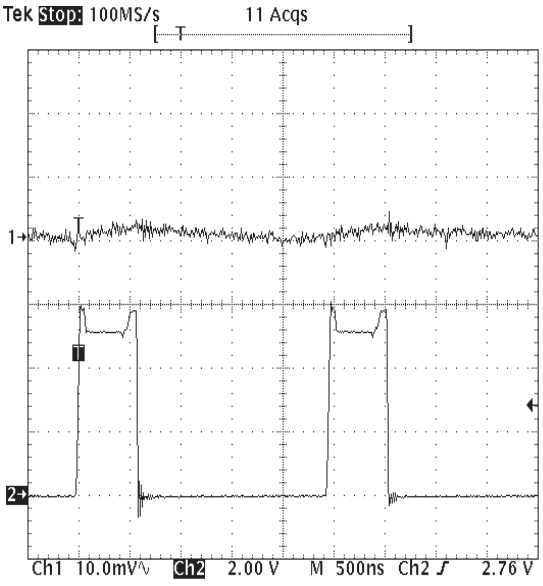


Figure 3–7. Output Inductor Current (Upper Trace) and Phase Voltage (Sourcing Mode)

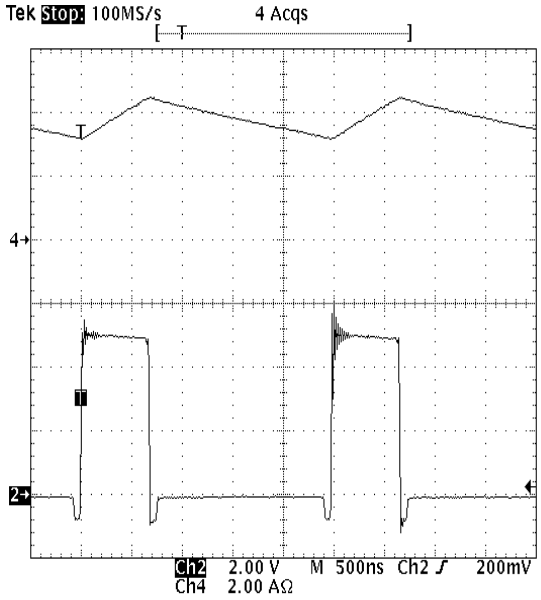


Figure 3–8. Output Inductor Current (Upper Trace) and Phase Voltage (Sinking Mode)