ANALOG DEVICES

17 GHz to 24 GHz, GaAs, MMIC, I/Q Upconverter

Data Sheet

ADMV1011

FEATURES

- **RF output frequency range: 17 GHz to 24 GHz**
- **IF input frequency range: 2 GHz to 4 GHz**
- **LO input frequency range: 8 GHz to 12 GHz with 2× multiplier**
- **Sideband rejection: 32 dB for lower sideband**
- **P1dB: 25 dBm**
- **Gain regulation: 30 dB**
- **Output IP3: 33 dBm**
- **Matched 50 Ω RF output, LO input, and IF input**
- **32-terminal, 4.9 mm × 4.9 mm LCC package**

APPLICATIONS

- **Point to point microwave radios**
- **Radars and electronic warfare systems**
- **Instrumentation, automatic test equipment**

FUNCTIONAL BLOCK DIAGRAM

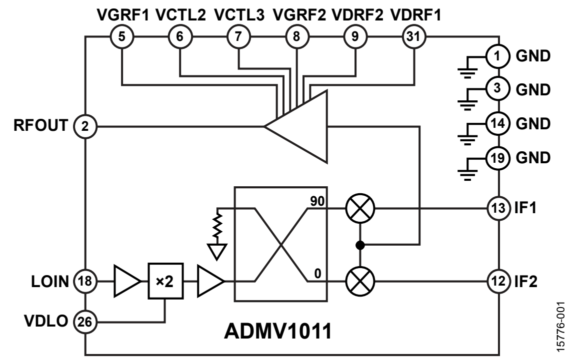

Figure 1.

GENERAL DESCRIPTION

The ADMV1011 is a compact, gallium arsenide (GaAs) design, monolithic microwave integrated circuit (MMIC), double sideband (DSB) upconverter in a RoHS compliant package optimized for point to point microwave radio designs that operates in the 17 GHz to 24 GHz frequency range.

The ADMV1011 provides 21 dB of conversion gain with 32 dBc of sideband rejection for the lower sideband and 23 dBc of sideband rejection for the upper sideband. The ADMV1011 uses a radio frequency (RF) amplifier preceded by an in phase/quadrature (I/Q) double balanced mixer, where a driver amplifier drives the local oscillator (LO) with a 2× multiplier.

IF1 and IF2 mixer inputs are provided and an external 90° hybrid is needed to select the required sideband. The I/Q mixer topology reduces the need for filtering the unwanted sideband. The ADMV1011 is a much smaller alternative to hybrid style DSB upconverter assemblies and it eliminates the need for wire bonding by allowing the use of surface-mount manufacturing assemblies.

The ADMV1011 upconverter comes in a compact, thermally enhanced, 4.9 mm × 4.9 mm LCC package. The ADMV1011 operates over the −40°C to +85°C temperature range.

Rev. A **Document Feedback**

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Technical Support **www.analog.com**

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10/2017—Revision 0: Initial Version

SPECIFICATIONS

Data specified at VDRF1 and VDRF2 = 5 V, VDLO = 3.5 V, IDRF1 = 220 mA, IDRF2 = 75 mA, −4 dBm ≤ LO ≤ +4 dBm, −40°C ≤ T_A ≤ +85°C, taken with Mini-Circuits QCN-45+ power splitter/combiner, unless otherwise noted. VCTL2, VCTL3 = −5 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RF OUTPUT FREQUENCY			17		24	GHz
INPUT FREQUENCY						
Local Oscillator	LO	With 2× multiplier	8		12	GHz
Intermediate Frequency	IF		2		4	GHz
LO AMPLITUDE			−4	0	+4	dBm
POWER INTERFACE						
Amplifier Bias Voltage						
LO	VDLO			3.5		V
RF	VDRF1, VDRF2			5		V
Amplifier Bias Current						
LO	IDLO			160	180	mA
RF	IDRF1	Adjust VGRF1 between −1.8 V to −0.8 V to get IDRF1		220	300	mA
	IDRF2	Adjust VGRF2 between −1.8 V to −0.8 V to get IDRF1		75		mA
Amplifier Gate Current						
RF	IGRF1			<1		mA
	IGRF2			<1		mA
RF Amplifier Gate Control Voltage	VGRF1, VGRF2		−1.8		−0.8	V
RF Amplifier Gain Control Voltage	VCTL2, VCTL3	Maximum gain = −5 V, minimum gain = 0 V	−5		0	V
Total Power Dissipation				2.1		W

LOWER SIDEBAND PERFORMANCE

Data specified at VDRF1 and VDRF2 = 5 V, VDLO = 3.5 V, IDRF1 = 220 mA, IDRF2 = 75 mA, −4 dBm ≤ LO ≤ +4 dBm, −40°C ≤ T_A ≤ +85°C, taken with Mini-Circuits QCN-45+ power splitter/combiner, unless otherwise noted. VCTL2, VCTL3 = −5 V, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RF PERFORMANCE						
Frequency						
Radio Frequency	RF		17		20	GHz
Local Oscillator	LO		8.5		12	GHz
Intermediate Frequency	IF		2		4	GHz
Conversion Gain			15	21	26.5	dB
Dynamic Range	VVA	VVA control slope > 35 mV/dB	30	32		dB
Single Sideband Noise Figure	SSB NF	With hybrid at maximum gain		14	16	dB
		With hybrid vs. gain regulation, gain control ≤ 25 dB		14	22	dB
Output Third-Order Intercept	IP3	At output power (P_{OUT}) = 8 dBm at maximum gain	31	33		dBm
Output Third-Order Intercept vs. Gain Regulation						
5 dB Attenuation			25.5	30		dBm
10 dB Attenuation			20	22		dBm
15 dB Attenuation			14.5	18		dBm
20 dB Attenuation			9	25		dBm
25 dB Attenuation			3.5	16		dBm
30 dB Attenuation			−2	+12		dBm
Output 1 dB Compression Point	P1dB		22.5	25		dBm
Sideband Rejection		Gain regulation change from 0 dB to 31 dB	20	32		dBc

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Leakage						
2× LO to RF		Maximum conversion gain at 18 GHz		−5	+5	dBm
		Vs. gain regulation			1	dB/dB
2× LO to IF				−40	−25	dBm
Return Loss						
RF Output				15	10	dB
LO Input		LO = 0 dBm		11	10	dB
IF Input				20	10	dB
IF Input Power			−25		0	dBm
3× LO − 4 × IF Spur		RF frequency (f_{RF}) = 18 GHz, IF = 0 dBm	64	80		dBc
1× LO + 2 × IF Spur		f_{RF} = 18 GHz, IF = 0 dBm	55	75		dBc
6× IF Spur		f_{RF} = 18 GHz, IF = 0 dBm	72	85		dBc

UPPER SIDEBAND PERFORMANCE

Data specified at VDRF1 and VDRF2 = 5 V, VDLO = 3.5 V, IDRF1 = 220 mA, IDRF2 = 75 mA, −4 dBm ≤ LO ≤ +4 dBm, −40°C ≤ T_A ≤ +85°C, taken with Mini-Circuits QCN-45+ power splitter/combiner, unless otherwise noted. VCTL2, VCTL3 = −5 V, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RF PERFORMANCE						
Frequency						
Radio Frequency	RF		20		24	GHz
Local Oscillator	LO		8		11	GHz
Intermediate Frequency	IF		2		4	GHz
Conversion Gain			15	21	26.5	dB
Dynamic Range	VVA	VVA control slope > 35 mV/dB	30	37		dB
Single Sideband Noise Figure	SSB NF	With hybrid at maximum gain		13.5	16	dB
		With hybrid vs. gain regulation, gain control ≤ 25 dB		13.5	22	dB
Output Third-Order Intercept	IP3	At output power (P_{OUT}) = 8 dBm	31	33		dBm
Output Third-Order Intercept vs. Gain Regulation						
5 dB Attenuation			25.5	27		dBm
10 dB Attenuation			20	25		dBm
15 dB Attenuation			14.5	17		dBm
20 dB Attenuation			9	12		dBm
25 dB Attenuation			3.5	8		dBm
30 dB Attenuation			−2	+7		dBm
Output 1 dB Compression Point	P1dB		22.5	25		dBm
Sideband Rejection		Gain regulation change from 0 dB to 31dB	20	23		dBc
Leakage						
2× LO to RF		Maximum conversion gain at 23 GHz		−5	+5	dBm
		Vs. gain regulation			1	dB/dB
2× LO to IF				−40	−25	dBm
Return Loss						
RF Output				15	10	dB
LO Input		LO = 0 dBm		11	10	dB
IF Input				20	10	dB
IF Input Power			−25		0	dBm
4× LO − 5 × IF Spur		RF frequency (f_{RF}) = 23 GHz, IF = 0 dBm	63	80		dBc
4× LO − 4 × IF Spur		f_{RF} = 23 GHz, IF = 0 dBm	61	75		dBc
3× LO − 2 × IF Spur		f_{RF} = 23 GHz, IF = 0 dBm	60	80		dBc
1× LO + 4 × IF Spur		f_{RF} = 23 GHz, IF = 0 dBm	65	80		dBc
7× IF Spur		f_{RF} = 23 GHz, IF = 0 dBm	75	110		dBc

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	
VDLO	5.5 V
VDRF1 – VGRF1, VDRF2 – VGRF2[1]	8 V
VGRF1, VGRF2	0 V
VCTRL2, VCTRL3	−6 V to +0.5 V
IF1/IF2 Source and Sink Current	2 mA
Maximum Junction Temperature (T_J)	175°C
Maximum Power Dissipation	2.64 W
Lifetime Maximum Junction Temperature (T_J)	>1 million hours
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Input Power	
LO	15 dBm
IF	15 dBm
Lead Temperature (Soldering 60 sec)	260°C
Moisture Sensitivity Level (MSL)[3]	MSL3
Electrostatic Discharge (ESD) Sensitivity	
Field Induced Charge Device Model (FICDM)	500 V
Human Body Model (HBM)	250 V

[1] The maximum VDRF voltage and the minimum VGRF voltage is determined by this difference. If a maximum VDRF voltage of +5.5 V is required, then the minimum VGRF voltage is −2.5 V.
[2] To calculate power dissipation, which is a theoretical number, use the following equation: $(T_J - 85°C)/\theta_{JC}$.
[3] Based on IPC/JEDEC J-STD-20 MSL classifications.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is thermal resistance, junction to ambient (°C/W), and θ_{JC} is thermal resistance, junction to case (°C/W).

Table 5.

Package Type	θ_{JA}[1]	θ_{JC}	Unit
E-32-1	33.4	34	°C/W

[1] See JEDEC standard JESD51-2 for additional information on optimizing the thermal impedance (printed circuit board (PCB) with 3 × 3 vias).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

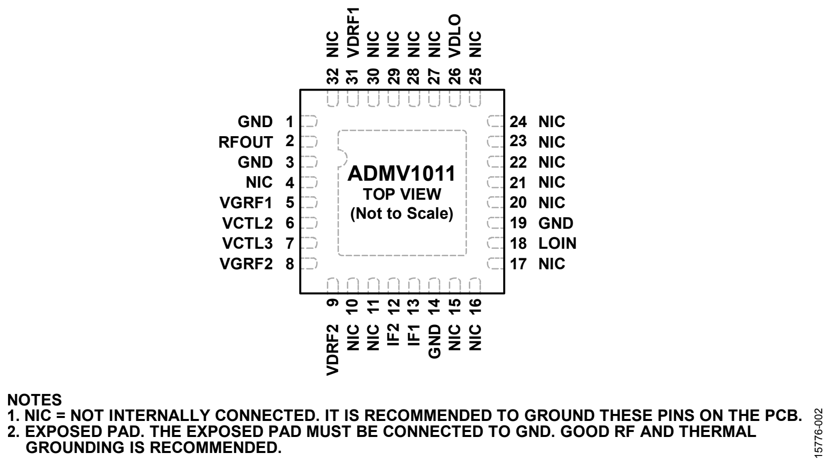


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 14, 19	GND	Ground. These pins are grounded internally and must be grounded on the PCB.
2	RFOUT	RF Output. This pin is ac-coupled internally and matched to 50 Ω single ended.
4, 10, 11, 15 to 17, 20 to 25, 27 to 30, 32	NIC	Not Internally Connected. It is recommended to ground these pins on the PCB.
5, 8	VGRF1, VGRF2	Power Supply Voltage for the Gate of the RF Amplifier. Refer to the Applications Information section for the required external components and biasing.
6, 7	VCTL2, VCLT3	Gain Control Voltage. Refer to the Applications Information section for biasing.
9, 31	VDRF2, VDRF1	Power Supply Voltage for the RF Amplifier. Refer to the Applications Information section for the required external components and biasing.
12, 13	IF2, IF1	Quadrature IF Inputs. These pins are matched to 50 Ω single ended and are dc-coupled. No external dc blocks required. To prevent device malfunction or failure, these pins must not source or sink more than 2 mA of current.
18	LOIN	Local Oscillator. This pin is ac-coupled and matched to 50 Ω single ended.
26	VDLO	Power Supply Voltage for the LO Amplifier. Refer to the external Applications Information section for the required external components and biasing.
	EPAD	Exposed Pad. The exposed pad must be connected to GND. Good RF and thermal grounding is recommended on the PCB.

TYPICAL PERFORMANCE CHARACTERISTICS

LOWER SIDEBAND

Data specified at VDRF1 and VDRF2 = 5 V, VDLO = 3.5 V, IDRF1 = 220 mA, IDRF2 = 75 mA, T_A = 25°C, LO = 0 dBm, IF frequency = 3 GHz, IFx pin= −10 dBm, and taken with Mini-Circuits QCN-45+ power splitter/combiner as lower sideband, unless otherwise noted. VCTL2 and VCTL3 = −5 V, unless otherwise noted.

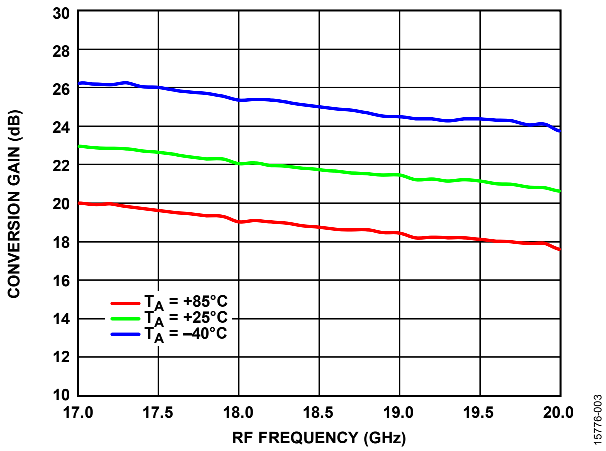


Figure 3. Conversion Gain vs. RF Frequency at Various Temperatures

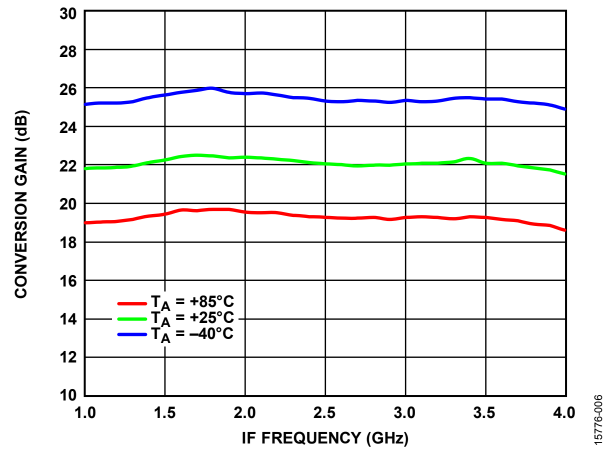


Figure 6. Conversion Gain vs. IF Frequency at Various Temperatures, RF Frequency = 18 GHz

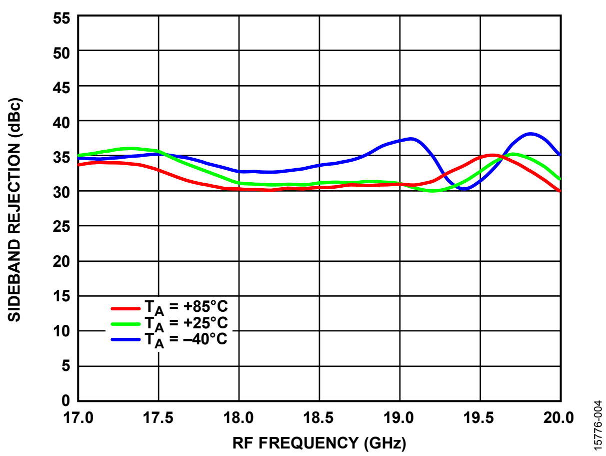


Figure 4. Sideband Rejection vs. RF Frequency at Various Temperatures

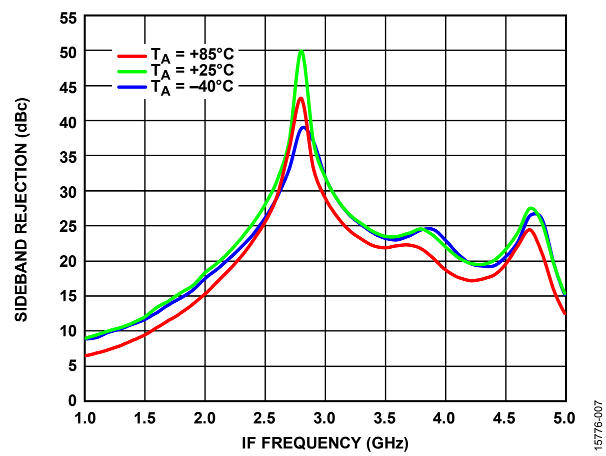


Figure 7. Sideband Rejection vs. IF Frequency, RF Frequency = 18 GHz

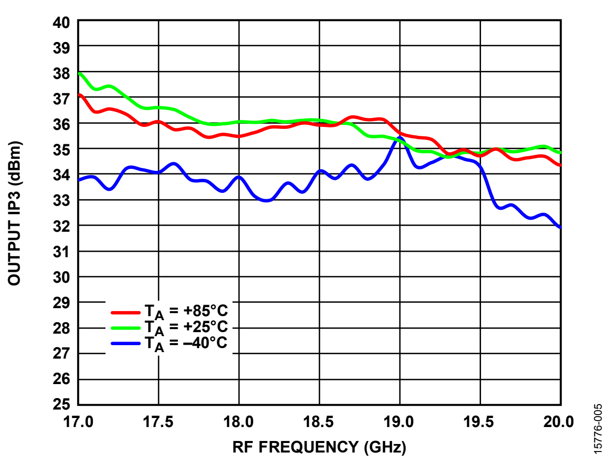


Figure 5. Output IP3 vs. RF Frequency at Various Temperatures, P_{OUT} = 12 dBm

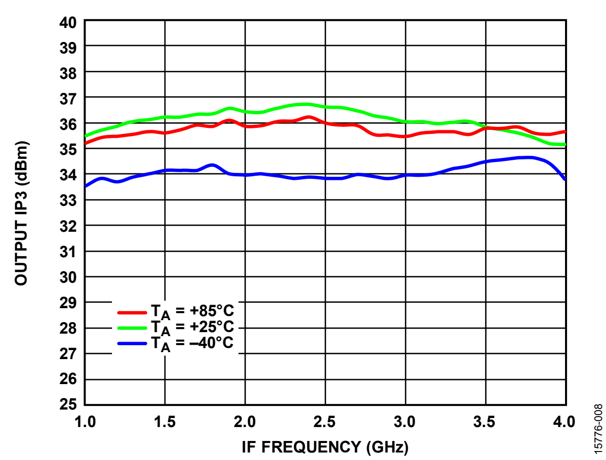


Figure 8. Output IP3 vs. IF Frequency at Various Temperatures, RF Frequency = 18 GHz

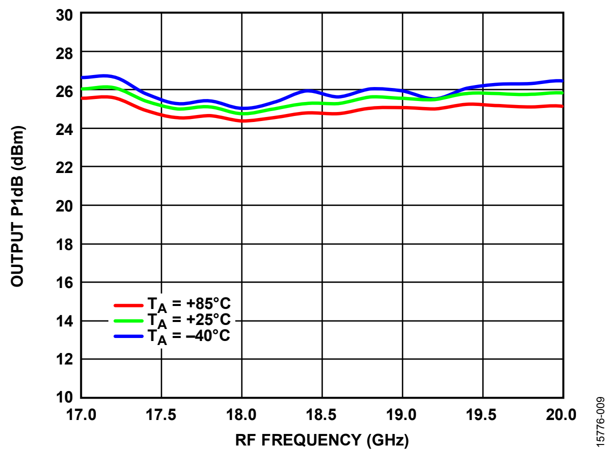


Figure 9. Output P1dB vs. RF Frequency at Various Temperatures

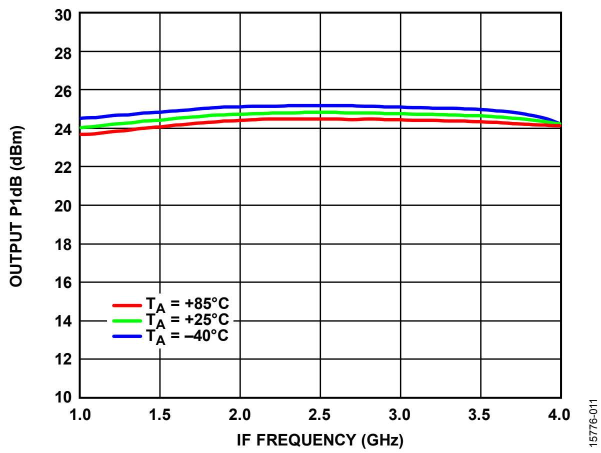


Figure 11. Output P1dB vs. IF Frequency at Various Temperatures, RF Frequency = 18 GHz

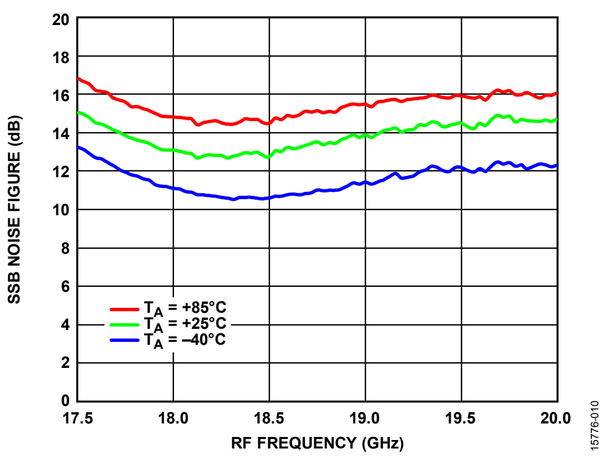


Figure 10. SSB Noise Figure vs. RF Frequency at Various Temperatures

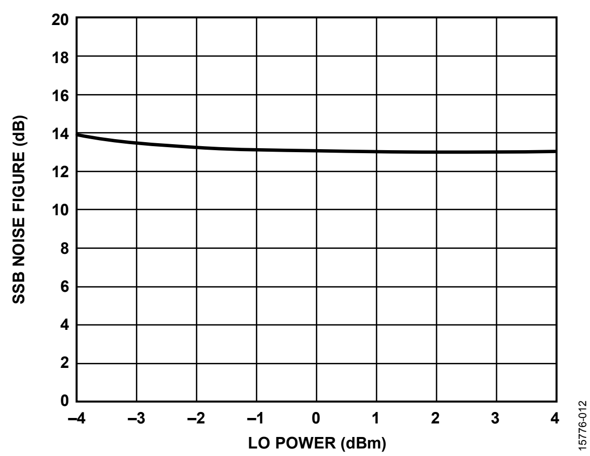


Figure 12. SSB Noise Figure vs. LO Power, RF Frequency = 18 GHz

UPPER SIDEBAND

Data specified at VDRF1 and VDRF2 = 5 V, VDLO = 3.5 V, IDRF1 = 220 mA, IDRF2 = 75 mA, TA = 25°C, LO = 0 dBm, IF frequency = 3 GHz, IFx pin = −10 dBm, and taken with Mini-Circuits QCN-45+ power splitter/combiner as upper sideband, unless otherwise noted. VCTL2 and VCTL3 = −5 V, unless otherwise noted.

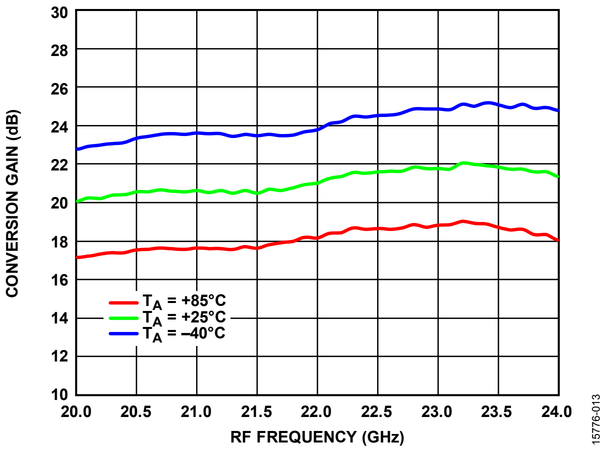


Figure 13. Conversion Gain vs. RF Frequency at Various Temperatures

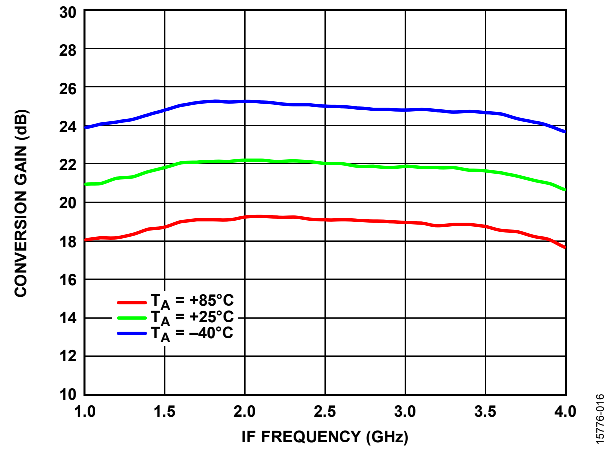


Figure 16. Conversion Gain vs. IF Frequency at Various Temperatures, RF Frequency = 23 GHz

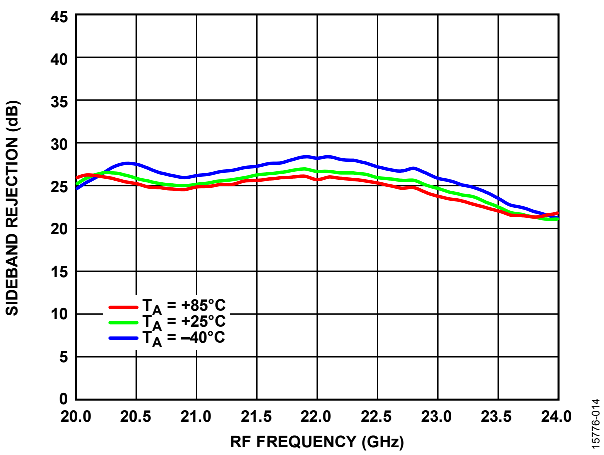


Figure 14. Sideband Rejection vs. RF Frequency at Various Temperatures

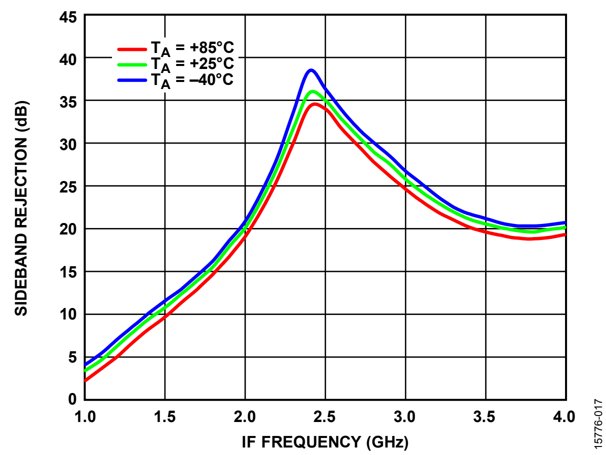


Figure 17. Sideband Rejection vs. IF Frequency at Various Temperatures, RF Frequency = 23 GHz

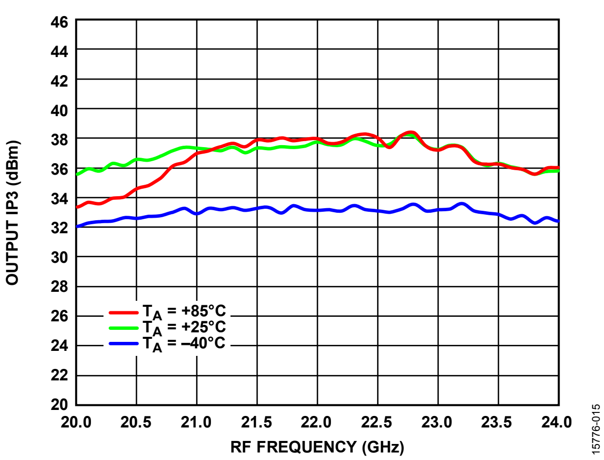


Figure 15. Output IP3 vs. RF Frequency at Various Temperatures, IF Frequencies at P_{OUT} = 12 dBm

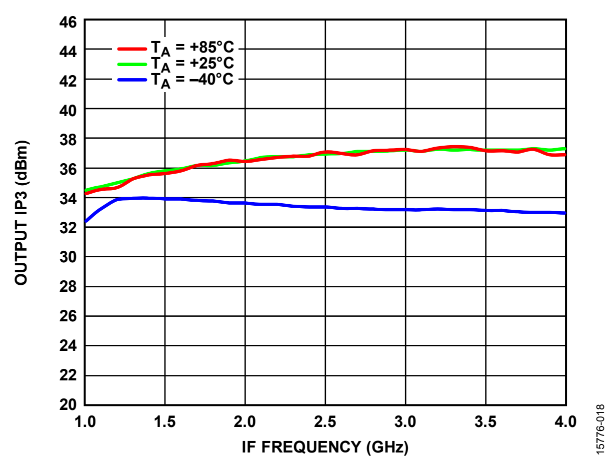


Figure 18. Output IP3 vs. IF Frequency at Various Temperatures, RF Frequency = 23 GHz

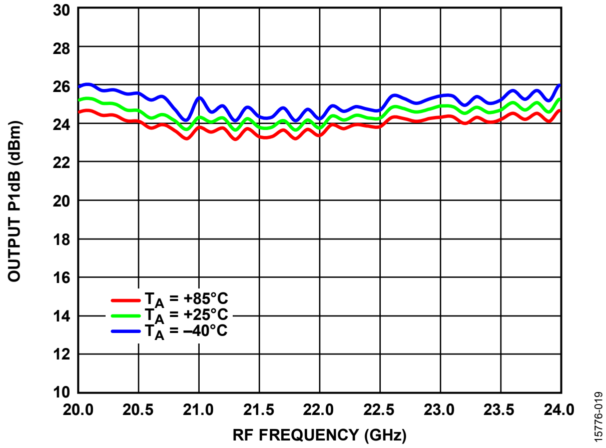


Figure 19. Output P1dB vs. RF Frequency at Various Temperatures

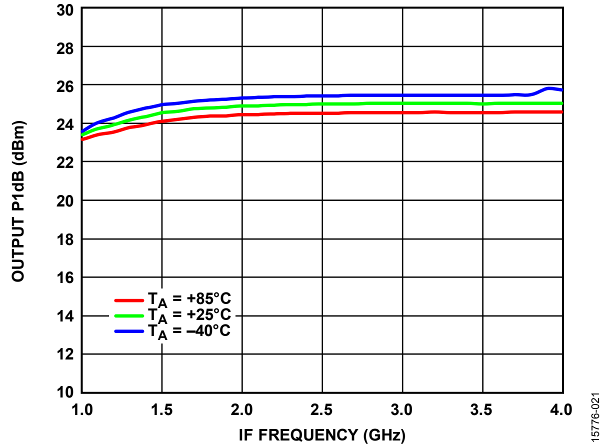


Figure 21. Output P1dB vs. IF Frequency at Various Temperatures, RF Frequency = 23 GHz

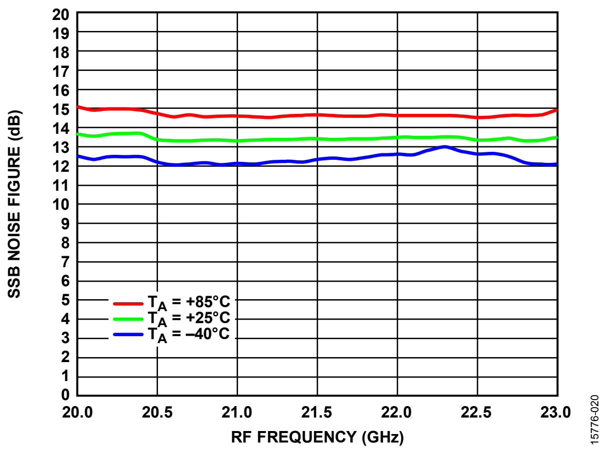


Figure 20. SSB Noise Figure vs. RF Frequency at Various Temperatures

Figure 22. SSB Noise Figure vs. LO Power, RF Frequency = 23 GHz

PERFORMANCE vs. GAIN REGULATION

Data specified at VDRF1 and VDRF2 = 5 V, VDLO = 3.5 V, IDRF1 = 220 mA, IDRF2 = 75 mA, T_A = 25°C, LO = 0 dBm, IF frequency = 3 GHz, and taken with Mini-Circuits QCN-45+ power splitter/combiner, unless otherwise noted. V_{CTL} is varied for gain regulation.

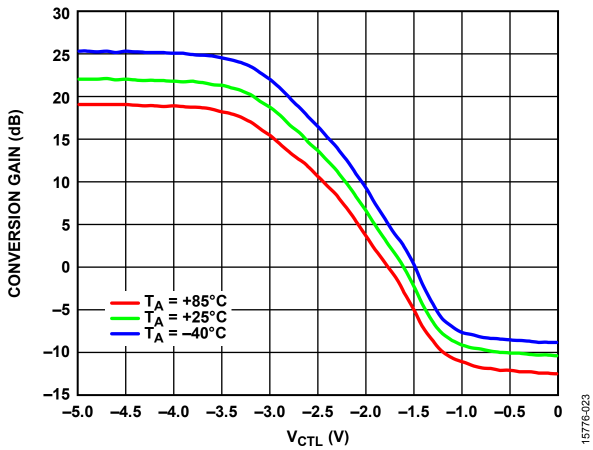


Figure 23. Conversion Gain vs. Control Voltage (V_{CTL}) at Various Temperatures, RF Frequency = 18 GHz, Lower Sideband

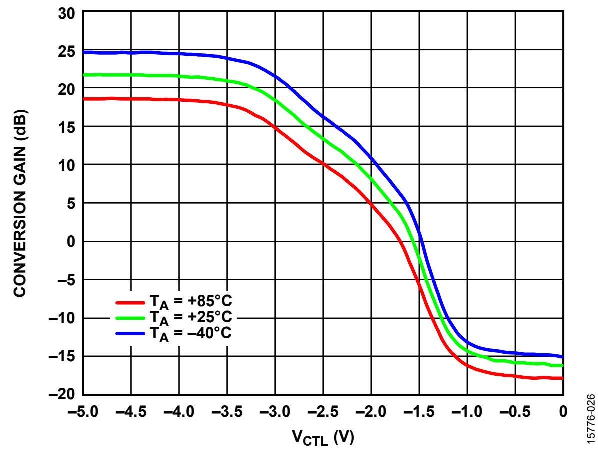


Figure 26. Conversion Gain vs. V_{CTL} at Various Temperatures, RF Frequency = 23 GHz, Upper Sideband

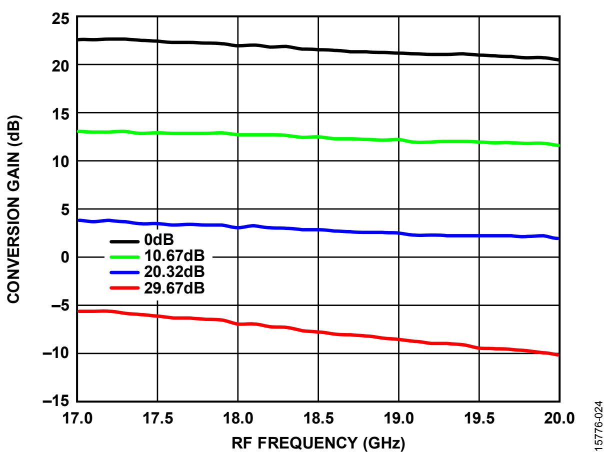


Figure 24. Conversion Gain vs. RF Frequency at Various Attenuation Levels, Lower Sideband

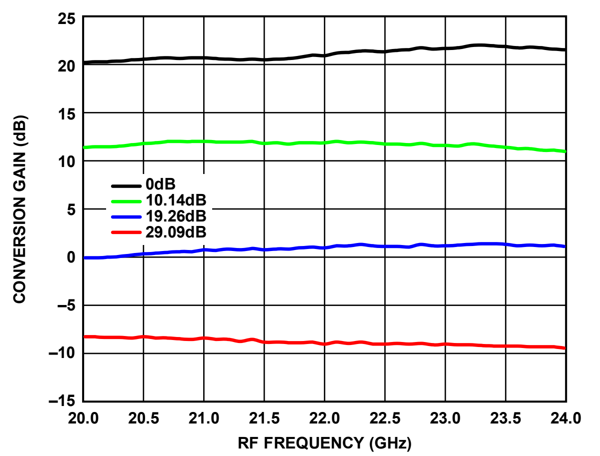


Figure 27. Conversion Gain vs. RF Frequency at Various Attenuation Levels, Upper Sideband

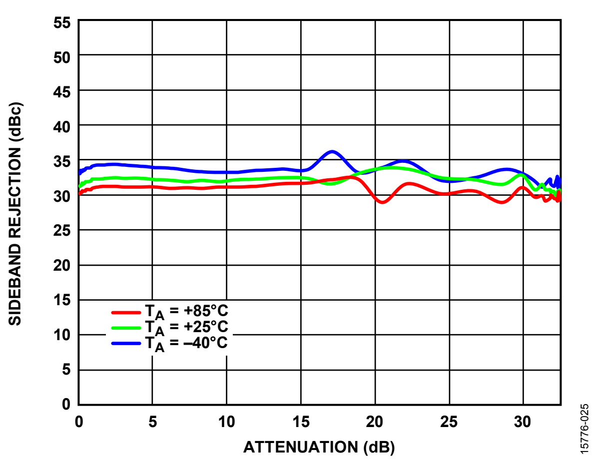


Figure 25. Sideband Rejection vs. Attenuation at Various Temperatures, RF Frequency = 18 GHz, Lower Sideband

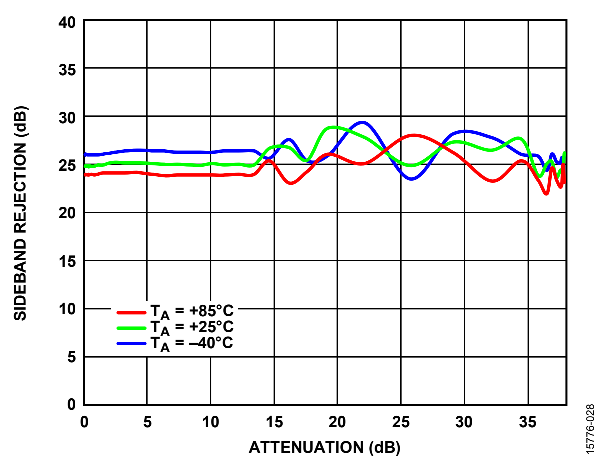


Figure 28. Sideband Rejection vs. Attenuation at Various Temperatures, RF Frequency = 23 GHz, Upper Sideband

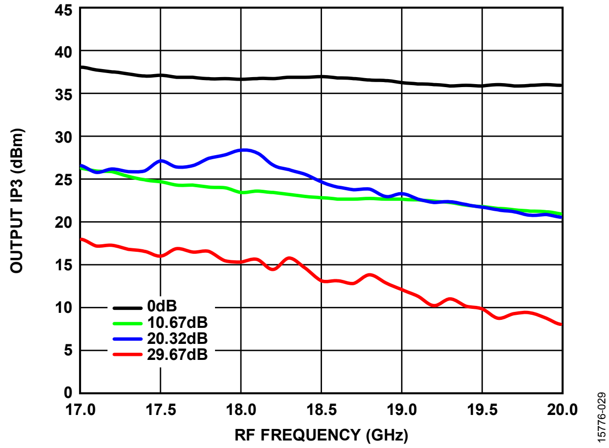


Figure 29. Output IP3 vs. RF Frequency at Various Attenuation Levels, Lower Sideband

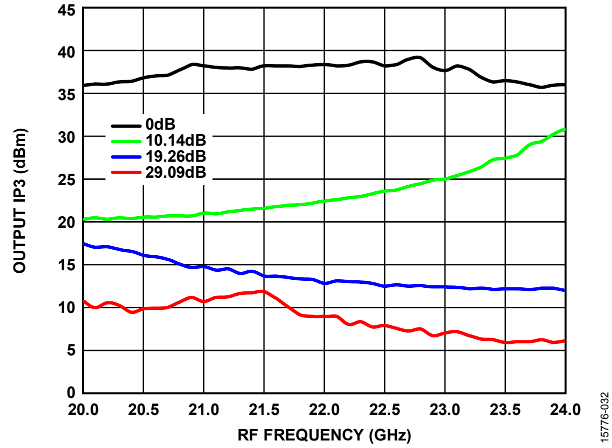


Figure 32. Output IP3 vs. RF Frequency at Various Attenuation Levels, Upper Sideband

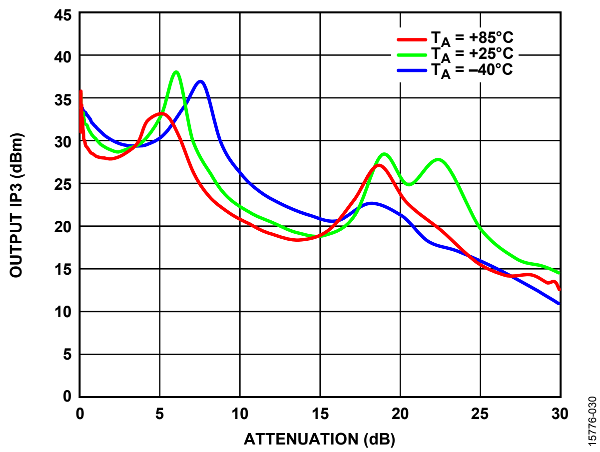


Figure 30. Output IP3 vs. Attenuation at Various Temperatures, RF Frequency = 18 GHz, Lower Sideband

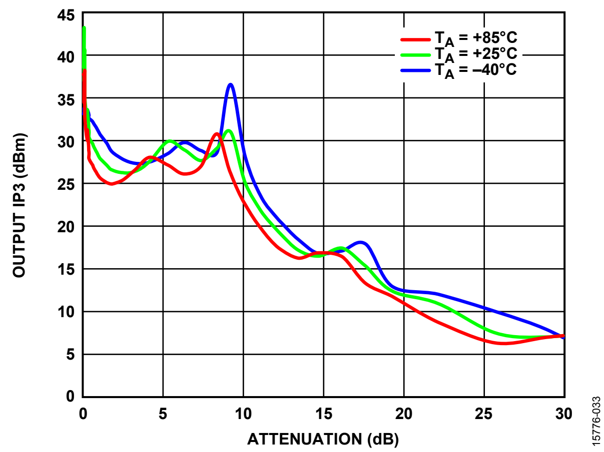


Figure 33. Output IP3 vs. Attenuation at Various Temperatures, RF Frequency = 23 GHz, Upper Sideband

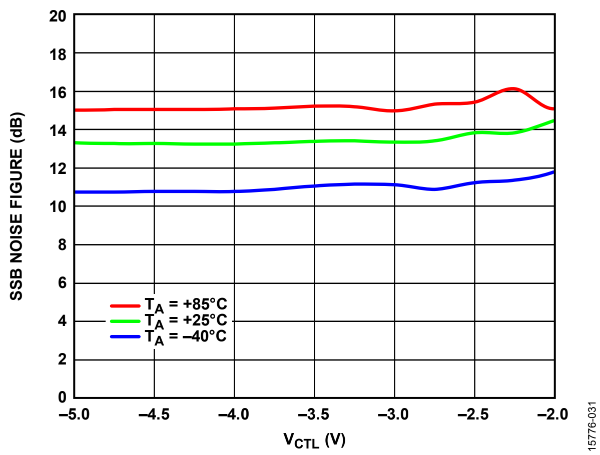


Figure 31. SSB Noise Figure vs. V_{CTL} at Various Temperatures, RF Frequency = 18 GHz, Lower Sideband

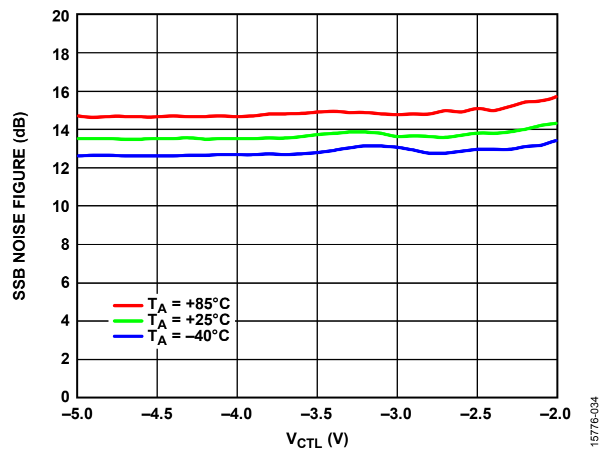


Figure 34. SSB Noise Figure vs. V_{CTL} at Various Temperatures, RF Frequency = 23 GHz, Upper Sideband

PERFORMANCE vs. LO POWER

Data specified at VDRF1 and VDRF2 = 5 V, VDLO = 3.5 V, IDRF1 = 220 mA, IDRF2 = 75 mA, T_A = 25°C, IF frequency = 3 GHz, and taken with Mini-Circuits QCN-45+ power splitter/combiner, unless otherwise noted. VCTL2 and VCTL3 = −5 V, unless otherwise noted.

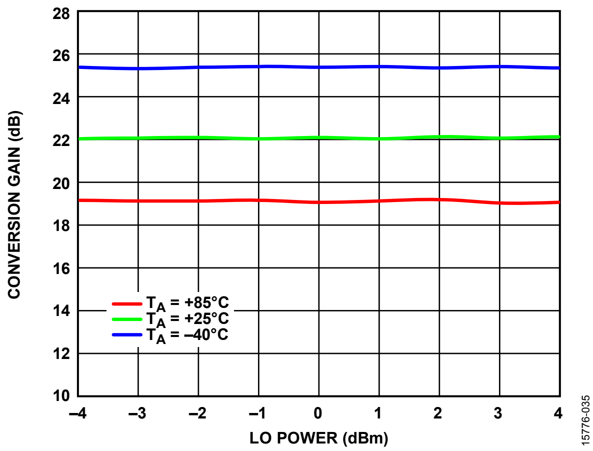


Figure 35. Conversion Gain vs. LO Power at Various Temperatures, RF Frequency = 18 GHz, Lower Sideband

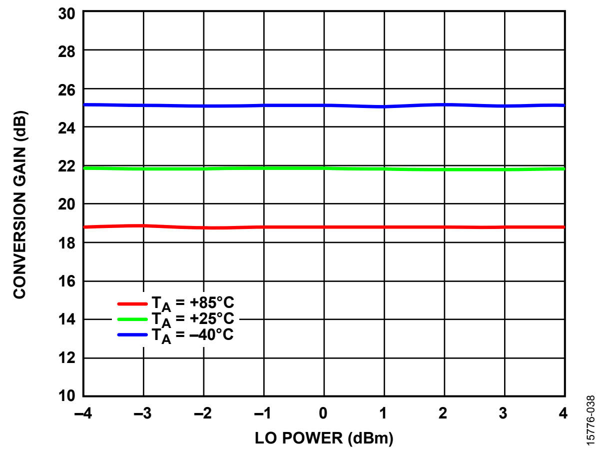


Figure 38. Conversion Gain vs. LO Power at Various Temperatures, RF Frequency = 23 GHz, Upper Sideband

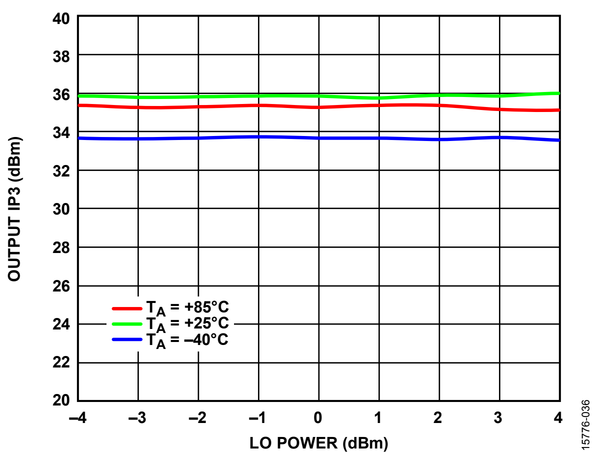


Figure 36. Output IP3 vs. LO Power at Various Temperatures, RF Frequency = 18 GHz, Lower Sideband

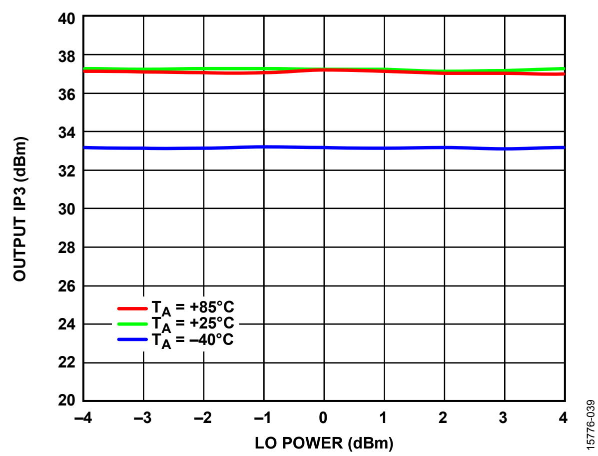


Figure 39. Output IP3 vs. LO Power at Various Temperatures, RF Frequency = 23 GHz, Upper Sideband

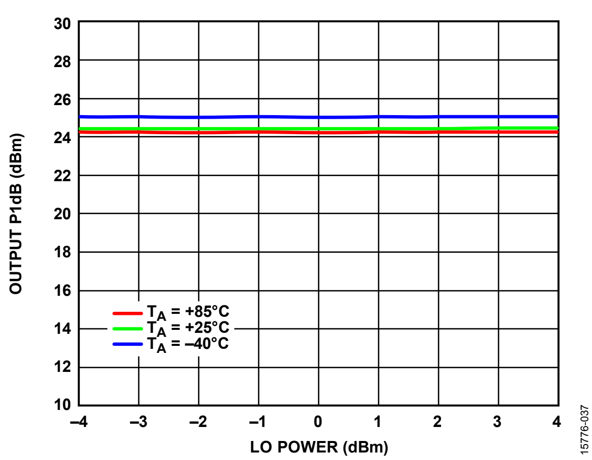


Figure 37. Output P1dB vs. LO Power at Various Temperatures, RF Frequency = 18 GHz, Lower Sideband

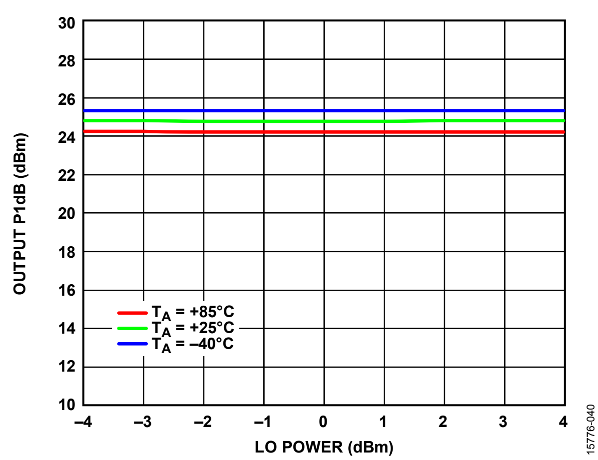


Figure 40. Output P1dB vs. LO Power at Various Temperatures, RF Frequency = 23 GHz, Upper Sideband

LEAKAGE AND RETURN LOSS PERFORMANCE

Data specified at VDRF1 and VDRF2 = 5 V, VDLO = 3.5 V, IDRF1 = 220 mA, IDRF2 = 75 mA, T_A = 25°C, LO = 0 dBm, and taken with Mini-Circuits QCN-45+ power splitter/combiner, unless otherwise noted. VCTL2 and VCTL3 = −5 V unless otherwise noted.

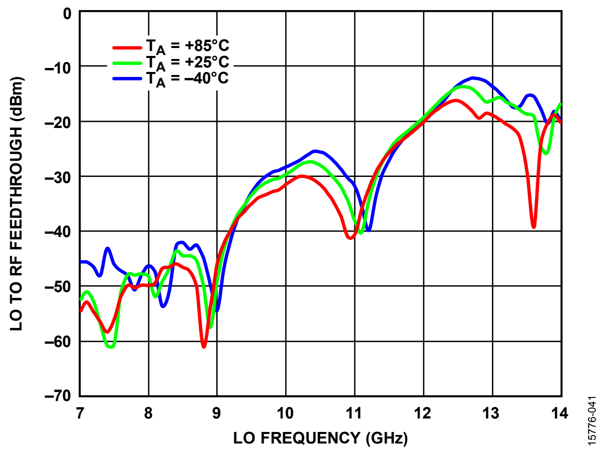


Figure 41. LO to RF Feedthrough vs. LO Frequency at Various Temperatures

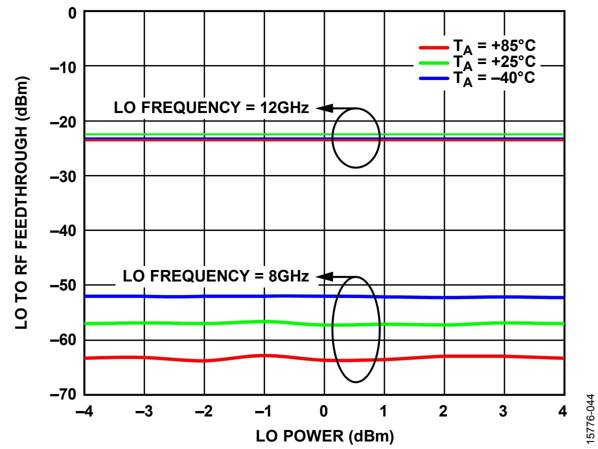


Figure 44. LO to RF Feedthrough vs. LO Power at Various Temperatures and LO Frequencies

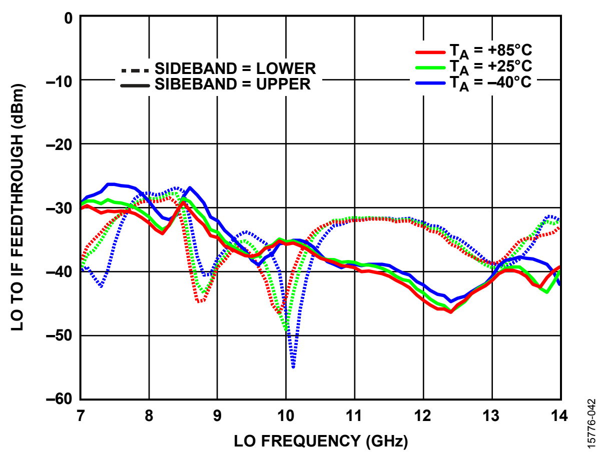


Figure 42. LO to IF Feedthrough vs. LO Frequency at Various Temperatures and Sidebands

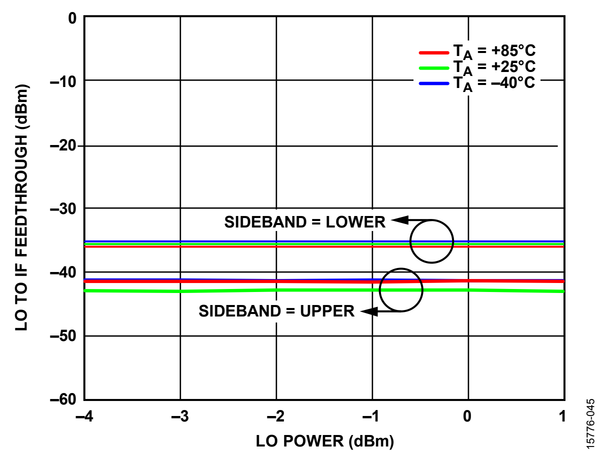


Figure 45. LO to IF Feedthrough vs. LO Power at Various Temperatures and Sidebands, LO Frequency = 10 GHz

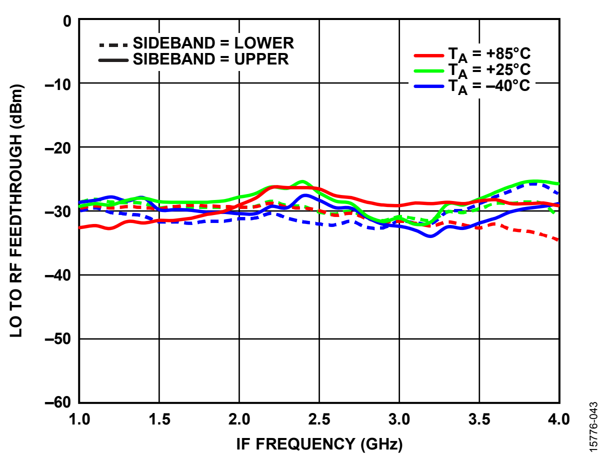


Figure 43. LO to RF Feedthrough vs. IF Frequency at Various Temperatures and Sidebands, IFx Pin = 0 dBm

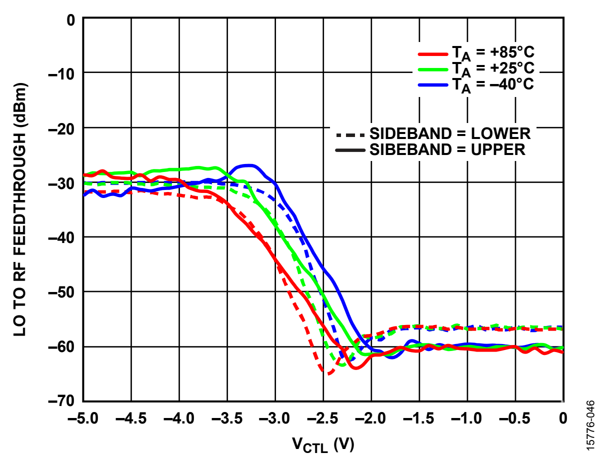


Figure 46. LO to RF Feedthrough vs. V_{CTL} at Various Temperatures and Sidebands, IFx Pin = 0 dBm

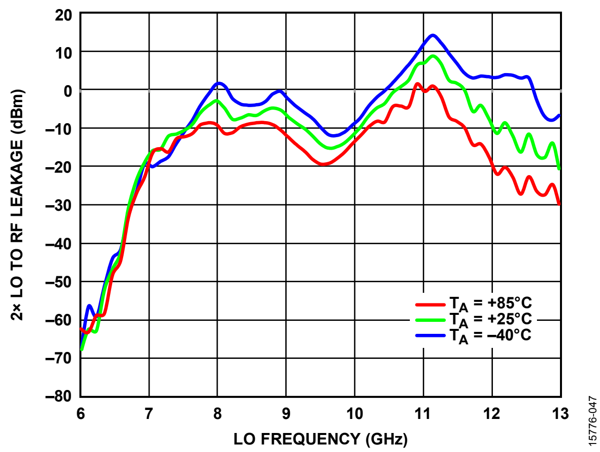


Figure 47. 2× LO to RF Leakage vs. LO Frequency at Various Temperatures, Without Nulling

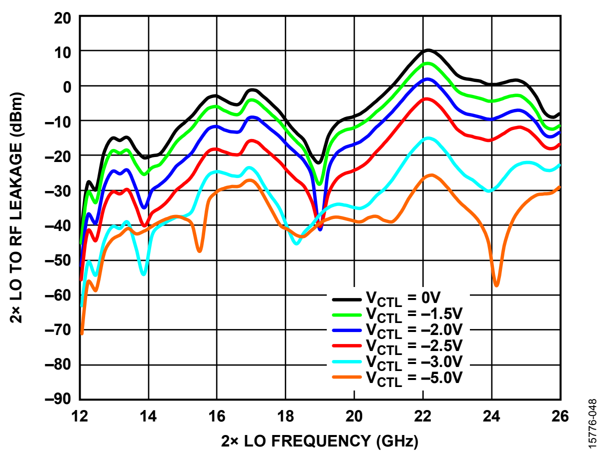


Figure 48. 2× LO to RF Leakage vs. 2× LO Frequency at Various Attenuation Levels (V_{CTL})

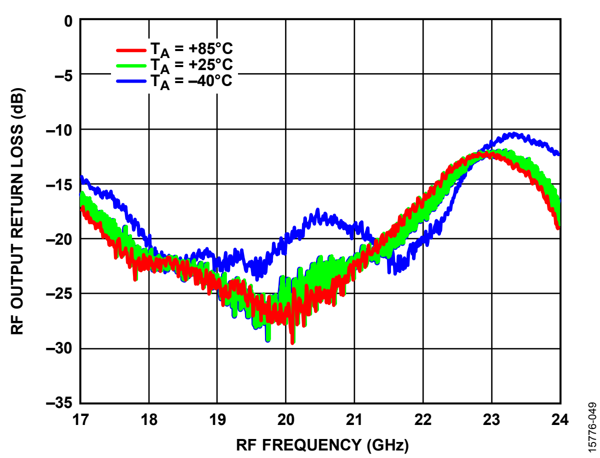


Figure 49. RF Output Return Loss vs. RF Frequency at Various Temperatures, LO Frequency = 10 GHz, 0 dBm

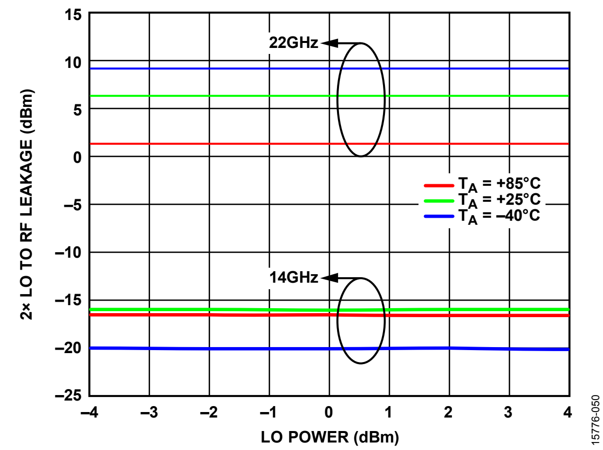


Figure 50. 2× LO to RF Leakage vs. LO Power at Various Temperatures and LO Frequencies, Without Nulling

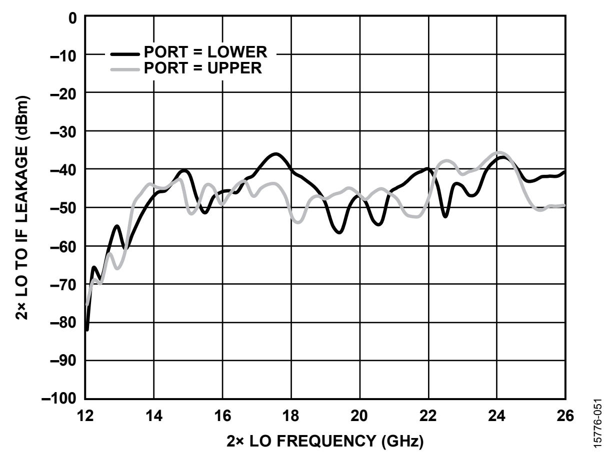


Figure 51. 2× LO to IF Leakage vs. 2× LO Frequency for Upper Sideband and Lower Sideband

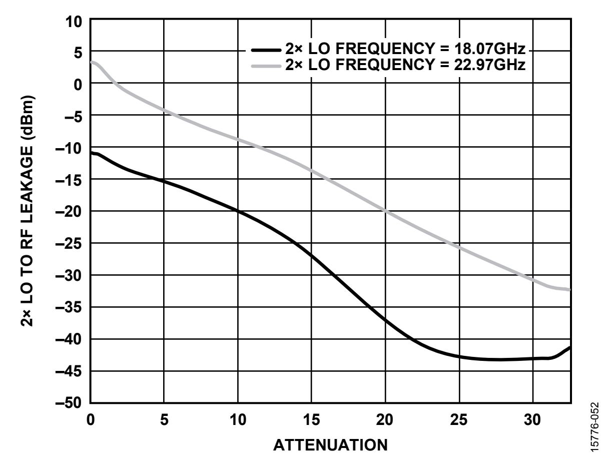


Figure 52. 2× LO to RF Leakage vs. Attenuation for Various Frequencies

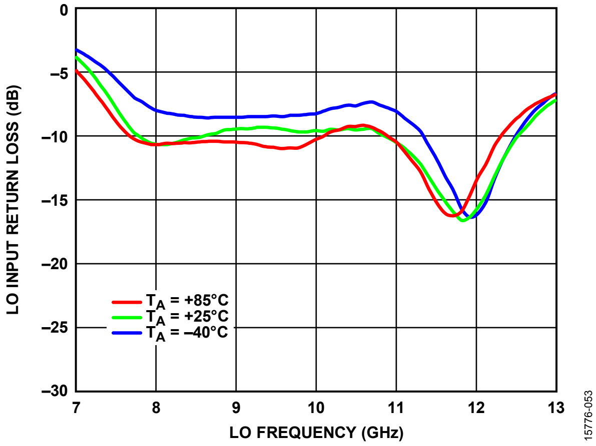


Figure 53. LO Input Return Loss vs. LO Frequency at Various Temperatures, LO = 0 dBm

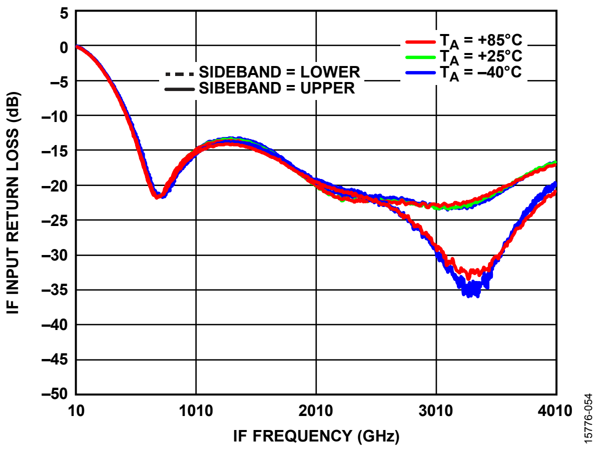


Figure 54. IF Input Return Loss vs. IF Frequency at Various Temperatures and Sidebands

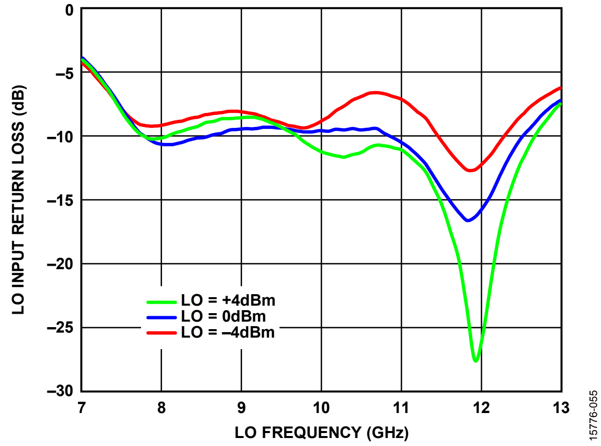


Figure 55. LO Input Return Loss vs. LO Frequency at Various LO Powers

M × N SPURIOUS PERFORMANCE

Mixer spurious products are measured in dBc from the RF output power level. N/A means not applicable.

Lower Sideband

Mixer spurious products are measured in dBc from the RF output power level. Spurious values are measured using the following equation: N × LO – M × IF. N/A means not applicable. The frequencies are referred from the frequencies applied to the pin of the ADMV1011.

IF = 2 GHz at 0 dBm, LO = 10 GHz at 0 dBm.

		N × LO				
		1	2	3	4	5
M × IF	0	52.2	30.9	56.1	63.4	77.1
	1	68.2	0	61.1	66.2	99.1
	2	73.6	47.1	55.9	43.5	99
	3	59	43.2	50.2	71.8	101.4
	4	77.1	58.7	21.4	65.5	99
	5	N/A	52.3	30.9	56.3	63.2

IF = 3 GHz at 0 dBm, LO = 10.5 GHz at 0 dBm.

		N × LO				
		1	2	3	4	5
M × IF	0	50.5	21.8	69.6	62.1	N/A
	1	73	0	64.1	58.9	96.6
	2	95.7	41.7	59.8	43.9	97.8
	3	124.6	42.7	71.2	65.2	97.5
	4	120.8	74.5	81.1	64.8	100.4
	5	95.4	48.1	76	65	102.8

IF = 4 GHz at 0 dBm, LO = 11 GHz at 0 dBm.

		N × LO				
		1	2	3	4	5
M × IF	0	60.2	9.8	68.1	76.1	N/A
	1	91.9	0	74.9	50.7	96.9
	2	98.9	33.9	70	44.7	98.8
	3	118.8	50.5	70.8	56.6	99.7
	4	114	72.8	81.9	63.4	100.5
	5	117.9	96.3	99.5	66.5	101.4

Upper Sideband

Mixer spurious products are measured in dBc from the RF output power level. Spurious values are measured using the following equation: N × LO + M × IF. N/A means not applicable. The frequencies are referred from the frequencies applied to the pin of the ADMV1011.

IF = 2 GHz at 0 dBm, LO = 10.5 GHz at 0 dBm.

		N × LO				
		1	2	3	4	5
M × IF	0	50.5	22.3	68.5	53.7	N/A
	1	58.2	0	81.9	65.6	N/A
	2	69.5	41.1	90.1	47.6	N/A
	3	81.7	41.2	95.3	78.5	N/A
	4	91.1	59.9	102.8	83	N/A
	5	93.9	70.4	101.4	N/A	N/A

IF = 3 GHz at 0 dBm, LO = 10 GHz at 0 dBm.

		N × LO				
		1	2	3	4	5
M × IF	0	50.9	30.2	54.7	72.1	78.4
	1	58	0	82.2	67.1	N/A
	2	74.9	58.3	90.9	48.5	N/A
	3	87.1	66.6	98.2	92.3	N/A
	4	79.4	100	101.3	N/A	N/A
	5	N/A	N/A	N/A	N/A	N/A

IF = 4 GHz at 0 dBm, LO = 9.5 GHz at 0 dBm.

		N × LO				
		1	2	3	4	5
M × IF	0	53.3	47.1	42.1	55.9	94
	1	58.1	0	79.6	79.7	N/A
	2	64.8	63.7	97.9	49.8	N/A
	3	80.6	62.4	94.8	95.8	N/A
	4	96	103.5	98.3	N/A	N/A
	5	104.3	100.6	94.8	N/A	N/A

THEORY OF OPERATION

The ADMV1011 is a GaAs, MMIC, double sideband upconverter in a RoHS compliant package optimized for upper sideband and lower sideband point to point microwave radio applications operating in the 17 GHz to 24 GHz output frequency range. The ADMV1011 supports LO input frequencies of 8 GHz to 12 GHz and IF input frequencies of 2 GHz to 4 GHz.

The ADMV1011 uses a variable gain RF amplifier and an I/Q preceded by a double balanced mixer, where a driver amplifier drives the LO (see Figure 1). The combination of design, process, and packaging technology allows the functions of these subsystems to be integrated into a single die, using mature packaging and interconnection technologies to provide a high performance, low cost design with excellent electrical, mechanical, and thermal properties. In addition, the need for external components is minimized, optimizing cost and size.

LO DRIVER AMPLIFIER

The LO driver amplifier takes a single LO input and doubles the frequency, amplifying it to the desired LO signal level for the mixer to operate optimally. The LO driver amplifier requires a single dc bias voltage (VDLO), which draws about 160 mA at 3.5 V under the LO drive. The LO drive range of −4 dBm to +4 dBm makes it compatible with Analog Devices, Inc., wideband synthesizer portfolio without the requirement for an external LO driver amplifier.

MIXER

The mixer is an I/Q double balanced mixer and reduces the need for filtering unwanted sideband. An external 90° hybrid is required to select the desired sideband of operation.

The ADMV1011 has been optimized to work with the Mini-Circuits QCN-45+ RF 90° hybrid.

RF AMPLIFIER

The RF amplifier is a variable gain amplifier where the gain can be adjusted by changing the control voltages (VCTL2 and VCTL3). The RF amplifier requires two dc bias voltages (VDRF1 and VDRF2) and two dc gate bias voltages (VGRF1 and VGRF2) to operate. Starting at −1.8 V at the gate supply (VGRF1 and VGRF2), the RF amplifier is biased at 5 V (VDRF1 and VDRF2). Then, the gate bias (VGRF1 and VGRF2) is varied until the desired RF amplifier bias current (IDRF1 and IDRF2) is achieved. The desired RF amplifier bias current is 220 mA for IDRF1 and 75 mA for IDRF2 under small signal conditions.

The ADMV1011 has an internal band-pass filter between the mixer and the RF driver amplifier that reduces LO leakage and filters out the lower sideband at the RF output. The balanced input drive allows exceptional linearity performance compared to similar single-ended solutions.

The typical application circuit (see Figure 56) shows the necessary external components on the bias lines to eliminate any undesired stability problems for the RF amplifier and the LO amplifier.

The ADMV1011 upconverter comes in a compact, thermally enhanced, 4.9 mm × 4.9 mm, 32-terminal ceramic leadless chip carrier (LCC) package. The ADMV1011 operates over the −40°C to +85°C temperature range.

APPLICATIONS INFORMATION

The evaluation board and the typical application circuit are optimized for low-side LO (upper sideband) performance with the Mini-Circuit QCN-45+ RF 90° hybrid.

The ADMV1011 can support IF frequencies from 4 GHz to dc because the I/Q mixers of the devices are double balanced.

TYPICAL APPLICATION CIRCUIT

The typical application circuit is shown in Figure 56. The application circuit shown has been replicated for the evaluation board circuit.

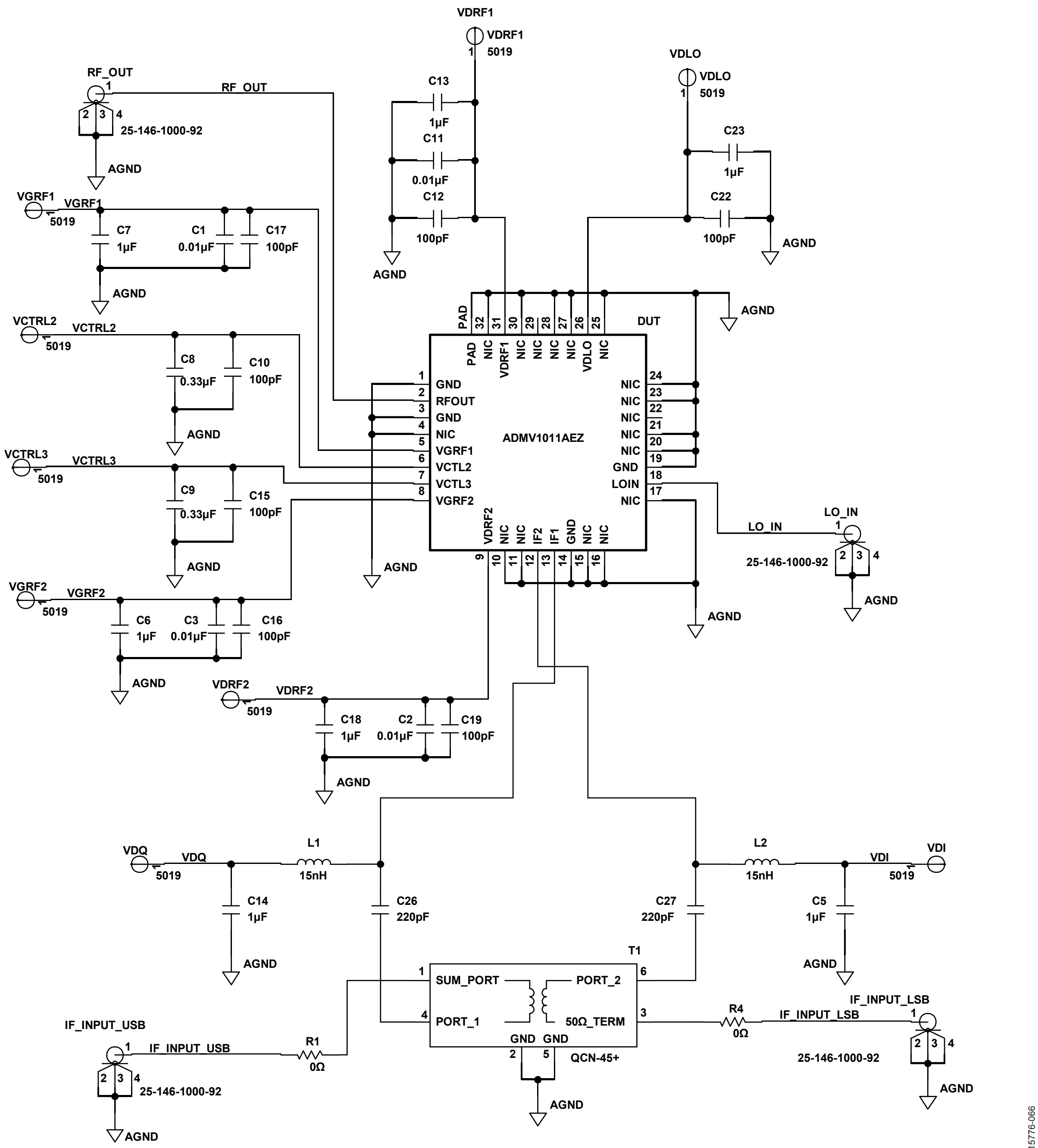


Figure 56. Typical Application Circuit

FINER RESOLUTION GAIN REGULATION

The data shown in the Performance vs. Gain Regulation section is shown based on VCTRL2 and VCTRL3 being equal. Finer resolution of the gain regulation can be obtained if VCTRL2 and VCTRL3 are used separately. Note that the overall dynamic range stays the same. Figure 57 through Figure 60 show the output IP3 and conversion gain when VCTRL2 and VCTRL3 are used separately.

Figure 57 and Figure 58 show the upper sideband performance for RFOUT at 23 GHz. Figure 59 and Figure 60 show the lower sideband performance for RFOUT at 18 GHz. In Figure 57 and Figure 59, VCTRL3 is held constant at −5 V, and VCTRL2 is swept from −5 V to −0.75 V. When VCTRL2 = −0.75 V, VCTRL3 is swept from −5 V to −0.75 V. In Figure 58 and Figure 60, VCTRL2 is held constant at −5 V, and VCTRL3 is swept from −5 V to −0.75 V. When VCTRL3 = −0.75 V, VCTRL 2 is swept from −5 V to −0.75 V.

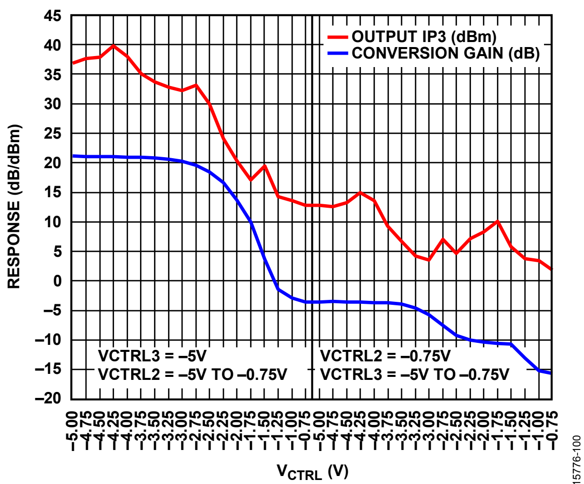


Figure 57. Output IP3 and Conversion Gain vs. V_{CTRL} when VCTRL2 and VCTRL3 Used Separately for the Upper Sideband at RFOUT = 23 GHz, T_A = 25°C, LO = 0 dBm, IF = 3 GHz

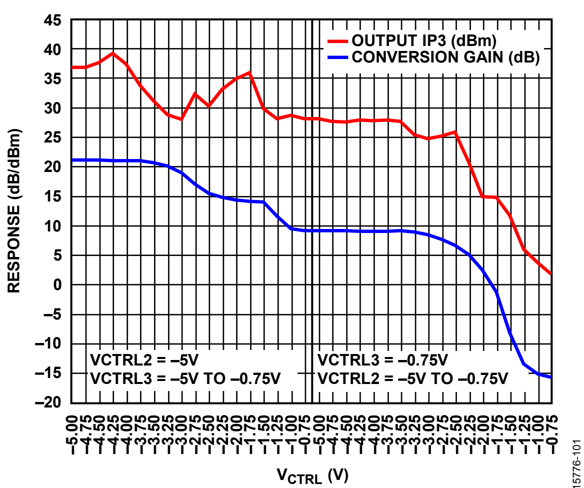


Figure 58. Output IP3 and Conversion Gain vs. V_{CTRL} when VCTRL2 and VCTRL3 Used Separately for Upper Sideband at RFOUT = 23 GHz, T_A = 25°C, LO = 0 dBm, IF = 3 GHz

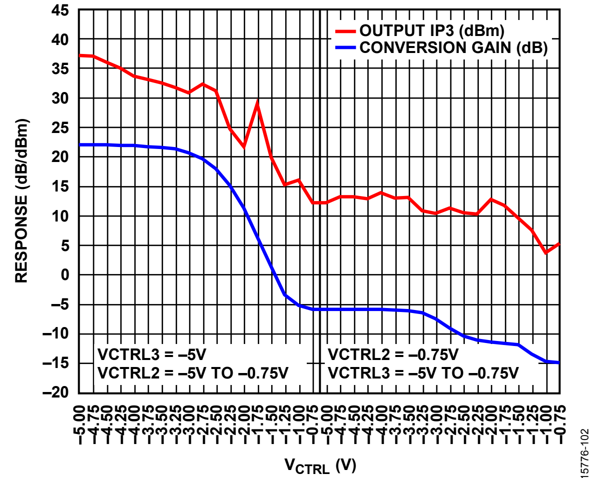


Figure 59. Output IP3 and Conversion Gain vs. V_{CTRL} when VCTRL2 and VCTRL3 Used Separately for Lower Sideband at RFOUT = 18 GHz, T_A = 25°C, LO = 0 dBm, IF = 3 GHz

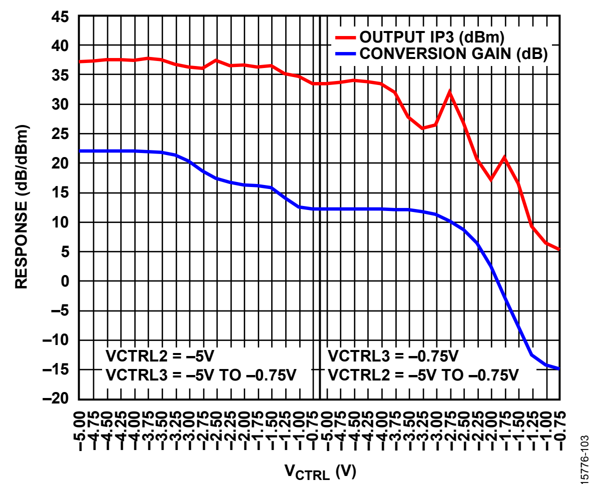


Figure 60. Output IP3 and Conversion Gain vs. V_{CTRL} when VCTRL2 and VCTRL3 Used Separately for Lower Sideband at RFOUT = 18 GHz, T_A = 25°C, LO = 0 dBm, IF = 3 GHz

Figure 61 shows the conversion gain vs. VCTRL2 for different VCTRL3 voltages at RFOUT = 23 GHz. Figure 61 shows 30 dB attenuation can be obtained at VCTRL2 = −1 V and VCTRL3 = −2 V. The overall attenuation range is 35 dB.

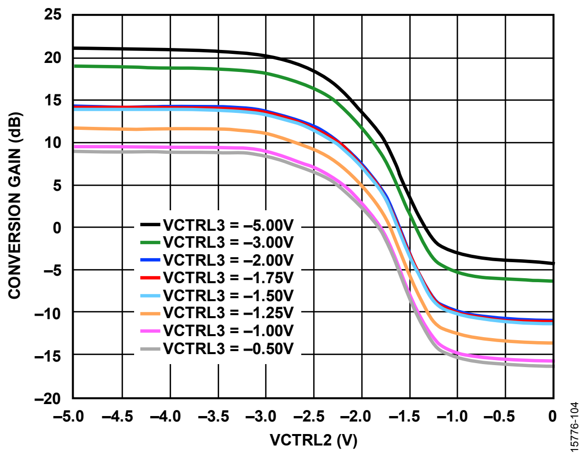


Figure 61. Conversion Gain vs. VCTRL2 at Different VCRTL3 Voltages

Figure 62 shows the conversion gain vs. VCTRL3 for different VCTRL2 voltages at RFOUT = 23 GHz. Figure 62 shows 30 dB attenuation can be obtained at VCTRL2 = −1 V and VCTRL3 = −1 V. The overall attenuation range is 37 dB.

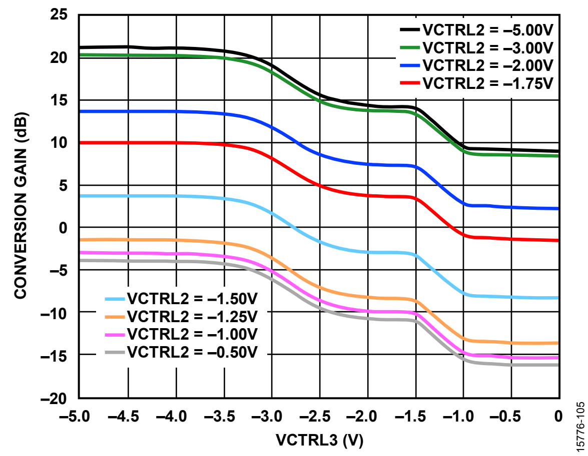


Figure 62. Conversion Gain vs. VCTRL3 at Different VCRTL2 Voltages

EVALUATION BOARD INFORMATION

The circuit board used in the application must use RF circuit design techniques. Signal lines must have 50 Ω impedance, and the package ground leads and exposed pad must be connected directly to the ground plane (see Figure 63 and Figure 64). Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation circuit board shown in Figure 65 is available from Analog Devices, upon request.

Layout

Solder the exposed pad on the underside of the ADMV1011 to a low thermal and electrical impedance ground plane. This pad is typically soldered to an exposed opening in the solder mask on the evaluation board. Connect these ground vias to all other ground layers on the evaluation board to maximize heat dissipation from the device package. Figure 63 shows the PCB land pattern footprint for the EVAL-ADMV1011, and Figure 64 shows the solder paste stencil for the EVAL-ADMV1011.

Power-On Sequence

Take the following steps to turn on the EVAL-ADMV1011:

1. Power up VGRF1 andVGRF2 with a −1.8 V supply.
2. Power up VCTL2 and VCTL3 with a −5 V supply for maximum conversion gain.
3. Power up VDRF1 and VDRF2 with a 5 V supply.
4. Power up VDLO with a 3.5 V supply.
5. Adjust the VGRF1 supply between −1.8 V to −0.8 V until IDRF1 = 220 mA.
6. Adjust the VGRF2 supply between −1.8 V to −0.8 V until IDRF2 = 75 mA.
7. Connect LOIN to the LO signal generator with a LO power between −4 dBm to +4 dBm.
8. For the upper sideband, add a 0 Ω resistor (R1) and remove the R4 resistor from the board. For the lower sideband, add a 0 Ω resistor (R4) and remove the R1 resistor from the board.
9. Apply the IF signal to the appropriate port.

Power-Off Sequence

Take the following steps to turn off the EVAL-ADMV1011:

1. Turn off the LO and IF signals.
2. Set VGRF1 and VGRF2 to −1.8 V.
3. Set VCTL2 and VCTL3 to 0 V.
4. Set the VDRF1 and VDRF2 supplies to 0 V and then turn off the VDRF1 and VDRF2 supplies.
5. Set the VDLO supply to 0 V and then turn off the VDLO supply.
6. Turn off the VGRF1, VGRF2, VCTL2, and VCTL3 supplies.

2× LO Suppression

The EVAL-ADMV1011 can suppress the 2× LO signal through the VDI and VDQ test points. The common mode of the two IF signals is 0 V. Injecting a nonzero voltage at VDI and VDQ can change the 2× LO level. The 2× LO signal is referenced from the LOIN pin of the ADMV1011. The VDI and VDQ voltage needs to be changed iteratively to get the desired level of 2 × LO suppression. To prevent device malfunction or failure, the current to the VDI and VDQ test points (IDI and IDQ) must not source or sink more than 2 mA of current.

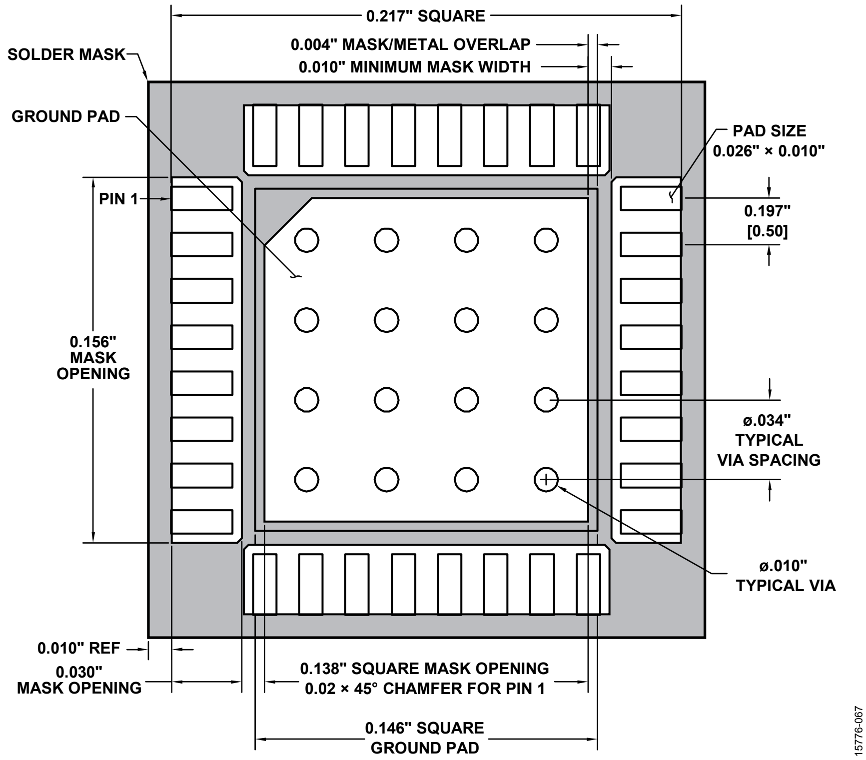


Figure 63. PCB Land Pattern Footprint of the EVAL-ADMV1011

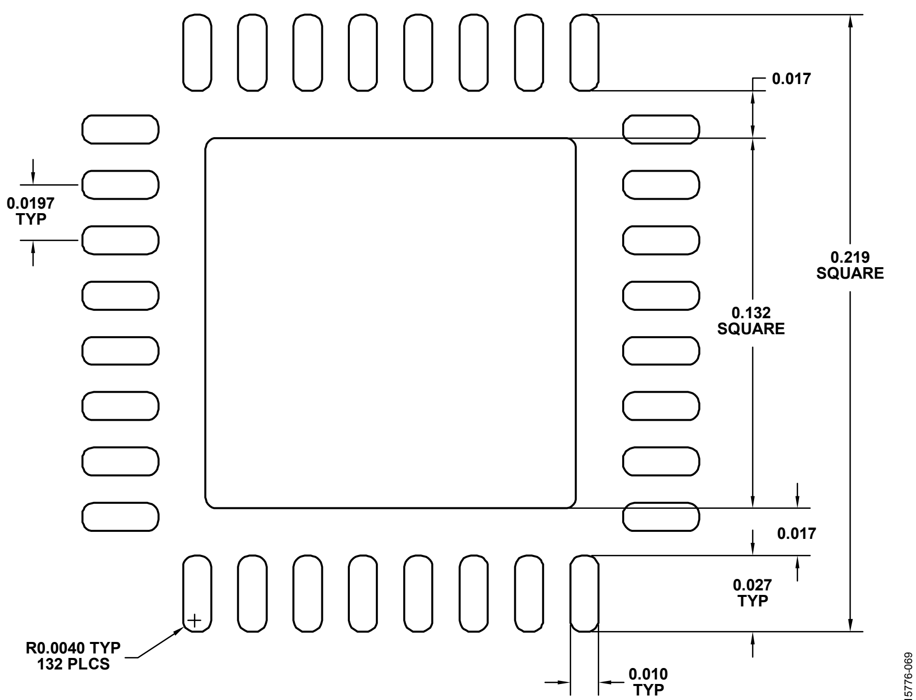
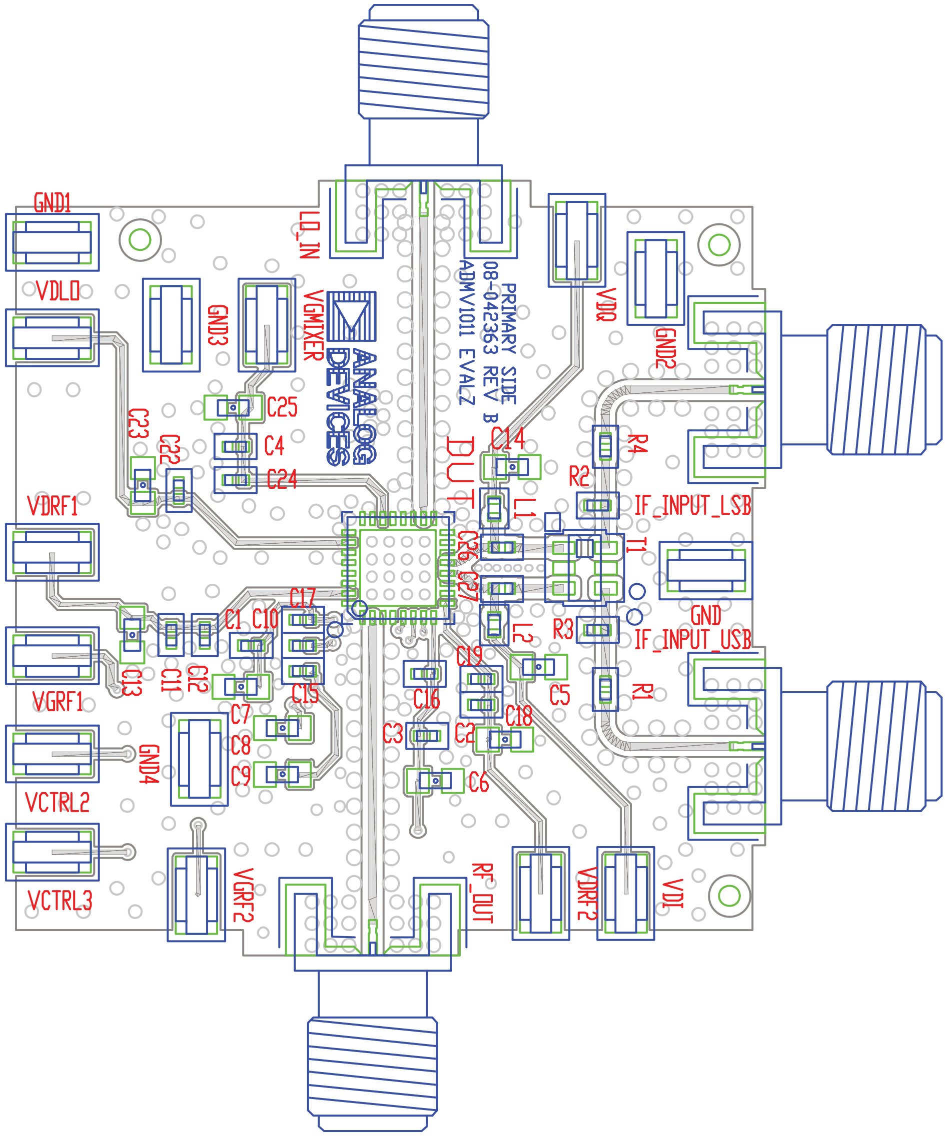


Figure 64. Solder Paste Stencil of the EVAL-ADMV1011



NOTES
1. NOT ALL COMPONENTS OR BIAS LINES ARE USED ON THE EVALUATION BOARD.

15776-068

Figure 65. EVAL-ADMV1011 Evaluation Board Top Layer

BILL OF MATERIALS

Table 7.

Qty.	Reference Designator	Description	Manufacturing/Part No.
1	Evaluation board	PCB	Analog Devices/08_042363a
4	C1 to C3, C11	0.01 µF ceramic capacitors, X7R, 0402	Murata/GRM155R71E103KA01D
7	C10, C12, C15 to C17, C19, C22	100 pF multilayer ceramic capacitors, NP0, high temperature, C0402	TDK/C1005NP01H101J050BA
7	C5 to C7, C13, C14, C18, C23	1 µF monolithic ceramic capacitors, X5R, C0603	Murata/GRM188R61E105KA12D
2	C8, C9	0.33 µF ceramic capacitors, X5R, C0603	AVX/0603YD334KAT2A
2	C26, C27	220 pF ceramic capacitors, C0G, 0402, C0402	Murata/GRM1555C1H221JA01D
10	AGND, VDI, VDQ, VDLO, VDRF1, VDRF2, VGRF1, VGRF2, VCTL2 to VCTL3	Connector PCB test points, compact mini, 5019, CNKEY5019	Keystone Electronic Corp/5019
4	LO_IN, RF_OUT, IF_INPUT_LSB, IF_INPUT_USB	Connector PCB SMA, K_SRI-NS, CNSMAL460W295H156	SRI Connector Gage/25-146-1000-92
2	L1, L2	15 nH inductor chips, 0402, L0402-2	Coilcraft/0402HP-15NXJLU
2	R1, R4	0 Ω resistors, chip surface-mounted diode jumper, 0402	Panasonic/ERJ-2GE0R00X
1	R2	50 Ω resistor, high frequency chip, R0402	Vishay Precision Group/FC0402E50R0BST1
1	R3	50 Ω resistor, high frequency chip, 0402, R0402	Vishay Precision Group/FC0402E50R0FST1
1	T1	Transformer power splitter/combiner, 2500 to 4500 MHz, TSML126W63H42	Mini-Circuits/QCN-45+
	Heatsink	Heatsink	114622-A/111332

OUTLINE DIMENSIONS

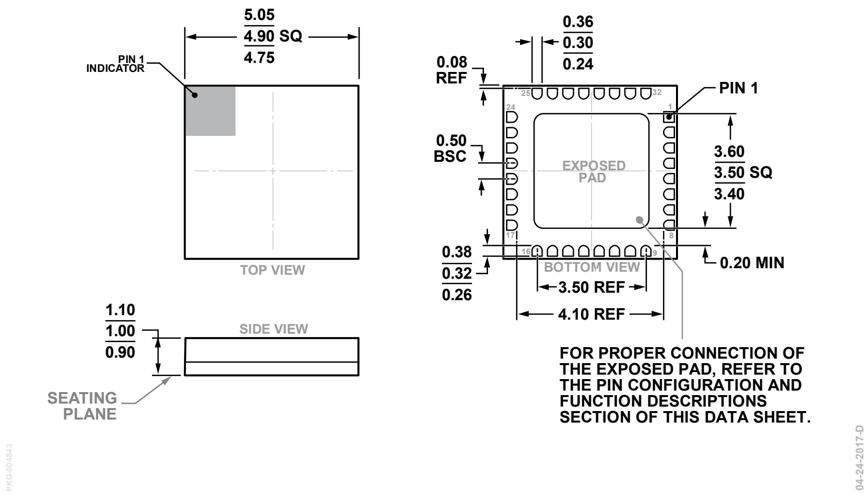


Figure 66. 32-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-32-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Body Material	Lead Finish	Package Description	Package Option
ADMV1011AEZ	−40°C to +85°C	Alumina Ceramic	Gold Over Nickel	32-Terminal LCC	E-32-1
ADMV1011AEZ-R7	−40°C to +85°C	Alumina Ceramic	Gold Over Nickel	32-Terminal LCC	E-32-1
ADM1011-EVALZ				Evaluation Board	

[1] Z = RoHS Compliant Part.