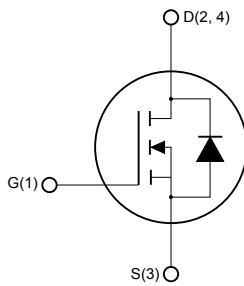


Automotive-grade N-channel 60 V, 0.07 Ω typ., 4 A STripFET II Power MOSFET in a SOT-223 package




SOT-223



Int_schem_nTnZ_SOT_223

Features

| Order code | V_{DS} | $R_{DS(on)}$ max. | I_D |
|------------|----------|-------------------|-------|
| STN4NF06L | 60 V | < 0.1 Ω | 4 A |

- AEC-Q101 qualified 
- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.



Product status link

[STN4NF06L](#)

Product summary

| | |
|-------------------|---------------|
| Order code | STN4NF06L |
| Marking | 4NF06L |
| Package | SOT-223 |
| Packing | Tape and reel |

1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|---|------------|---------------------|
| V_{DS} | Drain-source voltage ($V_{GS} = 0\text{ V}$) | 60 | V |
| V_{GS} | Gate-source voltage | ± 16 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 4 | A |
| | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 2.9 | A |
| $I_{DM}^{(2)}$ | Drain current (pulsed) | 16 | A |
| P_{TOT} | Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 3.3 | W |
| | Derating Factor | 0.026 | W/ $^\circ\text{C}$ |
| $dv/dt^{(3)}$ | Peak diode recovery avalanche energy | 10 | V/ns |
| $E_{AS}^{(4)}$ | Single pulse avalanche energy | 200 | mJ |
| T_{stg} | Storage temperature range | -55 to 150 | $^\circ\text{C}$ |
| T_J | Operating junction temperature range | | |

1. Current limited by the package.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 3\text{ A}$, $di/dt \leq 150\text{ A}/\mu\text{s}$, $V_{DD} = V_{(BR)DSS}$, $T_J \leq T_J\text{ max}$.
4. Starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = 4\text{ A}$, $V_{DD} = 30\text{ V}$.

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|---------------------|--|-------|---------------------------|
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb | 38 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-pcb}^{(2)}$ | | 100 | $^\circ\text{C}/\text{W}$ |
| $T_J^{(3)}$ | Maximum lead temperature for soldering purpose | 260 | $^\circ\text{C}$ |

1. When Mounted on FR-4 board with 1 inch² pad, 2 oz. of Cu. and $t < 10\text{ s}$.
2. When mounted on minimum recommended footprint.
3. For 10 s 1.6 mm from case.

2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified

Table 3. On-/off-states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|--|------|-------|-----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | 60 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$ | | | 1 | μA |
| | | $V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}, T_C = 125\text{ }^\circ\text{C}$ | | | 10 | μA |
| I_{GSS} | Gate-body leakage current | $V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$ | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | 1 | | 2.8 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}, I_D = 1.5\text{ A}$ | | 0.07 | 0.10 | Ω |
| | | $V_{GS} = 5\text{ V}, I_D = 1.5\text{ A}$ | | 0.085 | 0.12 | |

Table 4. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|---|------|------|------|------|
| C_{iss} | Input capacitance | $V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$ | - | 340 | | pF |
| C_{oss} | Output capacitance | | - | 63 | | pF |
| C_{rSS} | Reverse transfer capacitance | | - | 30 | | pF |
| Q_g | Total gate charge | $V_{DD} = 48\text{ V}, I_D = 3\text{ A}$ | - | 7 | 9 | nC |
| Q_{gs} | Gate-source charge | $R_G = 4.7\text{ }\Omega, V_{GS} = 5\text{ V}$ | - | 1.5 | | nC |
| Q_{gd} | Gate-drain charge | (see Figure 14. Test circuit for gate charge behavior) | - | 2.8 | | nC |

Table 5. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 30\text{ V}, I_D = 1.5\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 5\text{ V}$ | - | 9 | - | ns |
| t_r | Rise time | | - | 25 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | - | 20 | - | ns |
| t_f | Fall time | | - | 10 | - | ns |

Table 6. Source-drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|---|------|------|------|------|
| I_{SD} | Source-drain current | | - | | 4 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 16 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 4 \text{ A}$, $V_{GS} = 0 \text{ V}$ | - | | 1.5 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 4 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, | - | 50 | | ns |
| Q_{rr} | Reverse recovery charge | $V_{DD} = 25 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$ | - | 88 | | nC |
| I_{RRM} | Reverse recovery current | (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 3.5 | | A |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

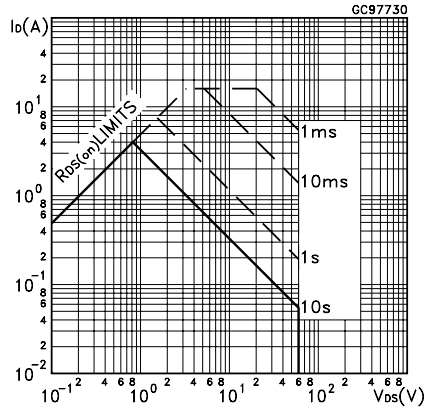


Figure 2. Thermal impedance

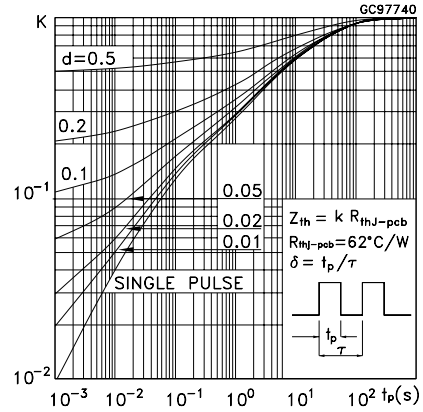


Figure 3. Output characteristics

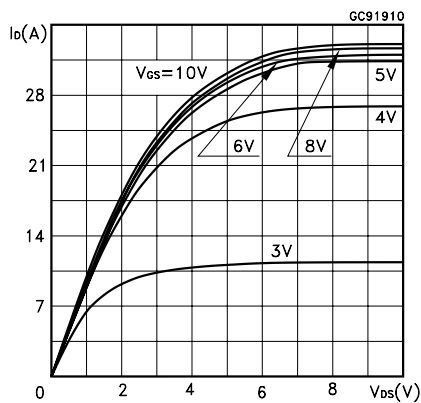


Figure 4. Transfer characteristics

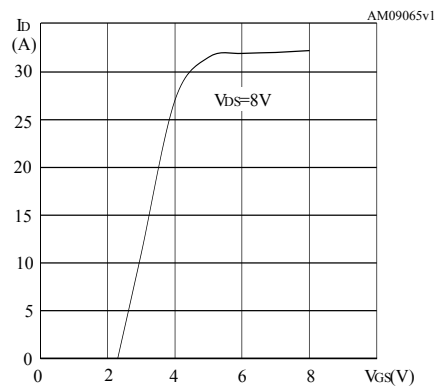


Figure 5. Static drain-source on resistance

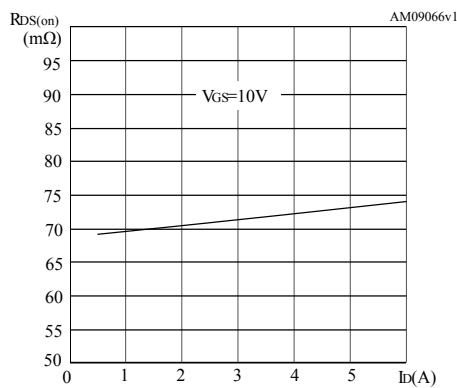


Figure 6. Gate charge vs. gate-source voltage

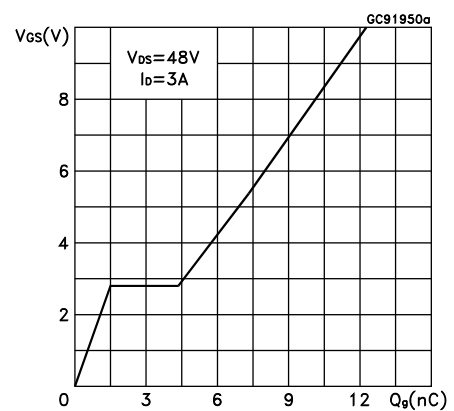


Figure 7. Capacitance variations

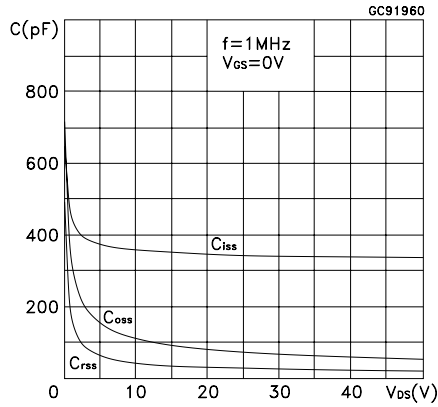


Figure 8. Normalized gate threshold voltage vs temperature

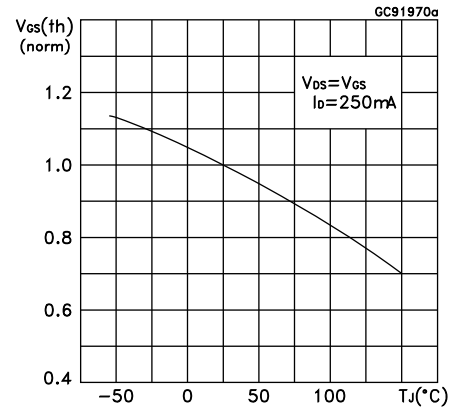


Figure 9. Normalized on-resistance vs temperature

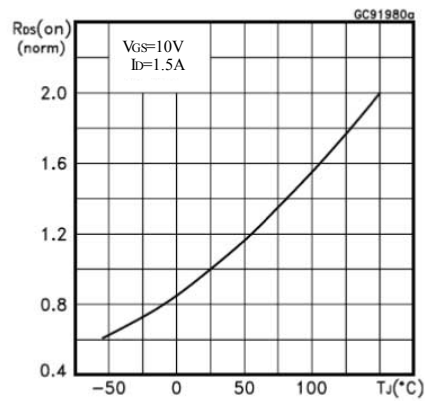


Figure 10. Source-drain diode forward characteristics

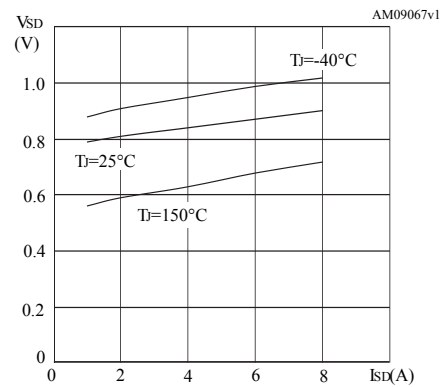
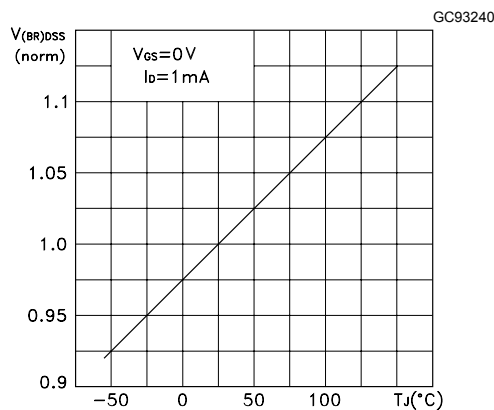
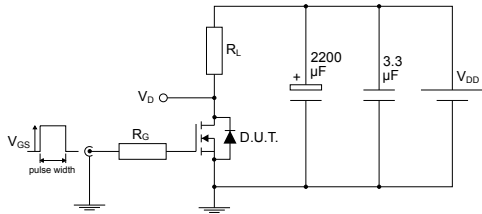


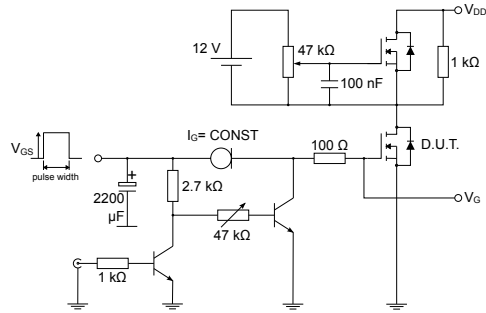
Figure 11. Normalized breakdown voltage vs temperature



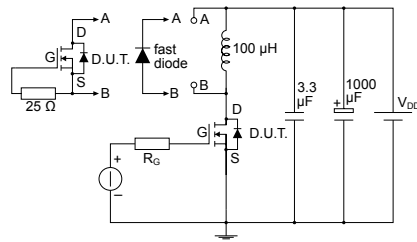
3 Test circuits

Figure 12. Test circuit for resistive load switching times


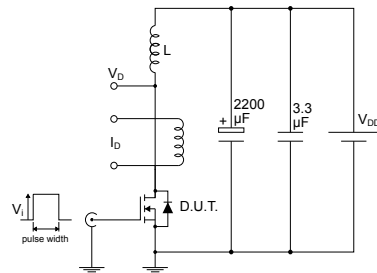
AM01468v1

Figure 13. Test circuit for gate charge behavior


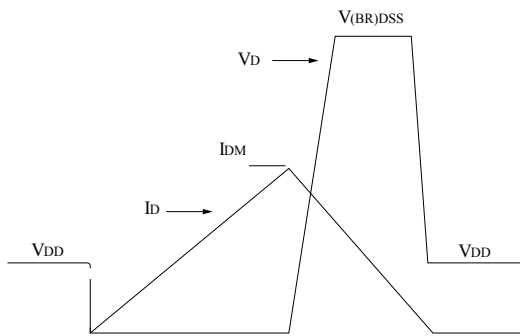
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Figure 14. Test circuit for inductive load switching and diode recovery times


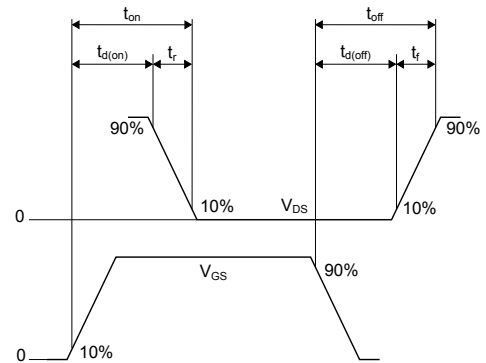
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Figure 15. Unclamped inductive load test circuit


AM01471v1

Figure 16. Unclamped inductive waveform


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Figure 17. Switching time waveform


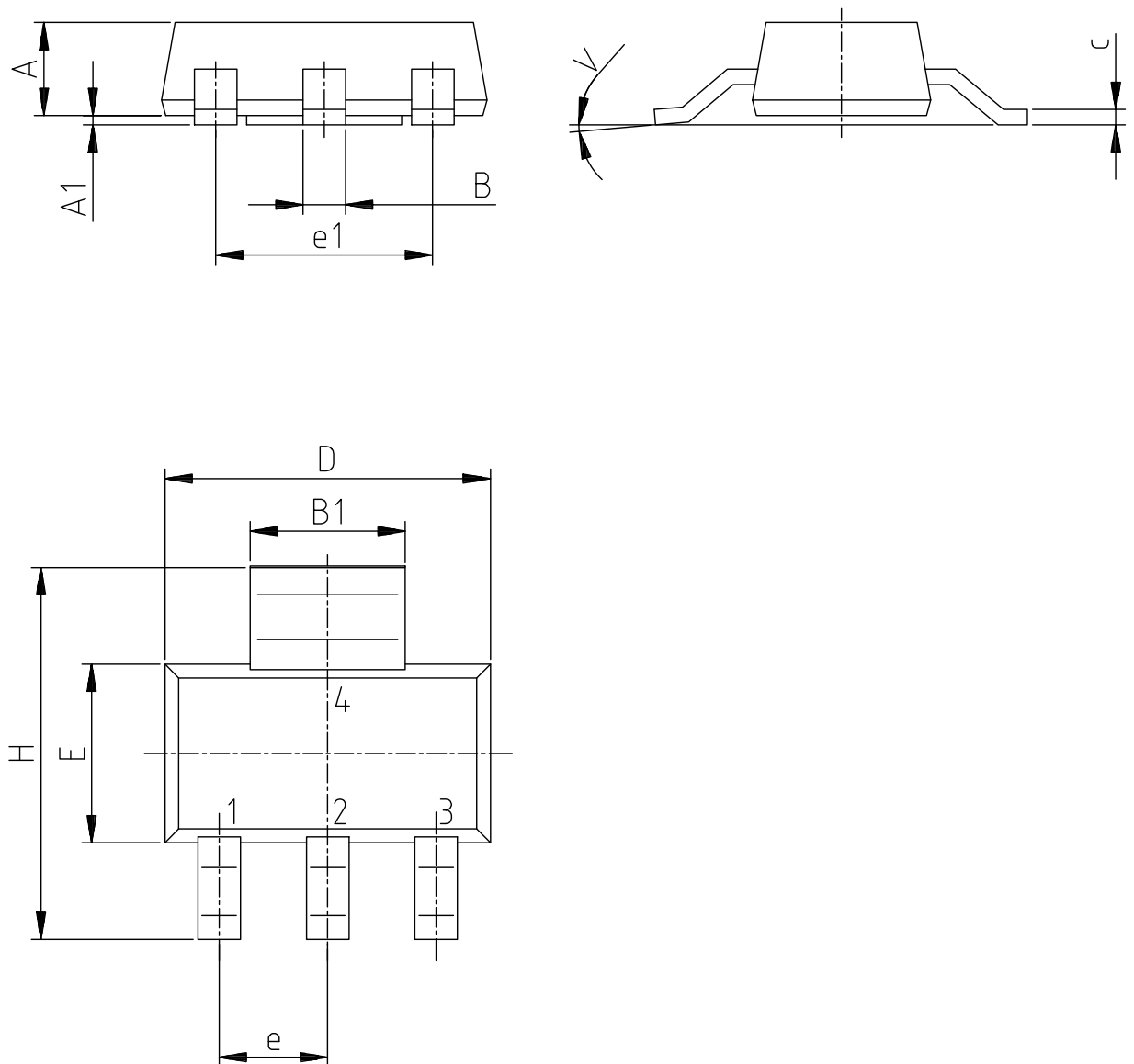
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SOT-223 package information

Figure 18. SOT-223 package outline

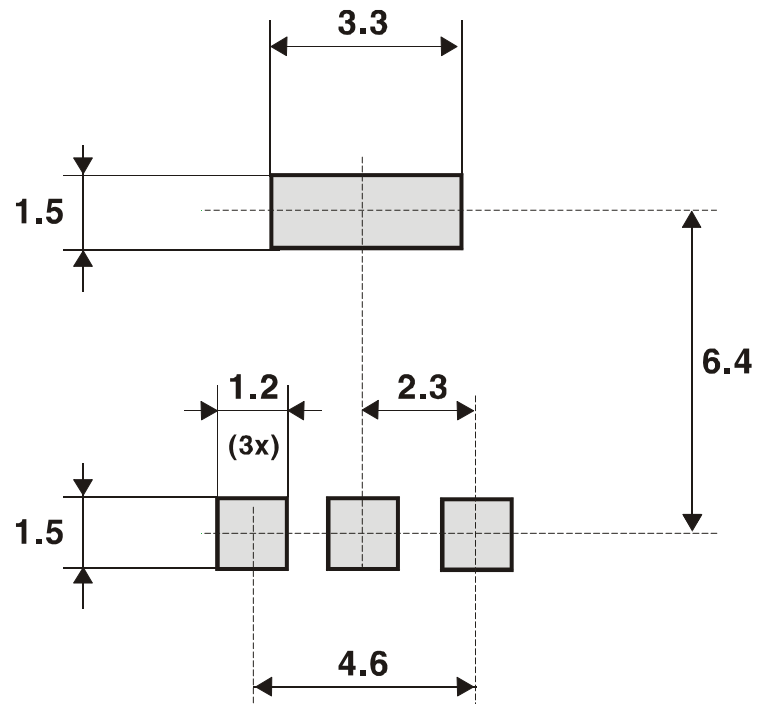


0046067_15

Table 7. SOT-223 package mechanical data

| Dim. | mm | | |
|------|------|------|--------|
| | Min. | Typ. | Max. |
| A | | | 1.8 |
| B | 0.6 | 0.7 | 0.85 |
| B1 | 2.9 | 3 | 3.15 |
| c | 0.24 | 0.26 | 0.35 |
| D | 6.3 | 6.5 | 6.7 |
| e | | 2.3 | |
| e1 | | 4.6 | |
| E | 3.3 | 3.5 | 3.7 |
| H | 6.7 | 7 | 7.3 |
| V | | | 10 deg |
| A1 | 0.02 | | 0.1 |

Figure 19. SOT-223 recommended footprint (dimensions are in mm)



0046067

Table 8. SOT-223 tape and reel mechanical data

| Tape | | | | Tape | | |
|------|------|------|------|-------------------|------|------|
| Dim. | mm | | | Dim. | mm | |
| | Min. | Typ. | Max. | | Min. | Max. |
| A0 | 6.75 | 6.85 | 6.95 | A | | 180 |
| B0 | 7.30 | 7.40 | 7.50 | N | 60 | |
| K0 | 1.80 | 1.90 | 2.00 | W1 | | 12.4 |
| F | 5.40 | 5.50 | 5.60 | W2 | | 18.4 |
| E | 1.65 | 1.75 | 1.85 | W3 | 11.9 | 15.4 |
| W | 11.7 | 12.0 | 12.3 | | | |
| P2 | 1.90 | 2.00 | 2.10 | Base quantity pcs | | 1000 |
| P0 | 3.90 | 4.00 | 4.10 | Bulk quantity pcs | | 1000 |
| P1 | 7.90 | 8.00 | 8.10 | | | |
| T | 0.25 | 0.30 | 0.35 | | | |
| DΦ | 1.50 | 1.55 | 1.60 | | | |
| D1Φ | 1.50 | 1.60 | 1.70 | | | |

Revision history

Table 9. Document revision history

| Date | Version | Changes |
|-------------|---------|---|
| 22-Apr-2008 | 1 | Initial version. |
| 29-Apr-2011 | 2 | <i>Figure 5, Figure 7, Figure 11 and Figure 12</i> have been updated. |
| 05-May-2020 | 3 | Updated Section 4.1 SOT-223 package information. Minor text changes. |

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