

MC14099B

8-Bit Addressable Latches

The MC14099B is an 8-bit addressable latch. Data is entered in serial form when the appropriate latch is addressed (via address pins A0, A1, A2) and write disable is in the low state. For the MC14099B the input is a unidirectional write only port.

The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/Read or Chip Enable.

A Master Reset capability is available on both parts.

- Serial Data Input
- Parallel Output
- Master Reset
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- MC14099B pin for pin compatible with CD4099B

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

| Symbol | Parameter | Value | Unit |
|-------------------|---|------------------------|-------------|
| V_{DD} | DC Supply Voltage Range | -0.5 to +18.0 | V |
| V_{in}, V_{out} | Input or Output Voltage Range (DC or Transient) | -0.5 to $V_{DD} + 0.5$ | V |
| I_{in}, I_{out} | Input or Output Current (DC or Transient) per Pin | ± 10 | mA |
| P_D | Power Dissipation, per Package (Note 3.) | 500 | mW |
| T_A | Ambient Temperature Range | -55 to +125 | $^{\circ}C$ |
| T_{stg} | Storage Temperature Range | -65 to +150 | $^{\circ}C$ |
| T_L | Lead Temperature (8-Second Soldering) | 260 | $^{\circ}C$ |

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:
Plastic "P and D/DW" Packages: -7.0 mW/ $^{\circ}C$ From 65 $^{\circ}C$ To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

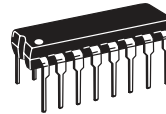
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



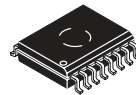
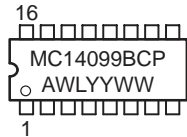
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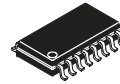
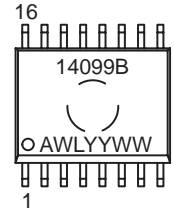
MARKING DIAGRAMS



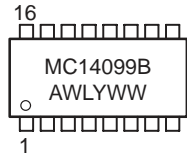
PDIP-16
P SUFFIX
CASE 648



SOIC-16
DW SUFFIX
CASE 751G



SOEIAJ-16
F SUFFIX
CASE 966



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

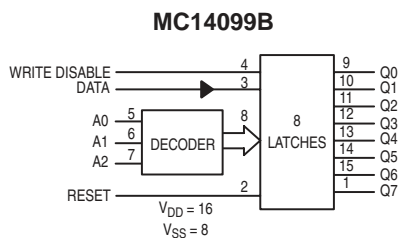
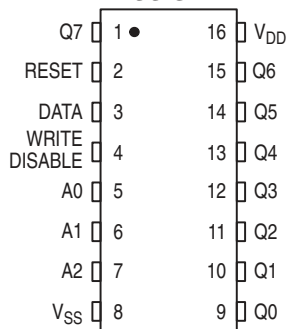
ORDERING INFORMATION

| Device | Package | Shipping |
|--------------|-----------|------------------|
| MC14099BCP | PDIP-16 | 2000/Box |
| MC14099BDW | SOIC-16 | 2350/Box |
| MC14099BDWR2 | SOIC-16 | 1000/Tape & Reel |
| MC14099BF | SOEIAJ-16 | See Note 1. |
| MC14099BFEL | SOEIAJ-16 | See Note 1. |

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

MC14099B

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V _{DD} Vdc | -55°C | | 25°C | | | 125°C | | Unit |
|---|---|------------------------|---|------|-------|--------------------|------|-------|------|------|
| | | | Min | Max | Min | Typ ⁽⁴⁾ | Max | Min | Max | |
| Output Voltage V _{in} = V _{DD} or 0 | "0" Level V _{OL} | 5.0 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | Vdc |
| | | 10 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | |
| V _{in} = 0 or V _{DD} | "1" Level V _{OH} | 5.0 | 4.95 | — | 4.95 | 5.0 | — | 4.95 | — | Vdc |
| | | 10 | 9.95 | — | 9.95 | 10 | — | 9.95 | — | |
| Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) | "0" Level V _{IL} | 5.0 | — | 1.5 | — | 2.25 | 1.5 | — | 1.5 | Vdc |
| | | 10 | — | 3.0 | — | 4.50 | 3.0 | — | 3.0 | |
| (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc) | "1" Level V _{IH} | 5.0 | 3.5 | — | 3.5 | 2.75 | — | 3.5 | — | Vdc |
| | | 10 | 7.0 | — | 7.0 | 5.50 | — | 7.0 | — | |
| Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) | Source I _{OH} | 5.0 | -3.0 | — | -2.4 | -4.2 | — | -1.7 | — | mAdc |
| | | 10 | -0.64 | — | -0.51 | -0.88 | — | -0.36 | — | |
| (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc) | Sink I _{OL} | 5.0 | 0.64 | — | 0.51 | 0.88 | — | 0.36 | — | mAdc |
| | | 10 | 1.6 | — | 1.3 | 2.25 | — | 0.9 | — | |
| | | 15 | 4.2 | — | 3.4 | 8.8 | — | 2.4 | — | |
| Input Current | I _{in} | 15 | — | ±0.1 | — | ±0.00001 | ±0.1 | — | ±1.0 | μAdc |
| Input Capacitance (V _{in} = 0) | C _{in} | — | — | — | — | 5.0 | 7.5 | — | — | pF |
| Input Capacitance MC14599B — Data (pin 3) (V _{in} = 0) | C _{in} | — | — | — | — | 15 | 22.5 | — | — | pF |
| Quiescent Current (Per Package) | I _{DD} | 5.0 | — | 5.0 | — | 0.005 | 5.0 | — | 150 | μAdc |
| | | 10 | — | 10 | — | 0.010 | 10 | — | 300 | |
| | | 15 | — | 20 | — | 0.015 | 20 | — | 600 | |
| Total Supply Current ⁽⁵⁾ ⁽⁶⁾ (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching) | I _T | 5.0 | I _T = (1.5 μA/kHz) f + I _{DD} | | | | | | | μAdc |
| 10 | I _T = (3.0 μA/kHz) f + I _{DD} | | | | | | | | | |
| 15 | I _T = (4.5 μA/kHz) f + I _{DD} | | | | | | | | | |

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

MC14099B

SWITCHING CHARACTERISTICS (7.) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

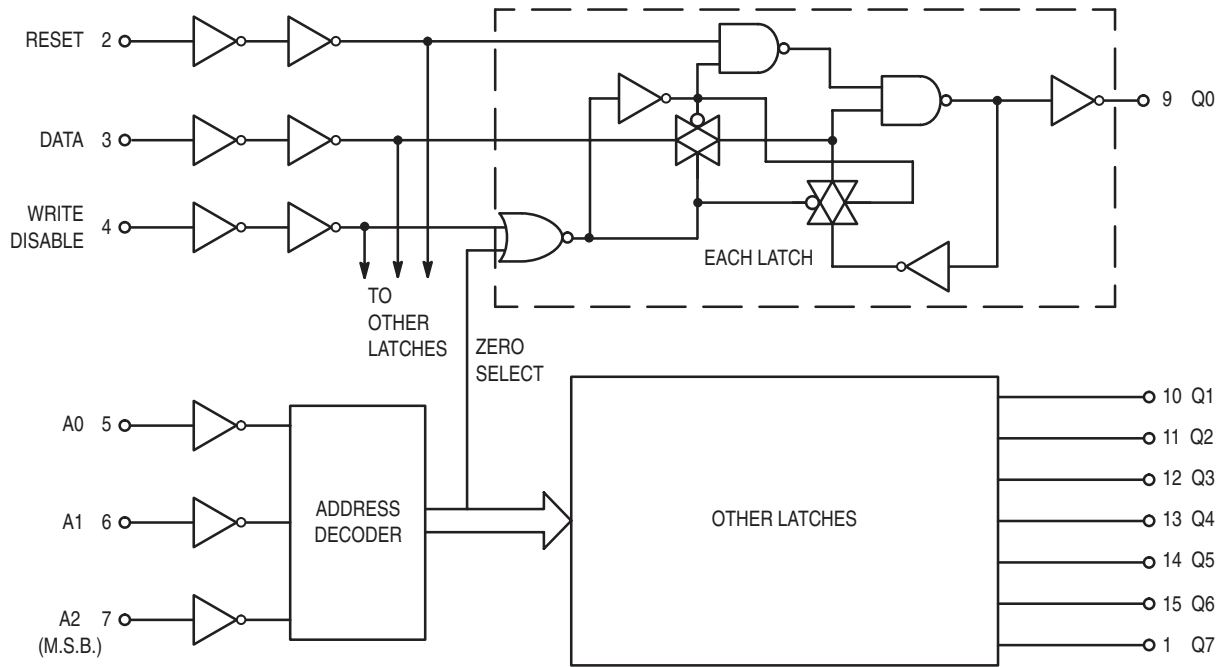
| Characteristic | Symbol | V_{DD} Vdc | Min | Typ (8.) | Max | Unit |
|---|--------------------------|-----------------|-------------------|----------------------|-------------------|------|
| Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.35 \text{ ns/pF}) C_L + 32 \text{ ns}$ t_{TLH} , $t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$ t_{TLH} , $t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$ | t_{TLH} , t_{THL} | 5.0 10 15 | — — — | 100 50 40 | 200 100 80 | ns |
| Propagation Delay Time Data to Output Q | t_{PHL} , t_{PLH} | 5.0 10 15 | — — — | 200 75 50 | 400 150 100 | ns |
| Write Disable to Output Q | | 5.0 10 15 | — — — | 200 80 60 | 400 160 120 | ns |
| Reset to Output Q | | 5.0 10 15 | — — — | 175 80 65 | 350 160 130 | ns |
| CE to Output Q (MC14599B only) | | 5.0 10 15 | — — — | 225 100 75 | 450 200 150 | ns |
| Propagation Delay Time, MC14599B only Chip Enable, Write/Read to Data | t_{PHL} , t_{PLH} | 5.0 10 15 | — — — | 200 80 65 | 400 160 130 | ns |
| Address to Data | | 5.0 10 15 | — — — | 200 90 75 | 400 180 150 | ns |
| Pulse Widths Reset | $t_{w(H)}$ $t_{w(L)}$ | 5.0 10 15 | 150 75 50 | 75 40 25 | — — — | ns |
| Write Disable | | 5.0 10 15 | 320 160 120 | 160 80 60 | — — — | ns |
| Set Up Time Data to Write Disable | t_{su} | 5.0 10 15 | 100 50 35 | 50 25 20 | — — — | ns |
| Hold Time Write Disable to Data | t_h | 5.0 10 15 | 150 75 50 | 75 40 25 | — — — | ns |
| Set Up Time Address to Write Disable | t_{su} | 5.0 10 15 | 100 80 40 | 45 30 10 | — — — | ns |
| Removal Time Write Disable to Address | t_{rem} | 5.0 10 15 | 0 0 0 | - 80 - 40 - 40 | — — — | ns |

7. The formulas given are for the typical characteristics only at 25°C .

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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MC14099B FUNCTION DIAGRAM



TRUTH TABLE

| Write Disable | Reset | Addressed Latch | Unaddressed Latches |
|---------------|-------|-----------------|---------------------|
| 0 | 0 | Data | Q_n^* |
| 0 | 1 | Data | Reset † |
| 1 | 0 | Q_n^* | Q_n^* |
| 1 | 1 | Reset | Reset |

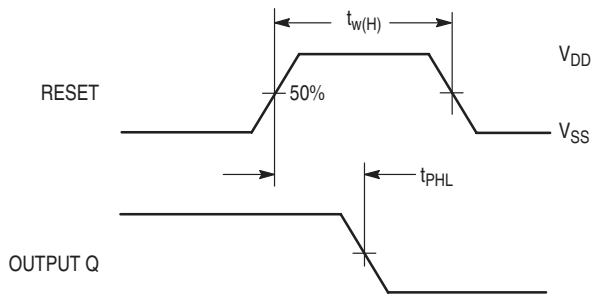
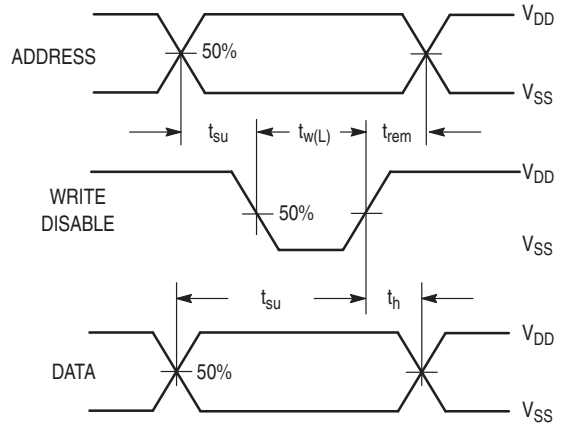
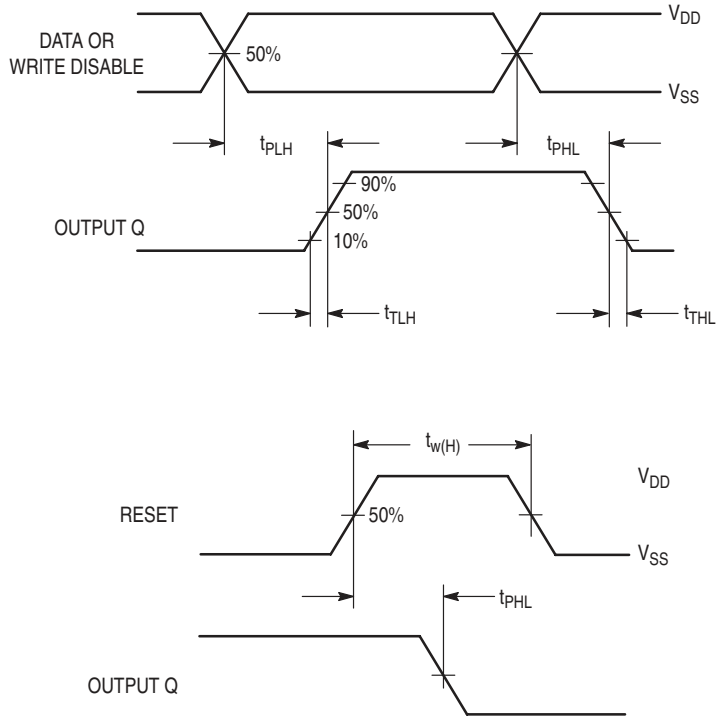
* Q_n is previous state of latch.

†Reset to zero state.

CAUTION: To avoid unintentional data changes in the latches, Write Disable must be active (high) during transitions on the address inputs A0, A1, and A2.

MC14099B

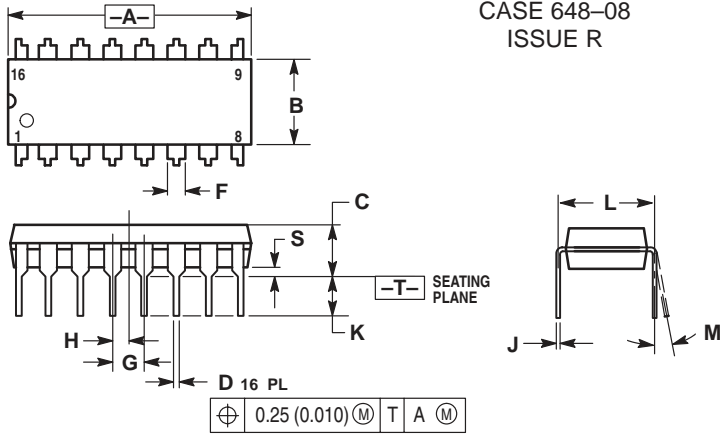
SWITCHING WAVEFORMS



MC14099B

PACKAGE DIMENSIONS

PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R

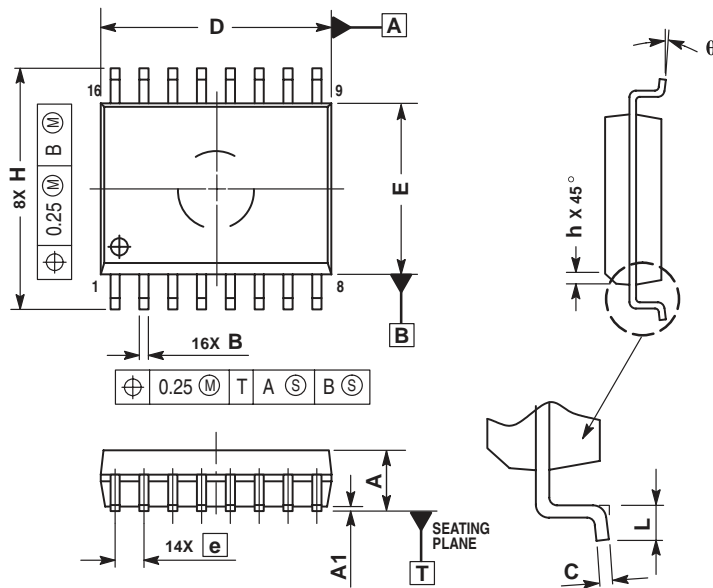


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

SOIC-16 DW SUFFIX PLASTIC SOIC PACKAGE CASE 751G-03 ISSUE B



NOTES:

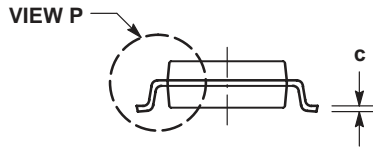
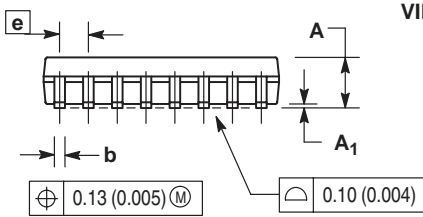
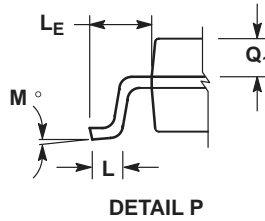
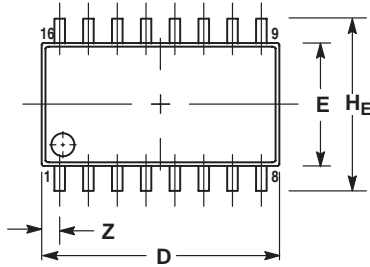
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 10.15 | 10.45 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

MC14099B

PACKAGE DIMENSIONS


SOEIAJ-16 F SUFFIX PLASTIC EIAJ SOIC PACKAGE CASE 966-01 ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | — | 2.05 | — | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.18 | 0.27 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| H _E | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| L _E | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | — | 0.78 | — | 0.031 |

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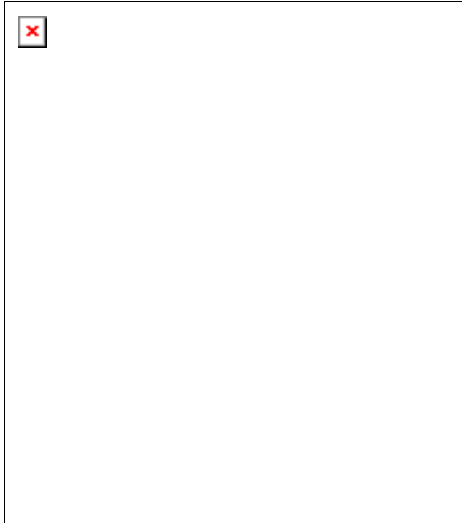
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Device MC14099B
8-Bit Addressable Latches

The MC14099B and MC14599B are 8-bit addressable latches. Data is entered in s appropriate latch is addressed (via address pins A0, A1, A2) and write disable is in must be high for writing into MC14599B. For the MC14599B the data pin is a bidire MC14099B the input is a unidirectional write only port. The Write/Read line control:

The data is presented in parallel at the output of the eight latches independently of Write/Read or Chip Enable.

A Master Reset capability is available on both parts.

Features:

- Serial Data Input
- Parallel Output
- Master Reset
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- MC14099B pin for pin compatible with CD4099B

Orderable Parts



Orderable Parts

| Action | Orderable Part | Short Desc. | Package Desc. | Pin Count | Case Outline | Status |
|---------------|-----------------------|---------------------|----------------------|------------------|-------------------------|---------------|
| N/A | MC14099BDW | 8-Bit Address Latch | SOIC | 16 | 751G-03 | Active |
| N/A | MC14099BDWR2 | Tape and Reel | SOIC | 16 | 751G-03 | Active |
| N/A | MC14099BF | 8-Bit Address Latch | MFP | 16 | 966-01 | Active |
| N/A | MC14099BFEL | Tape and Reel | MFP | 16 | 966-01 | Active |
| N/A | MC14099BFL1 | Tape and Reel | MFP | 16 | 966-01 | LifeTime |
| N/A | MC14099BCP | 8-Bit Address Latch | PDIP | 16 | 648-08 | Active |

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