MIC37300/01/02/03

3.0A, Low Voltage µCap LDO Regulator

Features

- 3A Minimum Output Current
- 500 mV Maximum Dropout Voltage over Temperature
  - Recommended for 3.0V to 2.5V Conversion
  - Recommended for 2.5V to 1.8V, 1.65V, or 1.5V Conversion
- Stable with Ceramic or Tantalum Capacitors
- Wide Input Voltage Range
  - V_{IN}: 2.25V to 6.0V
- +1.0% Initial Output Tolerance
- Fixed and Adjustable Output Voltages:
  - MIC37300: 3-pin S-PAK Fixed Voltages
  - MIC37301: 5-pin S-PAK or 8-pin ePad SOIC Fixed Voltages with Flag
  - MIC37302: 5-pin Adjustable Voltage
  - MIC37303: 8-pin ePad SOIC, DFN Adjustable Voltage with Flag
- Excellent Line and Load Regulation Specifications
- Thermal Shutdown and Current Limit Protection
- Reverse-Leakage Protection
- Low Profile S-PAK Package

Applications

- LDO Linear Regulator for Low Voltage Digital IC
- PC Add-In Cards
- PowerPC Power Supplies
- High Efficiency Linear Power Supplies
- SMPS Post Regulator
- Multimedia and PC Processor Supplies
- Battery Chargers
- Low Voltage Microcontrollers and Digital Logic

General Description

The MIC37300/01/02/03 is a 3.0A low-dropout linear voltage regulator that provides a low voltage, high current output with a minimum number of external components. It offers high precision, ultra-low dropout (500 mV over temperature), and low ground current.

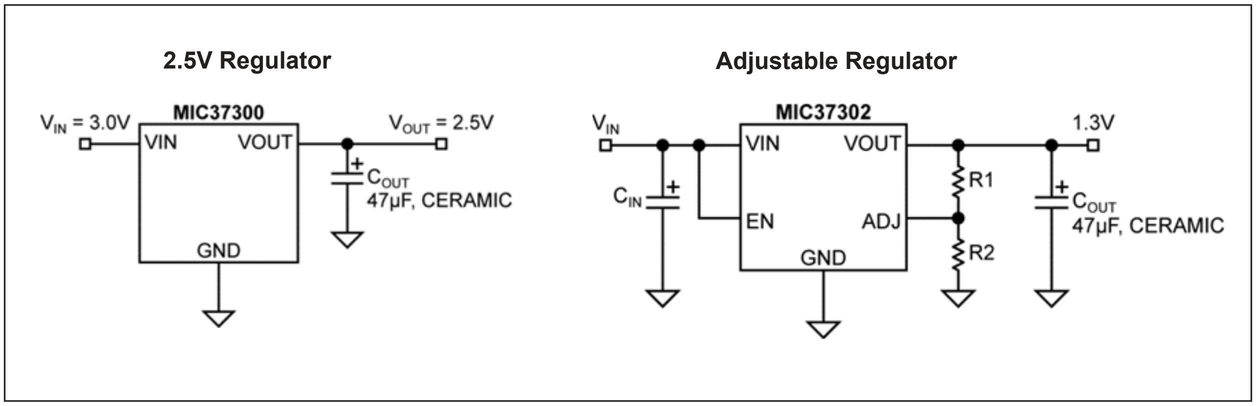
The MIC37300/01/02/03 operates from an input of 2.25V to 6.0V. It is designed to drive digital circuits requiring low-voltage at high currents (i.e., PLDs, DSP, microcontroller, etc.). It is available in fixed and adjustable output voltages. Fixed voltages include 1.5V, 1.8V, 2.5V, and 3.3V. The adjustable version is capable of 1.24V to 5.5V.

Features of the MIC37300/01/02/03 LDO include thermal and current limit protection, and reverse current protection. Logic enable and error flag pins are available on the 5-pin version.

Junction temperature range of the MIC37300/01/02/03 is from –40°C to +125°C.

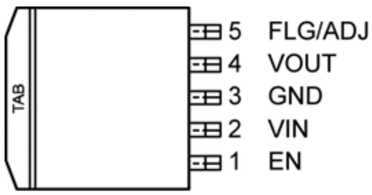
For applications requiring input voltage greater than 6.0V, see the MIC3910x, MIC3915x, MIC3930x, and MIC3950x LDOs.

Typical Application Circuits

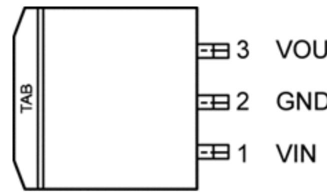


Package Types

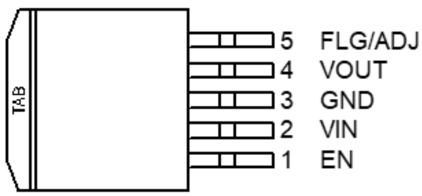
S-PAK-5 (R)
(Top View)



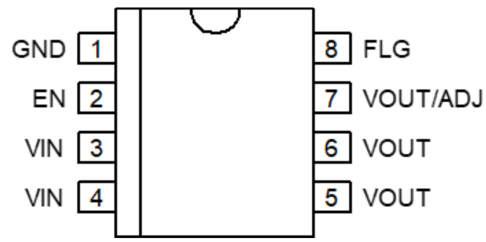
S-PAK-3 (R)
(Top View)



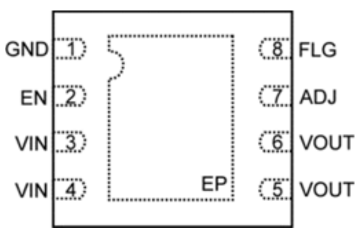
TO-263-5 (U)
(Top View)



ePad SOIC-8 (ME)
(Top View)



3 mm x 3 mm (DFN)
(Top View)



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{IN}) .... +6.5V
Enable Input Voltage (V_{EN}) .... +6.5V
Power Dissipation (P_D) (Note 1) .... Internally Limited
Junction Temperature (T_J) .... –40°C ≤ T_J ≤ +125°C
Storage Temperature (T_S) .... –65°C ≤ T_J ≤ +150°C
Lead Temperature (Soldering, 10s) .... 260°C
ESD Rating (Note 2) .... 2 kV

Operating Ratings ‡

Supply Voltage (V_{IN}) .... +2.25V to +6.0V
Enable Voltage (V_{EN}) .... 0V to +6.0V
Junction Temperature (T_J) .... –40°C ≤ T_J ≤ +125°C
Package Thermal Resistance
S-PAK (θ_{JA}) .... 5.5°C/W
TO-263-5 (θ_{JC}) .... 6.3°C/W
ePad SOIC-8 (θ_{JC}) .... 16°C/W
3 mm x 3 mm DFN (θ_{JC}) .... 29°C/W

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. Specifications are for packaged product only.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: $P_{D(max)} = (T_{J(max)} – T_A) \div \theta_{JA}$, where θ_{JA} depends upon the printed circuit layout. See “**Section 4.0 “Application Information”** section.

2: Devices are ESD sensitive. Handling precautions are recommended.

ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: $V_{IN} = V_{OUT}$ + 1V; $V_{EN} = V_{IN}$; I_L = 10 mA; T_A = 25°C, **Bold** values indicate –40°C < T_J < +125°C; unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Voltage Accuracy	V_{OUT}	–1	—	+1	%	I_L = 10 mA
		–2	—	**+2**	%	10 mA ≤ I_{OUT} ≤ $I_{L(MAX)}$, V_{OUT} + 1V ≤ V_{IN} ≤ 6V
Output Voltage Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	—	0.02	0.5	%	$V_{IN} = V_{OUT}$ + 1.0V to 6.0V; I_L = 10 mA
Output Voltage Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.2	**1**	%	I_L = 10 mA to 3A
V_{IN} - V_{OUT} Dropout Voltage (Note 2), (Note 5)	V_{DO}	—	175	**350**	mV	I_L = 1.5A (For S-PAK-5, TO-263-5)
		—		**400**		I_L = 1.5A (For e-Pad SOIC-8, DFN)
		—	300	**500**	mV	I_L = 3.0A (For S-PAK-5, TO-263-5)
		—		**550**		I_L = 3.0A (For e-Pad SOIC-8, DFN)
Ground Pin Current (Note 3)	I_{GND}	—	27	40 **50**	mA	I_L = 3A
Ground Pin Current In Shutdown	$I_{GND-SHDN}$	—	1.0	5	µA	V_{IL} ≤ 0.5V, $V_{IN} = V_{OUT}$ +1V
Current Limit	I_{LIM}	—	4.75	**6.5**	A	V_{OUT} = 0V
Start-Up Time	t_{START}	—	170	**500**	µs	$V_{EN} = V_{IN}$, I_{OUT} = 10 mA, C_{OUT} = 47 µF

ELECTRICAL CHARACTERISTICS (Note 1) (CONTINUED)

Electrical Characteristics: $V_{IN} = V_{OUT} + 1V$; $V_{EN} = V_{IN}$; $I_L = 10$ mA; $T_A = 25°C$, **Bold** values indicate –40°C < T_J < +125°C; unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Enable Input						
Enable Input Threshold	V_{EN}	**2.25**	—	—	V	Regulator Enable
		—	—	**0.8**		Regulator Shutdown
Enable Pin Input Current	I_{EN}	—	—	2 **4**	µA	$V_{IL} \leq 0.8V$ (Regulator Shutdown)
		1	15	30 **75**	µA	$V_{IH} \geq 2.25V$ (Regulator Enable)
Flag Output						
Output Leakage Current	$I_{FLG(LEAK)}$	—	—	1	µA	$V_{OH} = 6V$
		—	—	**2**		
Output Low Voltage (Note 4)	$V_{FLG(LO)}$	—	210	400 **500**	mV	$V_{IN} = 2.25V$, $I_{OL} = 250$ µA
Low Threshold	V_{FLG}	93	—	**—**	%	% of V_{OUT} Below Nominal
High Threshold		—	—	99.2		% of V_{OUT} Below Nominal
Hysteresis		—	2	**—**		—
MIC37302 Only						
Reference Voltage	V_{REF}	1.228	1.240	1.252	V	—
		1.215		**1.265**		
Adjust Pin Bias Current	I_{ADJ}	—	40	80	nA	—
				120		

1: Specification for packaged product only.

2: $V_{DO} = V_{IN} – V_{OUT}$ when V_{OUT} decreases to 98% of its nominal output voltage with $V_{IN} = V_{OUT} + 1V$. For output voltages below 1.75V, dropout voltage specification does not apply due to a minimum input operating voltage of 2.25V.

3: I_{GND} is the ground current. $I_{IN} = I_{GND} + I_{OUT}$.

4: For a 2.5V device, $V_{IN} = 2.250V$ (device is in dropout).

5: Limits specified down to:

$V_{IN} = 2.25V$ for $0°C \leq T_A \leq +125°C$
$V_{IN} = 2.35V$ for $0°C > T_A \geq –40°C$

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Lead Temperature	—	—	—	260	°C	(soldering, 10 sec.)
Junction Temperature	T_J	–40	—	+125	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistances						
Thermal Resistance SPAK-5	θ_{JC}	—	5.5	—	°C/W	—
Thermal Resistance TO-263-5	θ_{JC}	—	6.3	—	°C/W	—
Thermal Resistance ePad SOIC-8	θ_{JC}	—	16	—	°C/W	—
Thermal Resistance 3 mm x 3 mm DFN	θ_{JC}	—	29	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

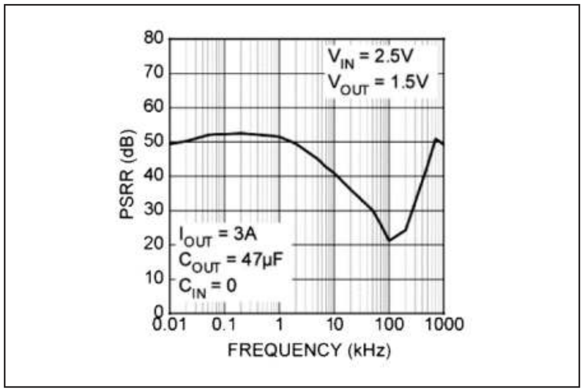


FIGURE 2-1: *Power Supply Rejection Ratio.*

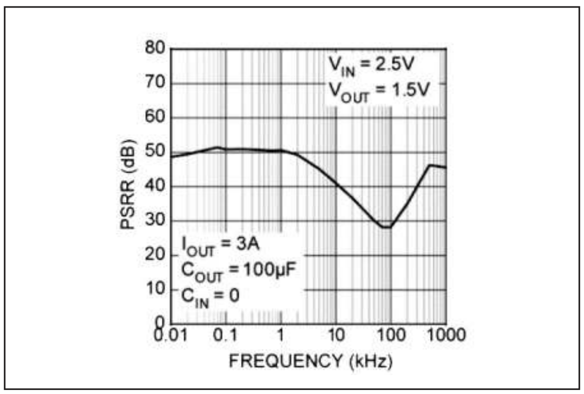


FIGURE 2-2: *Power Supply Rejection Ratio.*

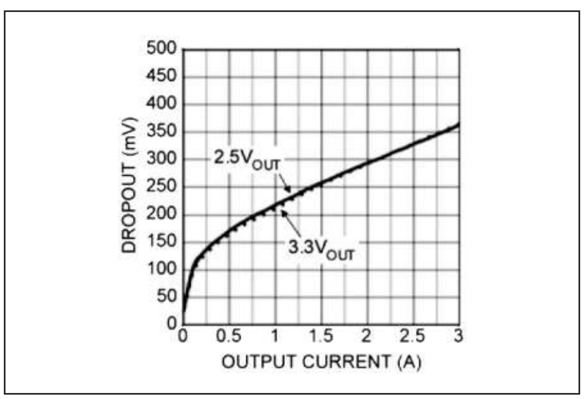


FIGURE 2-3: *Dropout vs. Output Current.*

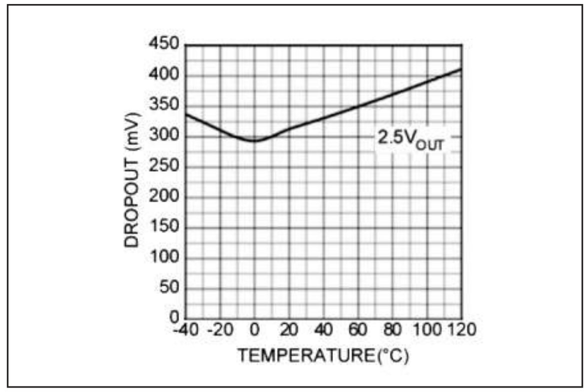


FIGURE 2-4: *Dropout vs. Temperature.*

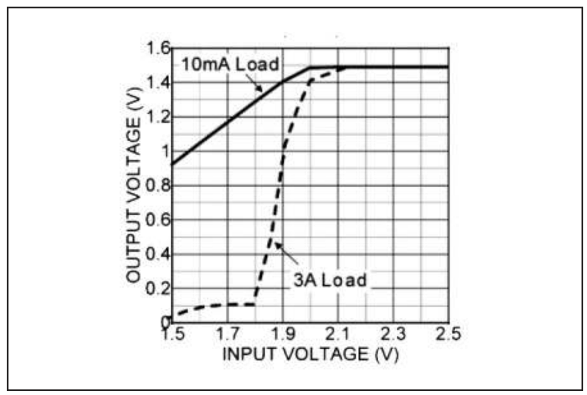


FIGURE 2-5: *Dropout Characteristics (1.5V).*

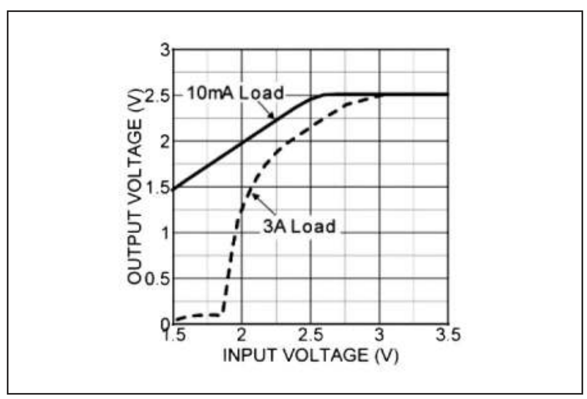


FIGURE 2-6: *Dropout Characteristics (2.5V).*

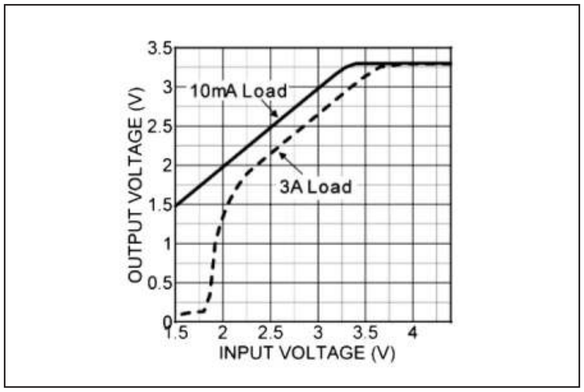


FIGURE 2-7: *Dropout Characteristics (3.3V).*

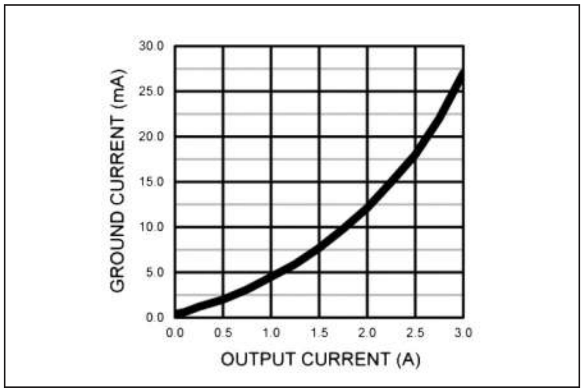


FIGURE 2-8: *Ground Current vs. Output Current.*

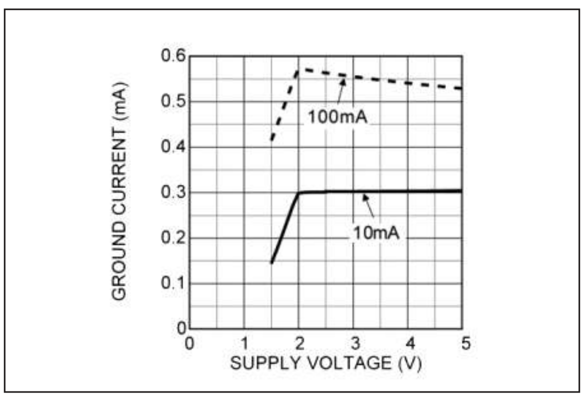


FIGURE 2-9: *Ground Current vs. Supply Voltage (1.5V).*

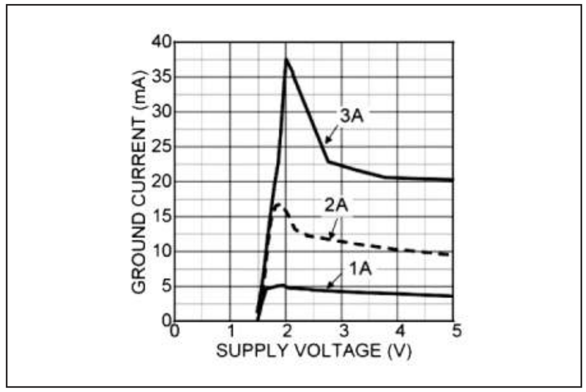


FIGURE 2-10: *Ground Current vs. Supply Voltage (1.5V).*

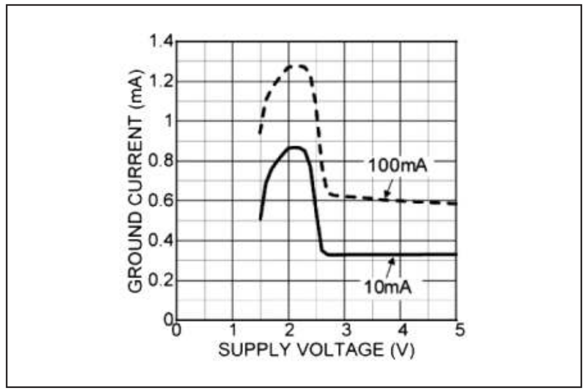


FIGURE 2-11: *Ground Current vs. Supply Voltage (2.5V).*

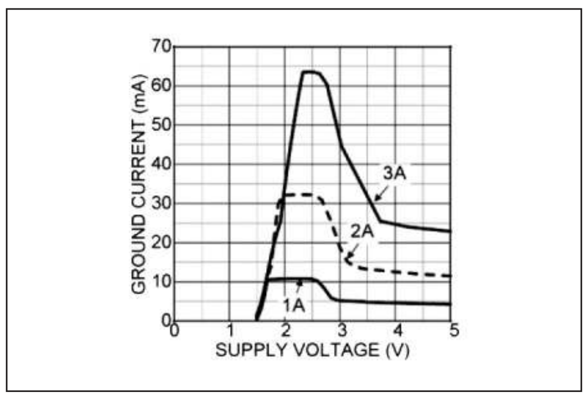


FIGURE 2-12: *Ground Current vs. Supply Voltage (2.5V).*

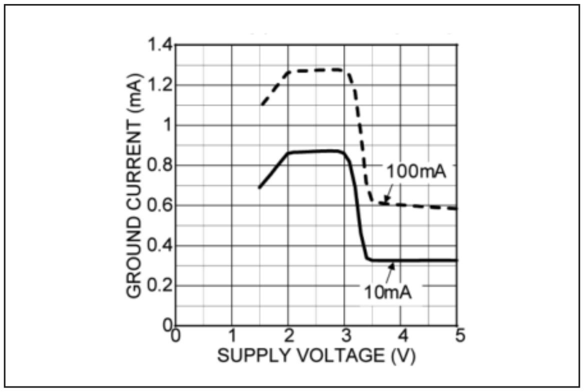


FIGURE 2-13: *Ground Current vs. Supply Voltage (3.3V).*

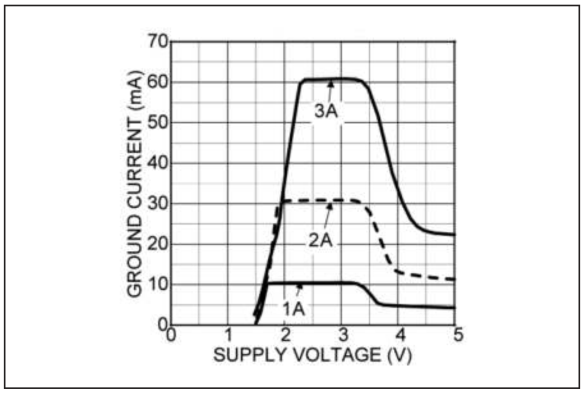


FIGURE 2-14: *Ground Current vs. Supply Voltage (3.3V).*

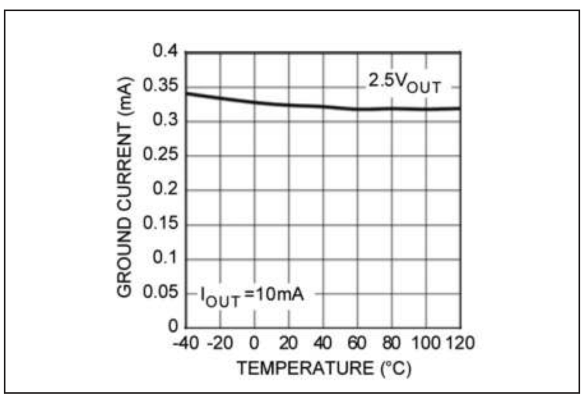


FIGURE 2-15: *Ground Current vs. Temperature.*

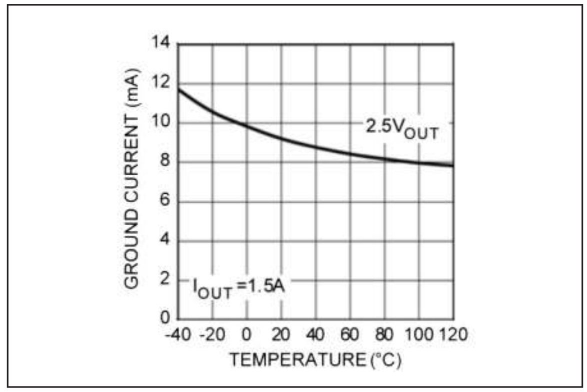


FIGURE 2-16: *Ground Current vs. Temperature.*

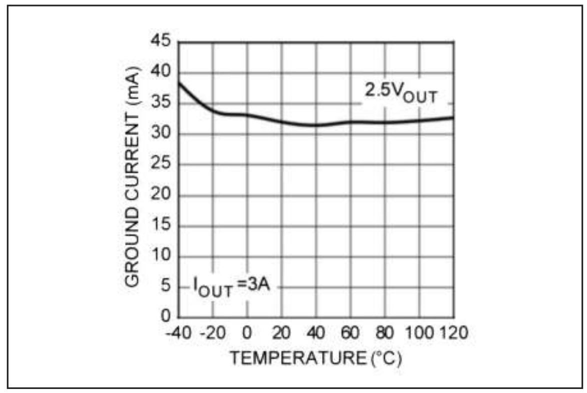


FIGURE 2-17: *Ground Current vs. Temperature.*

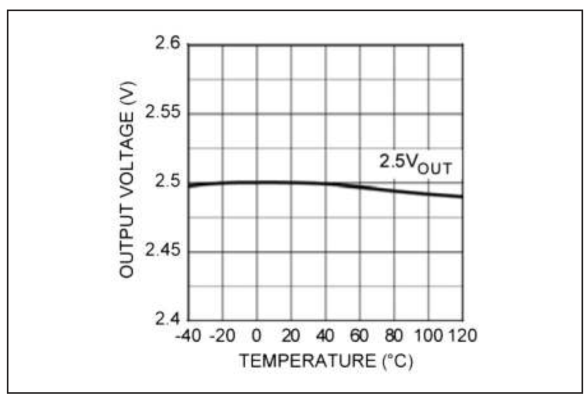


FIGURE 2-18: *Output Voltage vs. Temperature.*

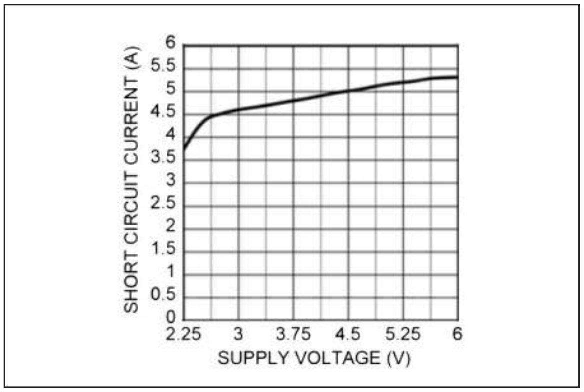


FIGURE 2-19: *Short-Circuit Current vs. Supply Voltage.*

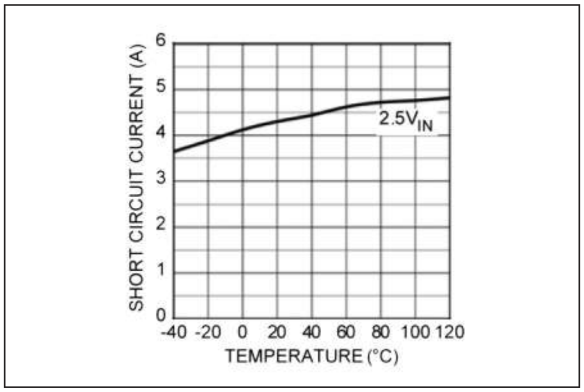


FIGURE 2-20: *Short-Circuit Current vs. Temperature.*

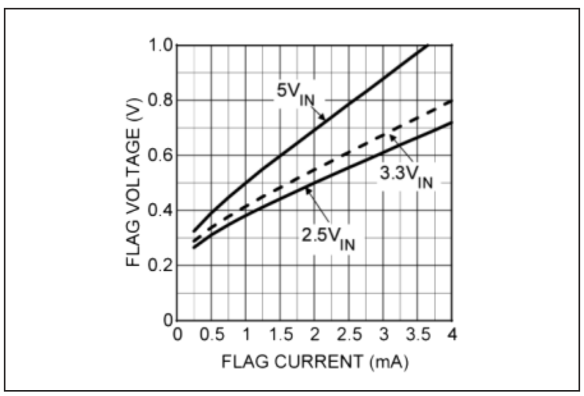


FIGURE 2-21: *Flag Voltage vs. Flag Current.*

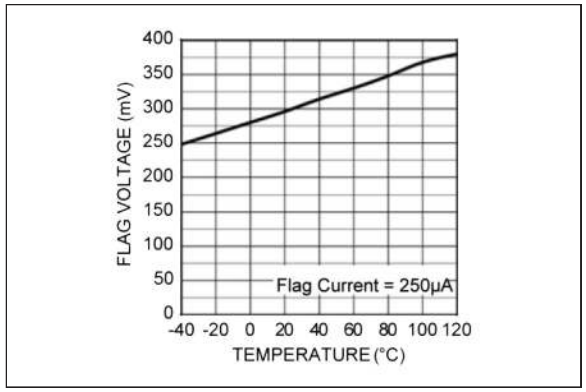


FIGURE 2-22: *Flag Low-Voltage vs. Temperature.*

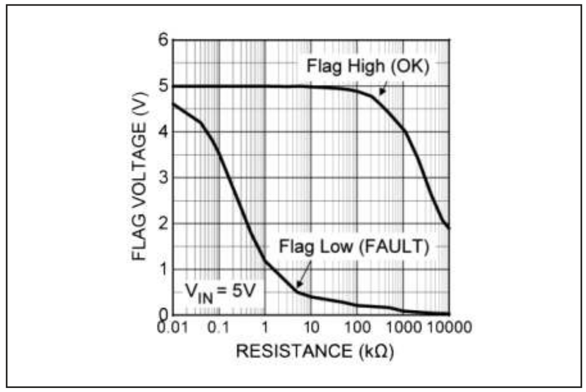


FIGURE 2-23: *Error Flag Pull-Up Resistor.*

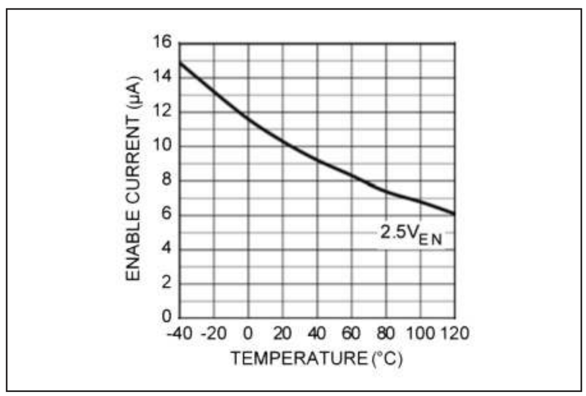


FIGURE 2-24: *Enable Current vs. Temperature.*

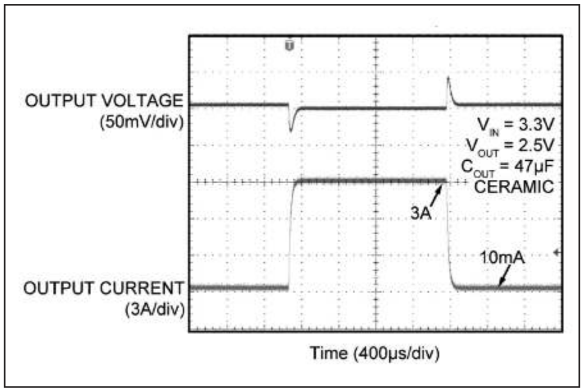


FIGURE 2-25: *Load Transient Response.*

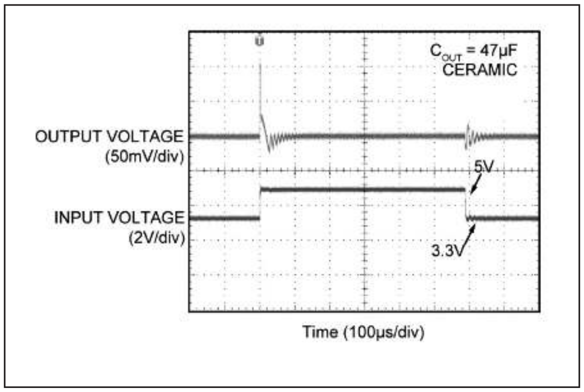


FIGURE 2-26: *Line Transient Response.*

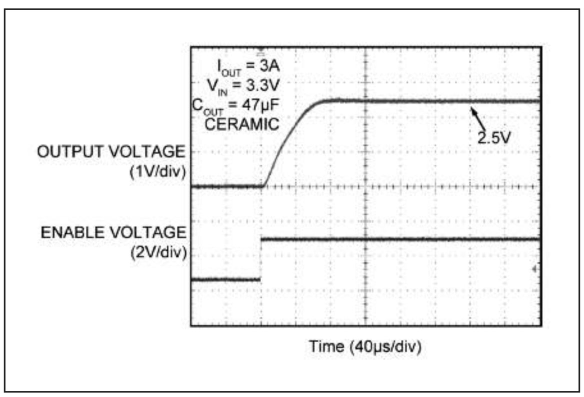


FIGURE 2-27: *Enable Transient Response.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

S-PAK-5 TO-263-5	S-PAK-3	ePAD SOIC-8 DFN	Pin Name	Description
1	—	2	EN	Enable (Input): CMOS compatible control input. Logic high = enable, Logic low = shutdown. Do not leave floating.
2	1	3, 4	VIN	Input voltage that supplies current to the output power device.
3	2	1	GND	Ground: TAB is connected to ground.
4	3	5, 6, 7 (Fixed) 5, 6, (Adj.)	VOUT	Regulator output.
5 (Fixed)	—	8	FLG	Flag (Output): Open collector output. Active LOW indicates an output fault condition.
5 (Adj)	—	7 (Adj.)	ADJ	Adjustable regulator feedback input: Connect to resistor voltage driver.
—	—	EP	ePad	Connect to GND for best thermal performance.

4.0 APPLICATION INFORMATION

The MIC37300/01/02/03 is a high-performance low dropout voltage regulator suitable for moderate to high current regulator applications. The 500 mV dropout voltage at full load and over temperature makes it especially valuable in battery-powered systems and as high-efficiency noise filters in post regulator applications. Unlike older NPN-pass transistor designs, where the minimum dropout voltage is limited by the based-to-emitter voltage drop and collector-to-emitter saturation voltage, dropout performance of the PNP output of these devices is limited only by the low V_{CE} saturation voltage.

A trade-off for the low dropout voltage is a varying base drive requirement. Microchip's Super βeta PNP process reduces this drive requirement to only 2% to 5% of the load current.

The MIC37100/01/02 regulator is fully protected from damage due to fault conditions. Linear current limiting is provided. Output current during overload conditions is constant. Thermal shutdown disables the device when the die temperature exceeds the maximum safe operating temperature. The output structure of these regulators allows voltages in excess of the desired output voltage to be applied without reverse current flow.

4.1 Thermal Design

Linear regulators are simple to use. The most complicated design parameters to consider are thermal characteristics. Thermal design requires the following application specific parameters:

- Maximum ambient temperature (T_A)
- Output current (I_{OUT})
- Output voltage (V_{OUT})
- Input voltage (V_{IN})
- Ground current (I_{GND})

First, calculate the power dissipation of the regulator and the device parameters from Electrical Characteristics section or the Typical Performance Curves section.

EQUATION 4-1:

$$P_D = (V_{IN} - V_{OUT})I_{OUT} + V_{IN} \times I_{GND}$$

Then the heat sink thermal resistance is determined with Equation 4-2:

EQUATION 4-2:

$$\theta_{SA} = ((T_{J(MAX)} - T_A)/P_D) - (\theta_{JC} + \theta_{CS})$$

Where:

$T_{J(MAX)}$	=	<125°C
θ_{CS}	=	between 0°C/W and 2°C/W.

The heat sink may be significantly reduced in applications where the minimum input voltage is known and is large compared with the dropout voltage. Use a series input resistor to drop excessive voltage and distribute the heat between this resistor and the regulator. The low dropout properties of Microchip's Super ßeta PNP regulators allow significant reductions in regulator power dissipation and the associated heat sink without compromising performance. When this technique is employed, a capacitor of at least 1.0 µF is needed directly between the input and regulator ground.

4.2 Output Capacitor

The MIC37300/01/02/03 requires an output capacitor for stable operation. As a µCap LDO, the MIC37300/01/02/03 can operate with ceramic output capacitors as long as the amount of capacitance is 47 µF or greater. For values of output capacitance lower than 47 µF, the recommended ESR range is 200 mΩ to 2Ω. The minimum value of output capacitance recommended for the MIC37300 is 10 µF.

For 47 µF or greater, the ESR range recommended is less than 1Ω. Ultra-low ESR, ceramic capacitors are recommended for output capacitance of 47 µF or greater to help improve transient response and noise reduction at high frequency. X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% and 60%, respectively, over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic capacitor to ensure the same minimum capacitance over the equivalent operating temperature range.

4.3 Input Capacitor

An input capacitor of 1.0 µF or greater is recommended when the device is more than 4 inches away from the bulk supply capacitance, or when the supply is a battery. Small, surface-mount chip capacitors can be used for the bypassing. The capacitor should be place within 1 inch of the device for optimal performance. Larger values will help to improve ripple rejection by bypassing the input to the regulator, further improving the integrity of the output voltage.

4.4 Transient Response and 3.3V to 2.5V or 2.5V to 1.8V, 1.65V, or 1.5V Conversions

The MIC37300/01/02/03 has excellent transient response to variations in input voltage and load current. The device has been designed to respond quickly to load current variations and input voltage variations. Large output capacitors are not required to obtain this performance. A standard 47 µF output capacitor, is all that is required. Larger values help to improve performance even further.

By virtue of its low dropout voltage, this device does not saturate into dropout as readily as similar NPN-based designs. When converting from 3.3V to 2.5V or 2.5V to 1.8V, or lower, the NPN based regulators are already operating in dropout, with typical dropout requirements of 1.2V or greater. To convert down to 2.5V or 1.8V without operating in dropout, NPN-based regulators require an input voltage of 3.7V at the very least. The MIC37100 regulator will provide excellent performance with an input as low as 3.0V or 2.25V respectively. This gives the PNP based regulators a distinct advantage over older, NPN based linear regulators.

4.5 Minimum Load Current

The MIC37300/01/02/03 regulator is specified between finite loads. If the output current is too small, then the leakage currents dominate and the output voltage rises. A 10 mA minimum load current is necessary for proper operation. For adjustable regulators, this can be accomplished by selecting the feedback resistors to load the output with 10 mA.

4.6 Error Flag

The MIC37301 and MIC37303 feature an error flag circuit that monitors the output voltage and signals an error condition when the voltage is 5% below the nominal output voltage. The error flag is an open collector output that can sink 10 mA during a fault condition.

Low output voltage can be caused by a number of problems, including an overcurrent fault (device in current limit) or low input voltage. The flag is inoperative during overtemperature shutdown.

4.7 Enable Input

The MIC37301/02/03 also features an enable input for on/off control of the device. Its shutdown state draws “zero” current (only microamperes of leakage). The enable input is TTL/CMOS compatible for simple logic interface, but can be connected up to V_{IN}. When enabled, it draws approximately 15 µA.

4.8 Adjustable Regulator Design

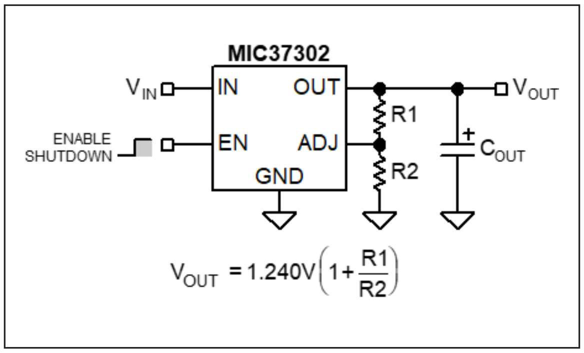


FIGURE 4-1: Adjustable Regulator with Resistors.

The MIC37302 and MIC37303 allow programming the output voltage anywhere between 1.24V and the 5.5V maximum operating rating of the family. Two resistors are used. Resistors can be quite large, up to 1 MΩ, because of the very high input impedance and low bias current of the sense comparator. The resistor values are calculated by:

EQUATION 4-3:

$$R1 = R2\left(\frac{V_{OUT}}{1.240} - 1\right)$$

Where:

V_{OUT} = The desired output voltage.

Figure 4-1 shows the component definition. Applications with widely varying load currents may scale the resistors to draw the minimum load current required for proper operation.

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

Package	Marking	Example
8-Lead SOIC*	XXXXX -XXXXX WNNN	37301 -15YME 1916
3-Lead S-PAK*	XXXXX -X.XXX WNNNP XXX	37300 -1.5WR 1910P USA
5-Lead S-PAK*	XXXXX XX WNNNP XXX	37302 WR 1930P USA
5-Lead TO-263*	XXX XXXXXXX WNNNP	MIC 37302WU 1936P
8-Lead DFN*	XXXXX WNNNP	37303 1836P

Legend:

XX...X	Product code or customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week '01')
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

●, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).

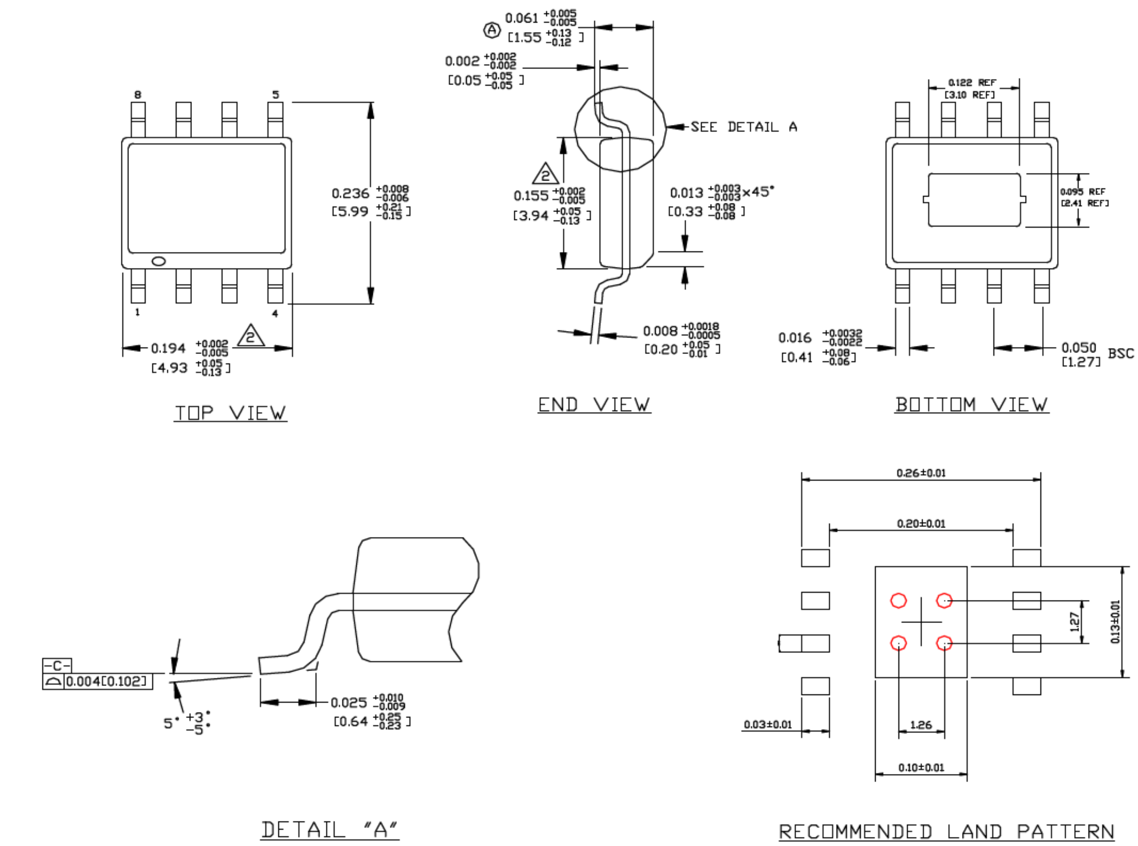
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

8-Lead SOIC-8 (ME) Package Outline and Recommended Land Pattern

TITLE
8 LEAD SOICN EPAD PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOICNEP-8LD-PL-1	**UNIT**	INCH [MM]



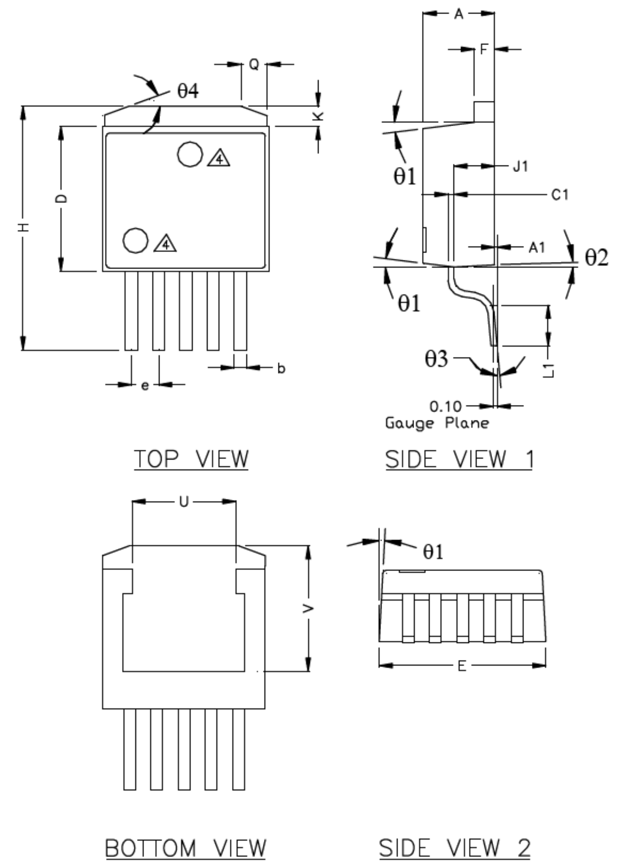
NOTE:
1. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL EXCEED 0.006 INCHES PER SIDE
2. RED CIRCLES IN LAND PATTERN REPRESENT THERMAL VIAS. RECOMMENDED SIZE IS 0.30-0.30MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAXIMUM THERMAL PERFORMANCE

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

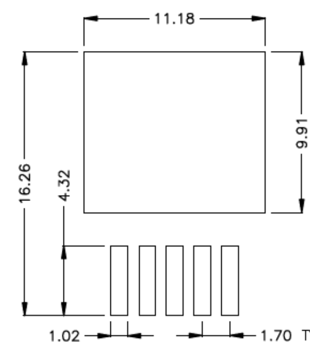
5-Lead TO-263-5 (U) Package Outline and Recommended Land Pattern

TITLE
5 LEAD T0263 PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	T0263-5LD-PL-1	**UNIT**	INCH/MM



POS	INCH		MM	
	MIN	MAX	MIN	MAX
A	0.170	0.181	4.318	4.597
A1	0.000	0.012	0.000	0.305
b	0.026	0.036	0.660	0.914
C1	0.012	0.023	0.305	0.584
D	0.330	0.361	8.392	9.169
E	0.396	0.420	10.058	10.668
e	0.062	0.072	1.575	1.829
F	0.045	0.055	1.143	1.397
H	0.575	0.625	14.605	15.875
J1	0.080	0.120	2.032	3.048
K	0.045	0.066	1.143	1.676
L1	0.090	0.110	2.286	2.794
θ1	3°	10°	3°	10°
θ2	1°	7°	1°	7°
θ3	0°	8°	0°	8°
θ4	18°	22°	18°	22°
Q	0.055	0.075	1.397	1.905
U	0.256 Ref.		6.502 Ref.	
V	0.305 Ref.		7.747 Ref.	



RECOMMENDED LAND PATTERN
(UNIT : mm)

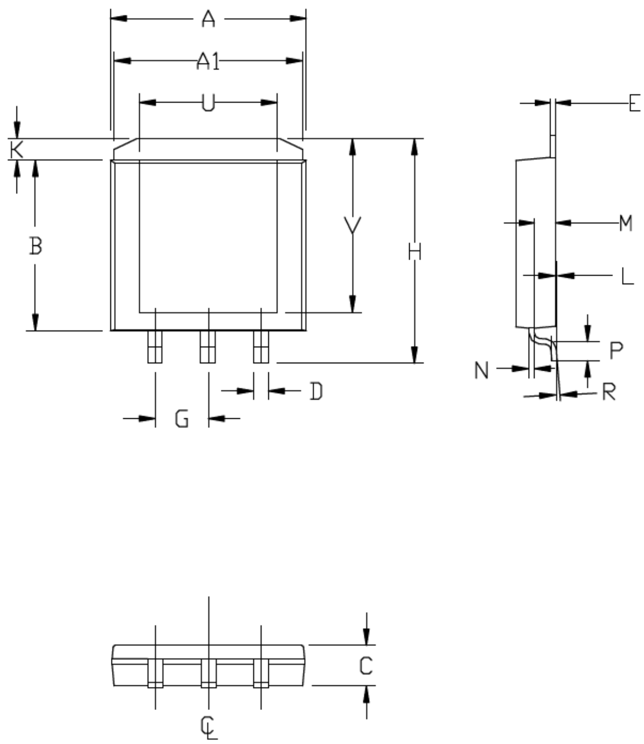
NOTE:
1. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
2. PACKAGE OUTLINE INCLUSIVE OF PLATING THICKNESS.
3. FOOT LENGTH USING GAUGE PLANE METHOD MEASUREMENT 0.010"
4. PACKAGE TOP MARK MAY BE IN TOP CENTER OR LOWER LEFT CORNER
5. ALL DIMENSIONS ARE IN INCHES/MILLIMETERS.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

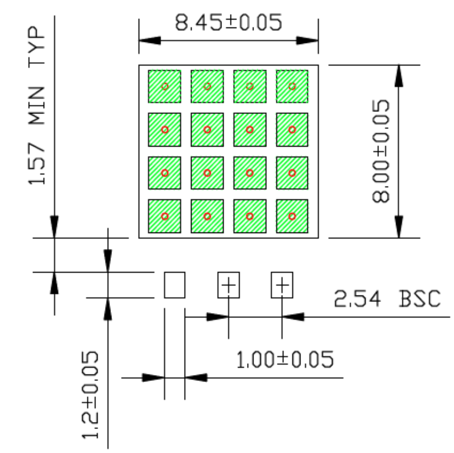
3-Lead S-PAK (R) Package Outline and Recommended Land Pattern

TITLE
3 LEAD SPAK PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SPAK-3LD-PL-1	**UNIT**	INCH/MM



	INCHES		MILLIMETERS	
A	0.365	0.375	9.27	9.52
A1	0.350	0.360	8.89	9.14
B	0.310	0.320	7.87	8.13
C	0.070	0.080	1.78	2.03
D	0.025	0.031	0.63	0.79
E	0.010	BSC	0.25	BSC
G	0.100	BSC	2.54	BSC
H	0.410	0.420	10.41	10.67
K	0.030	0.050	0.76	1.27
L	0.001	0.005	0.03	0.13
M	0.035	0.045	0.89	1.14
N	0.010	BSC	0.25	BSC
P	0.031	0.041	0.79	1.04
R	0°	6°	0°	6°
U	0.256	BSC	6.50	BSC
V	0.316	BSC	8.03	BSC



RECOMMENDED LAND PATTERN (UNIT: MM)

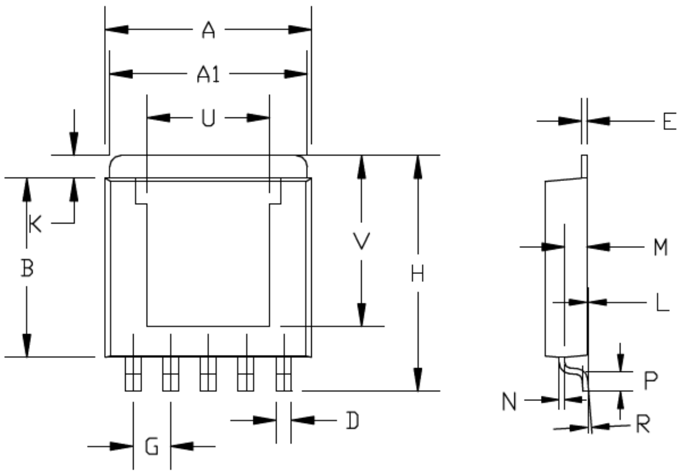
NOTE:
1. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. DIMENSION INCLUDES PLATING THICKNESS. SOLDER MASK OPENING
3. RED CIRCLES IN LAND PATTERN REPRESENT THERMAL VIA, 0.30MM IN DIAMETER & SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE
4. GREEN RECTANGLES IN LAND PATTERN REPRESENT SOLDER STENCIL OPENING (OPTIONAL), 1.50X1.50MM.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

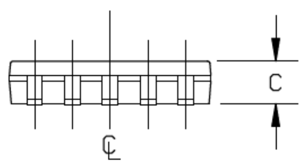
5-Lead S-PAK (R) Package Outline and Recommended Land Pattern

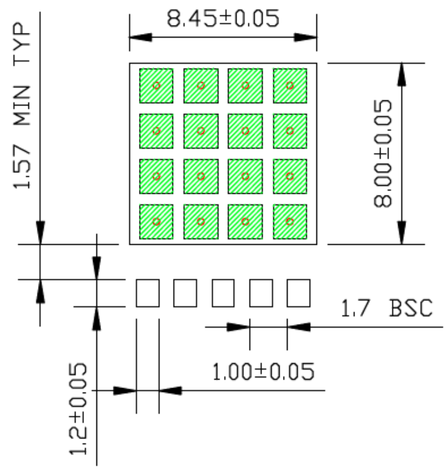
TITLE
5 LEAD SPAK PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SPAK-5LD-PL-1	UNIT	MM



	INCHES		MILLIMETERS	
A	0.365	0.375	9.27	9.52
A1	0.350	0.360	8.89	9.14
B	0.310	0.320	7.87	8.13
C	0.070	0.080	1.78	2.03
D	0.025	0.031	0.63	0.79
E	0.010	BSC	0.25	BSC
G	0.067	BSC	1.70	BSC
H	0.410	0.420	10.41	10.67
K	0.030	0.050	0.76	1.27
L	0.001	0.005	0.03	0.13
M	0.035	0.045	0.89	1.14
N	0.010	BSC	0.25	BSC
P	0.031	0.041	0.79	1.04
R	0°	6°	0°	6°
U	0.220	BSC	5.58	BSC
V	0.296	BSC	7.52	BSC





RECOMMENDED
LAND PATTERN

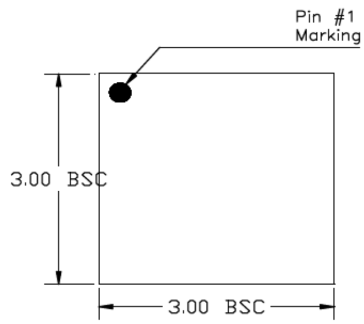
NOTE:
1. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. DIMENSION INCLUDES PLATING THICKNESS. SOLDER MASK OPENING
3. RED CIRCLES IN LAND PATTERN REPRESENT THERMAL VIA, 0.30MM IN DIAMETER & SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE
4. GREEN RECTANGLES IN LAND PATTERN REPRESENT SOLDER STENCIL OPENING (OPTIONAL), 1.50X1.50MM.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

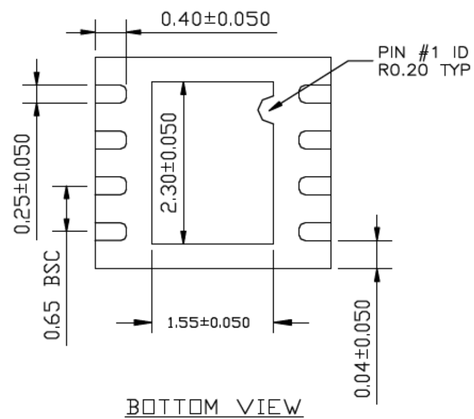
8-Lead 3 mm x 3 mm DFN (ML) Package Outline and Recommended Land Pattern

TITLE
8 LEAD DFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

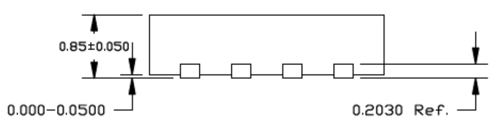
DRAWING #	DFN33-8LD-PL-1	**UNIT**	MM



TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



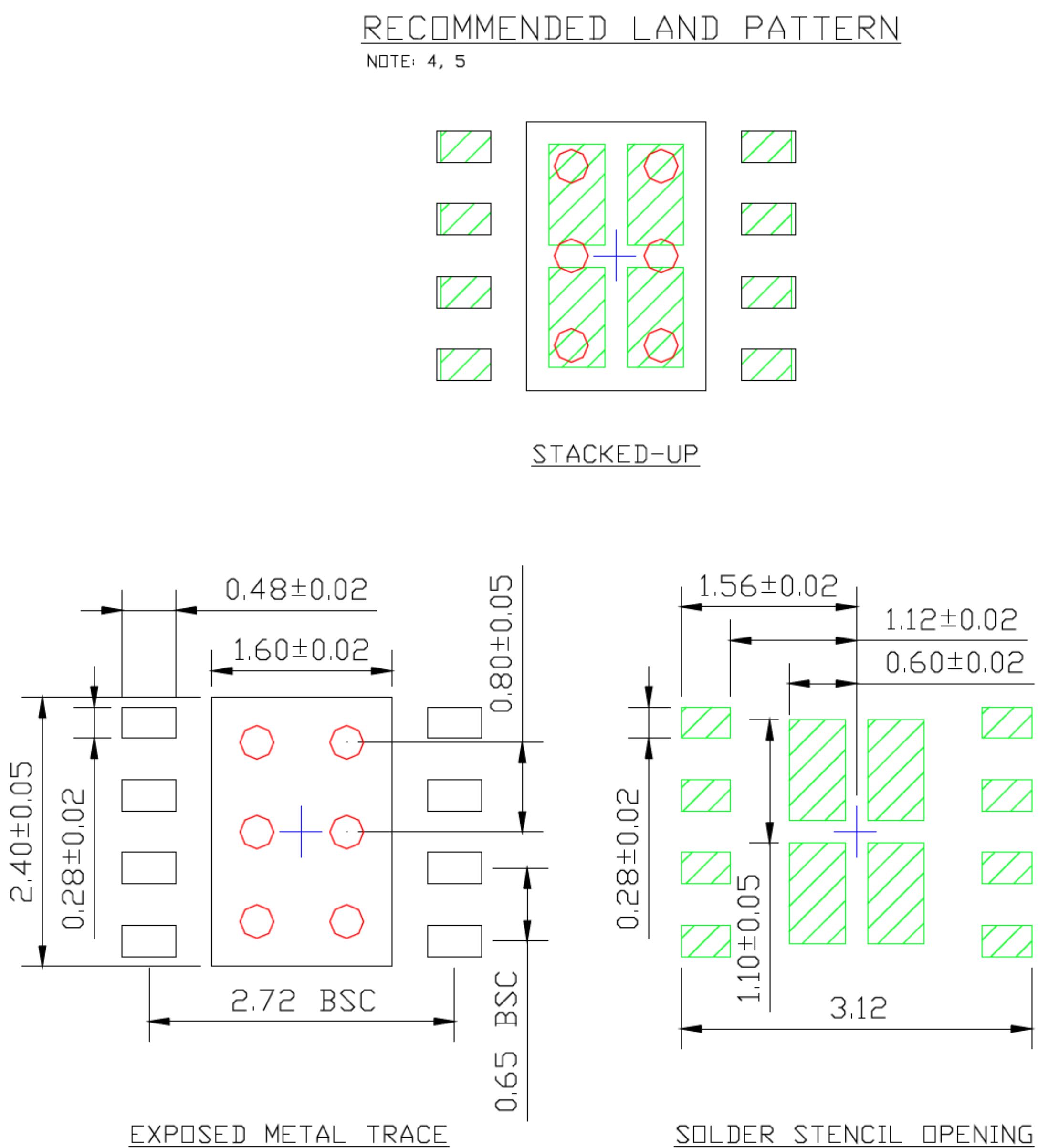
SIDE VIEW
NOTE: 1, 2, 3

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) INDICATE SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.50x0.90 MM IN SIZE, 0.20 MM SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

8-Lead 3 mm x 3 mm DFN (ML) Package Outline and Recommended Land Pattern

POD-Land Pattern drawing #DFN33-8LD-PL-1



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (March 2019)

- Converted Micrel document MIC37300/01/02/03 to Microchip data sheet DS20006169A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	–X.X	X	XX	–XX
Device	Output Voltage	Junction Temperature Range	Package	Media Type

Device:	MIC373xx: 3.0A Low-Voltage µCap LDO Regulator MIC37300: Fixed V_{OUT} to 3.3V in S-PAK (3-Pin) Package MIC37301: Fixed V_{OUT} to 3.3V in S-PAK (5-Pin) 8-Pin SOIC (ePad) Package MIC37302: Adjustable V_{OUT} to 1.24V in S-PAK Package (5-Pin) MIC37303: Adjustable V_{OUT} to 1.24V in 8-Pin ePad SOIC and DFN Packages
Output Voltage:	Fixed Output Voltage Option (MIC37300/37301) 1.5 = 1.5V 1.65 = 1.65V 1.8 = 1.8V 2.5 = 2.5V 3.3 = 3.3V Adjustable Output Voltage Option (MIC37302, MIC37303) <blank> = Adjustable
Junction Temperature Range:	W = –40°C to +125°C, RoHs Compliant* Y = –40°C to +125°C, RoHs Compliant
Package:	R = S-PAK-3, S-PAK-5 (MIC37300, MIC37301 and MIC37302) M = SOIC-8 (ePad), DFN (MIC37301/37303) U = TO-263-5 (MIC37302)
Media Type:	<blank> = 48/Tube (R, S-PAK) <blank> = 50/Tube (U, TO-263-5) <blank> = 95/Tube (M, SOIC-8, DFN) T5 = 500/Reel (M, DFN) TR = 750/Reel (R, U, S-PAK, TO-263-5) TR = 2,500/Reel (M, SOIC-8 (ePad), DFN)

*RoHS-compliant with 'high-melting solder' exemption.

Examples:

a) MIC37300-1.5WR:	3.0A Low-Voltage µCap LDO Regulator, 1.5 Fixed Output Voltage option, –40°C to +125°C Junction Temperature Range, RoHs Compliant, 3-Lead S-PAK, 48/Tube
b) MIC37300-1.8WR-TR:	3.0A Low-Voltage µCap LDO Regulator, 1.5 Fixed Output Voltage option, –40°C to +125°C Junction Temperature Range, RoHs Compliant, 3-Lead S-PAK, 750/ Reel
c) MIC37301-1.65YM:	3.0A Low-Voltage µCap LDO Regulator, 1.65 Fixed Output Voltage option, –40°C to +125°C Junction Temperature Range, RoHs Compliant, SOIC-8, 95/Tube
d) MIC37301-1.65YM-TR:	3.0A Low-Voltage µCap LDO Regulator, 1.65 Fixed Output Voltage option, –40°C to +125°C Junction Temperature Range, RoHs Compliant, DFN, 2,500/Reel
e) MIC37302WU:	3.0A Low-Voltage µCap LDO Regulator, ADJ. Output Voltage option, –40°C to +125°C Junction Temperature Range, RoHs Compliant, TO-263-5, 50/Tube
f) MIC37302WU-TR:	3.0A Low-Voltage µCap LDO Regulator, ADJ. Output Voltage option, –40°C to +125°C Junction Temperature Range, RoHs Compliant, TO-263-5, 750/Reel
g) MIC37303YM:	3.0A Low-Voltage µCap LDO Regulator, ADJ. Output Voltage option, –40°C to +125°C Junction Temperature Range, RoHs Compliant, SOIC-8, 95/Tube
h) MIC37303YM-T5:	3.0A Low-Voltage µCap LDO Regulator, ADJ. Output Voltage option, –40°C to +125°C Junction Temperature Range, RoHs Compliant, DFN, 500/Reel
h) MIC37303YM-TR:	3.0A Low-Voltage µCap LDO Regulator, ADJ. Output Voltage option, –40°C to +125°C Junction Temperature Range, RoHs Compliant, SOIC-8, 2, 500/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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