

LTM467

Quad Output (Dual 12A, Dual 5A) Step-Down µModule Regulator

DESCRIPTION

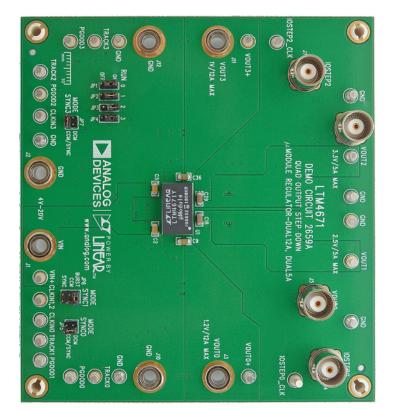
DC-DC point-of-load regulator in a thermally enhanced requirements. The LTM4671EY is a complete multi-output can be paralleled together to satisfy higher rail current rails can be paralleled together, and lower current rails voltage is programmable from 0.6V to 5.5V. High current from 0.6V to 3.3V while the two lower current rails' output two higher current rails' output voltage is programmable up to 5A from each of its two lower current rails. The up to 12A from each of its two higher current rails and operating input voltage range of 3.6V to 20V providing four output step-down regulator. The LTM4671EY has an µModule® regulator, a high performance high efficiency Demonstration circuit 2659A features the LTM®4671

> a few input and output capacitors. Output voltage tracking is made available by the TRACK/SS pins for supply rail modifying demo circuit 2659A in conjunction with this demo manual for working on or module phases. The LTM4671 data sheet must be read pins provide for optional synchronization of additional nization is available through the CLKIN pins, CLKOUT via the TSENSE and TMON pins. External clock synchrosequencing. Temperature sensing options are included 16mm × 9.5mm × 4.82mm BGA package requiring only

Design files for this circuit board are available.

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BOARD PHOTO



PERFORMANCE SUMMARY Specifications are at $T_A = 25$ °C

PARAMETER	CONDITIONS/NOTES	VALUE
Input Voltage Range		3.6V - 20V
Output Voltage V _{OUT}	Jumper Selectable	$V_{0UT0} = 1.2V_{DC}, V_{0UT1} = 2.5V_{DC}, V_{0UT2} = 3.3V_{DC}, V_{0UT4} = 1V_{DC}$
Maximum Continuous Output Current per Phase	De-Rating is Necessary for Certain Operating Conditions. See Data Sheet for Details	IOUTOMAX, IOUT3MAX = 12ADC IOUT1MAX, IOUT2MAX = 5ADC
Default Operating Frequency		600kHz (for V _{0UT0} , V _{0UT3}) 1MHz (for V _{0UT1} , V _{0UT2})
Efficiency	V _{IN} = 12V V _{OUTO} = 1.2V, I _{OUT} = 12A V _{OUTO} = 3.3V, I _{OUT} = 5A	See Figure 2 87.4% 91.6%

QUICK START PROCEDURE

Demonstration circuit 2659A is an easy way to evaluate the performance of the LTM4671EY. Please refer to Figure 1 for test setup connections and follow the procedure below.

 With power off, place the jumpers in the following positions:

CCM	CCM	CCM	NO	NO	NO	NO
MODE3	MODE1	MODE0	RUN3	RUN2	RUN1	RUN0
JP7	JP6	JP5	JP4	JP3	JP2	JP1

- 2. Before connecting input supply, loads and meters, preset the input voltage supply to be between 4V to 20V. Preset the load currents to 0A.
- With power off, connect the loads, input voltage supply and meters as shown in Figure 1.
- Turn on input power supply. The output voltage meters for each phase should display the programmed output voltage ±2%.
- 5. Once the proper output voltages are established, adjust the load currents for each phase within the 0A–12A

- range for V_{OUT0} and V_{OUT3} outputs and within OA–5A for V_{OUT1} and V_{OUT2} outputs. Observe each output's load regulation, efficiency, and other parameters. Output voltage ripples for each output should be measured across the furthest output capacitor with a BNC cable and oscilloscope. BNCs J5 and J9 are available for V_{OUT0} and V_{OUT2} ripple measurements, respectively.
- 6. To observe increased light load efficiency, for V_{OUTO} and V_{OUT3} place the MODE pin jumpers (JP5, JP7) in the DCM position, for V_{OUT1} and V_{OUT2} place the MODE pin jumper (JP6) in the BURST position.
- 7. For optional load transient testing on-board transient circuits are provided to measure transient responses on V_{OUTO} and V_{OUT2} outputs. Place a positive pulse signal between the IOSTEPx_CLK pin and GND pins. The pulse amplitude sets the load step current amplitude. The pulse width should be short (<1ms) and pulse duty cycle should be low (<15%) to limit the thermal stress on the load transient circuit. The load step response for V_{OUTO} and V_{OUT2} can be monitored with a BNC connected to J4 (10mV/A) and J7 (20mV/A), respectively.

QUICK START PROCEDURE

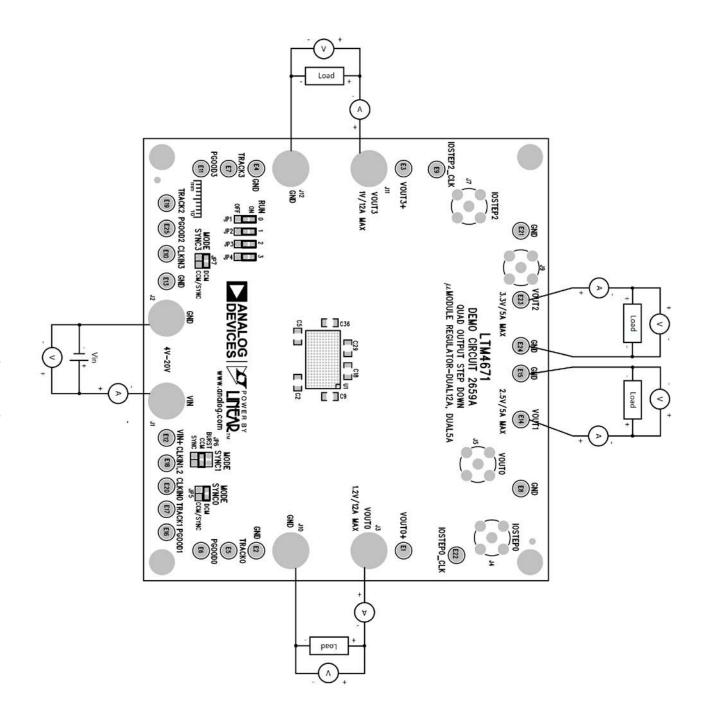
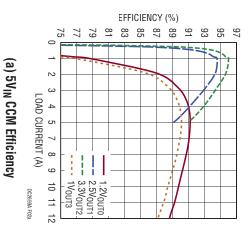


Figure 1. Test Setup of DC2659A

QUICK START PROCEDURE



EFFICIENCY (%)

8

75 79 77

0

2

ω

9

10 11 12

DC2659A F02b

1.2Vоито 2.5Vоит1 3.3Vоит2 1Vоит3

(b) 12V_{IN} CCM Efficiency

97 95 93 91 91 89 87 83

Figure 2. Measured Supply Efficiency at $5V_{IN}$ and $12V_{IN}$

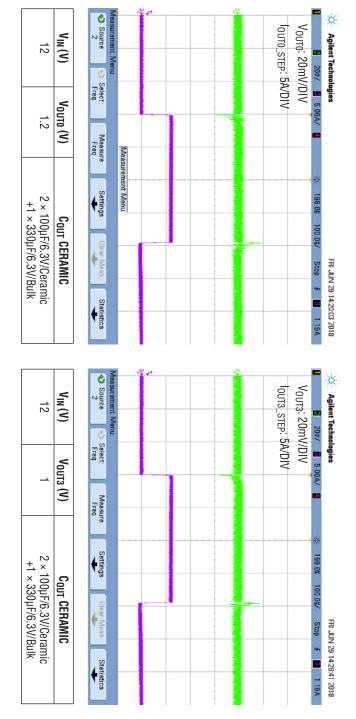
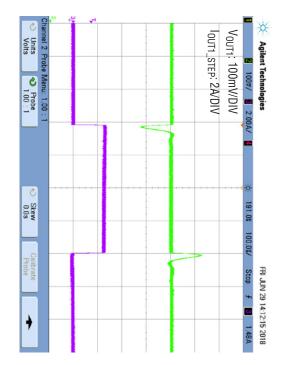


Figure 3. Measured V_{0UT0} = 1.2V and V_{0UT3} = 1V Load Transient Responses (6A Load Step)

QUICK START PROCEDURE

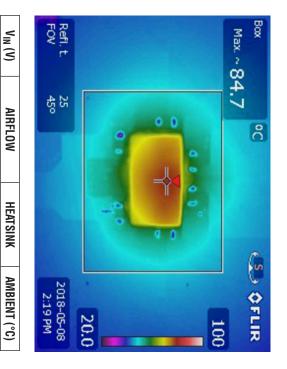


	Save	- 4	- T			Ş			=
Save	Save to file =						TOUT2_STEP: 5A/DIV	V _{OUT2} : 100mV/DIV	
	= scope						STEP:	100	100
Recall	9 9						5A/C	mV/D	4
9							₹	₹	2.00/
				ı		7			<
Default	L			L					
	2			L	 				*
				L					199.0%
F									100.0%/
Press to					•				Stop
									£ 3 513m
Quick Print									<u> </u>
Print									513m

2 × 4/μF/6.3V/Ceramic +1 × 10μF/6.3V/Ceramic	2.5	12
		5
C _{OUT} CERAMIC	V _{0UT1} (V)	V _{IN} (V)

V _{IN} (V)	V _{0UT2} (V)	C _{OUT} CERAMIC
12	3.3	2 × 47µF/6.3V/Ceramic +1 × 10uF/6.3V/Ceramic

Figure 4. Measured V_{0UT1} = 2.5V and V_{0UT2} =3.3V Load Transient Responses (2.5A Load Step)



Refl. t. FOV		Box Max. ~ 89.0
45°		
3		°C
2018-05-08 2:43 PM	20.0	(NE) \$FLIR

CHANNEL	
VOLITO	
Volita	
Valle	
Valle	

VIN (V)

12

Natural Convection

23

		200LFM	
	None	Forced Air	12
AMBIENT (°C	HEATSINK	AIRFLOW	V _{IN} (V)

CHANNEL	V _{OUTO}	V _{OUT1}	V _{OUT2}	V _{OUT3}
$V_{OUT}(V)$	1.2	2.5	3.3	1
I _{OUT} (A)	12	5	5	12

Figure 5. Measured Thermal Captures

PARTS LIST

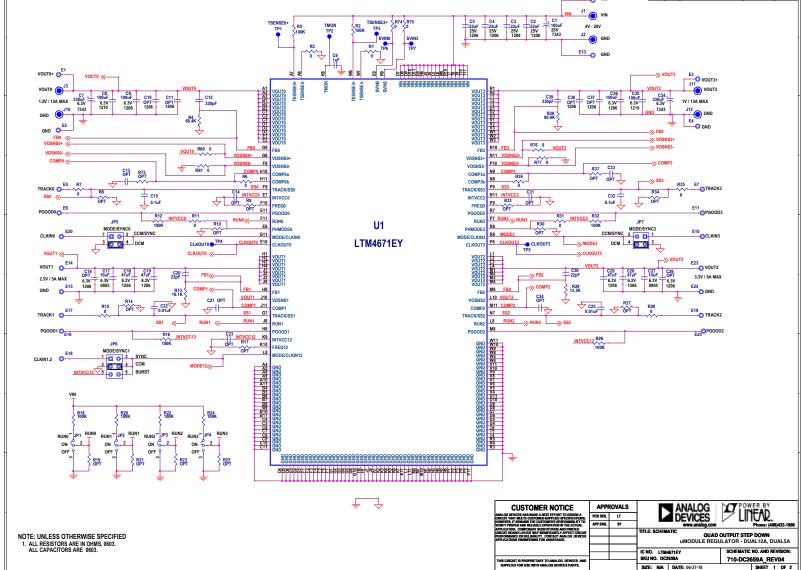
19	18	17	16	15	14	13	12	⇉	10	9	00	7	6	5	4	ω	2	_	Additio	00	7	6	5	4	ω	2	_	Requir	ITEM
_	_	2	4	10	16	2	2	4	2	_	_	2	2	2	2	2	2	2	nal De	_	_	_	1	_	2	2	4	ed Circ	QTY
R70	R55	R54, R69	R50, R51, R82, R83	R2, R5, R12, R16, R26, R32, R18, R20, R22, R24	R1, R3, R6, R7, R11, R15, R28, R31, R35, R36, R74, R75, R76, R77, R80, R81	Q1, Q2	C42, C46	C40, C43, C45, C47	C22, C25	C6	C1	C15, C32	C12, C39	C20, C30	C19, C29	C17, C27	C9, C36	C7, C34	Additional Demo Board Circuit Components	Li	R39	R29	R13	R4	C18, C28	C8, C35	C2, C3, C4, C5	Required Circuit Components	REFERENCE
RES., 0.02, 1%, 1/2W, 2010, SENSE, AEC-Q200	RES., 0.01, 1%, 1/2W, 2010, SENSE, AEC-Q200	RES., 10k, 1%, 1/10W, 0603, AEC-Q200	RES., 1k, 1%, 1/10W, 0603, AEC-Q200	RES., 100k, 1%, 1/10W, 0603, AEC-Q200	RES., 0Ω, 1/10W, 0603, AEC-Q200	XSTR., MOSFET, N-CH, 40V, TO-252 (DPAK)	CAP, 1µF, X7R, 50V, 10%, 0805	CAP, 1µF, X7R, 16V, 20%, 0603	CAP, 0.01μF, X7R, 50V, 10%, 0603	CAP., 1µF, X5R, 16V, 10%, 0603	CAP., 100µF, TANT. POLY., 25V, 20%, 7343	CAP., 0.1μF, X7R, 50V, 10%, 0603	CAP, 330pF, C0G, 50V, 5%, 0603	CAP., 22pF, C0G, 50V, 5%, 0603	CAP, 47µF, X5R, 16V, 20%, 1206	CAP, 10µF, X5R, 16V, 10%, 0805	CAP., 100μF, X5R, 6.3V, 20%, 1206	CAP., 330μF, ALUM. ELECT., 2.5V, 20%, 7343, 9mΩ, 6.3A		IC, QUAD HIGH EFFICIENCY MODULE, BGA-16mm × 9.5mm × 4.72mm	RES., 90.9k, 1%, 1/10W, 0603, AEC-Q200	RES., 13.3k, 1%, 1/10W, 0603, AEC-Q200	RES., 19.1k, 1%, 1/10W, 0603, AEC-Q200	RES., 60.4k, 1%, 1/10W, 0603, AEC-Q200	CAP, 47µF, X5R, 16V, 20%, 1206	CAP., 100μF, X5R, 6.3V, 20%, 1210	CAP., 22µF, X5R, 25V, 20%, 1206		PART DESCRIPTION
VISHAY, WSL2010R0200FEA	VISHAY, WSL2010R0100FEA	VISHAY, CRCW060310K0FKEA	VISHAY, CRCW06031K00FKEA	VISHAY, CRCW0603100KFKEA	VISHAY, CRCW06030000Z0EA	VISHAY, SUD50N04-8M8P-4GE3	MURATA, GRM21BR71H105KA12L	TDK, C1608X7R1C105M080AC	KEMET, C0603C103K5RACTU	MURATA, GRM188R61C105KA93D	KEMET, T521X107M025ATE060	TDK, C1608X7R1H104K080AA	MURATA, GRM1885C1H331JA01J	MURATA, GRM1885C1H220JA01J	TDK, C3216X5R1C476M160AB	MURATA, GRM21BR61C106KE15L	TDK, C3216X5R0J107M160AB	PANASONIC, EEFSX0E331ER		ANALOG DEVICES., LTM4671EY#PBF	VISHAY, CRCW060390K9FKEA	VISHAY, CRCW060313K3FKEA	VISHAY, CRCW060319K1FKEA	VISHAY, CRCW060360K4FKEA	TDK, C3216X5R1C476M160AB	TDK, C3225X5R0J107M250AC	MURATA, GRM31CR61E226ME15L		MANUFACTURER/PART NUMBER

PARTS LIST

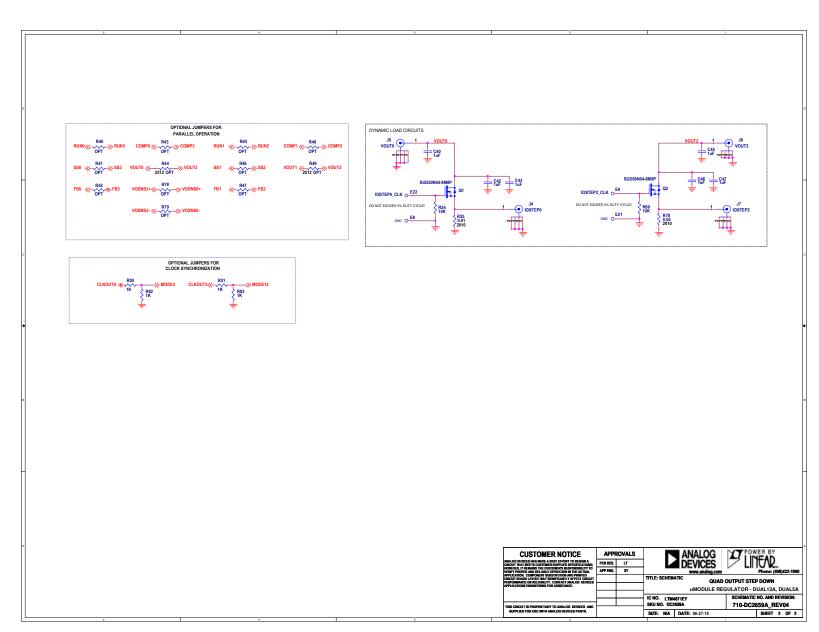
ITEM	ΩTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Hardware	are			
_	25	E1, E2, E3, E4, E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, E16, E17, E18, E19, E20, E21, E22, E23, E24, E25	TEST POINT, TURRET, 0.094", MTG. HOLE	MILL-MAX, 2501-2-00-80-00-00-07-0
2	9	J1, J2, J3, J10, J11, J12	CONN.,BANANA JACK, FEMALE, THT,	KEYSTONE, 575-4
ω	4	JP1, JP2, JP3, JP4	CONN., HDR, MALE, 1mm ×3mm × 2mm, VERT, STR, THT	WURTH ELEKTRONIK, 62000311121
4	4	J4, J5, J7, J9	CONN., RF, BNC, RCPT JACK, 5-PIN, STR, THT, 50Ω	AMPHENOL RF, 112404
57	2	JP5, JP7	CONN., HDR, MALE, $2\text{mm}\times2\text{mm}\times2\text{mm},$ VERT, STR, THT	WURTH ELEKTRONIK, 62000421121
6	_	JP6	CONN., HDR, MALE, $2\text{mm}\times 3\text{mm}\times 2\text{mm},$ VERT, STR, THT	WURTH ELEKTRONIK, 62000621121
7	4	MH1, MH2, MH3, MH4	STANDOFF, NYLON, SNAP-ON, 0.375"	KEYSTONE, 8832
00	7	XJP1, XJP2, XJP3, XJP4, XJP5, XJP6, XJP7	CONN., SHUNT, FEMALE, 2-POS,2mm	WURTH ELEKTRONIK, 60800213421

SCHEMATIC DIAGRAM

REVISION HISTORY ECO REV DESCRIPTION APPROVED DATE PRODUCTION SAM Y. 06-27-18 E12 VIN+ 22uF 25V 1206 TSENSE3+ TP3 SVIN0 R1 TP6 22uF 25V 1206 C3 22uF 25V 1206 TSENSE0+ TMON TP2 E13 GND 58355824459885cep VOUT0+ CH J11 VOUT3+ *************** C36 100uF 6.3V 1206 C8 100uF 6.3V C9 100uF C10 6.3V OPT 1206 1206 C35 100uF 6.3V 1210 1.2V / 12A MAX 330UF 5 6.3V GND J10 7343 330uF 6.3V 7343 C11 OPT 1206 C37 OPT 1206 1V / 12A MAX 12 13 01 02 03 V1 V2 V3 W1 W2 W3 J12 GND R39 90.9K E4 O GND -55 FB3 →>> VOSNS3+ VOUT3 FB3 VOSNS3+ VOSNS3+ R76 0 VOUT3 FB0 G9 FB0 _>> VOSNS3 VOSNS0- « VOSNS3- P10 VOSNS3- R77 0 OSNS0- F8 VOSNS0-C33 VOSNS3-COMP3a N9 COMP3 N9 R36 R37 C13 R73 OPT OPT COMP0 H10 COMP0a сомрзь № —≫ SS3 E7 TRACK3 TRACKO C.... TRACK/SS3 P9 SS3 INTVCC0 E7 R9 F10 OPT E11 PGOOD0 R34 RACK/SS3 INTVCC3 FREQ3 PGO0D3 R7 OPT C15 0.1uF 0.1uF 👃 PGOODIO E6 E11 OPGOOD3 INTVCC0 KII RUN0 F11 RUN0 RUN3 P7 RUN3 >> RUN U1 E6 PHMODE0 MODE/SYNC3 MODE/SYNC0 CCM/SYNC PHMODE3 E10 OCLKIN3 G11 MODE/CLKINO MODE/CLKIN3 R8 MODE3 3 O A DCM CLKOUTO E10 CLKOUTO LTM4671EY P6 CLKOUT3 CLKOUT3 DCM 4 0 0 3 CLKOUT3 VOUT1 < VOUT: VOUT: VOUT: VOUT: VOUT: VOUT: VOUT: VOUT: VOUT1 E14 E23 O VOUT2 C16 OPT 6.3V 1206 C27 C26 10uF OPT C20 = —≫ FB2 FB1₆₆ 2.5V / 5A MAX 6.3V 1206 6.3V 6.3V 6.3V 6.3V 1206 1206 0805 1206 6.3V 1206 E15 R29 13.3K S COMP2 H9 FB1 FB2 M9 FB2 R13 19.1K 0 -O GND VOUT1 J10 VOSNS1 VOSNS2 L10 VOUT2 C24 OPT 0PT C22 0.01uF C21 OPT COMP1 J11 COMP1 COMP2 M11 COMP2 R27 OPT ٦ŀپ ┍╤┼╟╴ E19 TRACK2 SS1 G7 N7 SS2 TRACK/SS1 TRACK/SS2 RUN1 76 L8 RUN2 RUN2



SCHEMATIC DIAGRAM



Rev. 0



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board in you have read and agrees to the Agreement. Tour use of the the Evaluation Board is any office and an agrees that the Evaluation Board is provided for the sole and exclusive, non-sublemass and shall signly your acceptance of the Agreement. This Agreement is and conditions of the Agreement, ADI hereby grants to Customer at free, limited, personal, temporary, non-exclusive, non-sublemass below, non-transferable librarse to use the Evaluation Board for any other purpose. Furthermore, the license grant ad agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board and the Evaluation Board is any other purpose. Furthermore, the license grant and agrees that the Evaluation Board is any other purpose. Furthermore, the license grant is expressly granted the confidential and proprietary information of ADI. Customer the Evaluation Board is any other purpose, affiliates and in-house consultants. The Evaluation Board is any other party for any reason, Upon discontinuation of the Evaluation Board or termination of this Agreement of the Evaluation Board is any other party for any reason, Upon discontinuation of the Evaluation Board or termination of the Evaluation Board is any other party for any reason. Upon discontinuation of the Evaluation Board is any other party for any reason. Upon discontinuation of the Evaluation Board to any other party for any reason. Upon discontinuation of the Evaluation Board is the Evaluation Board or termination of the Evaluation Board is any other party for any reason. Upon discontinuation of the Evaluation Board is the E

