MP8794

16V, 20A, Synchronous, Step-Down Converter with Adjustable Current Limit, Configurable Frequency, and Voltage Tracking

DESCRIPTION

The MP8794 is a fully integrated, high-frequency, synchronous, buck converter. The MP8794 offers a compact solution that achieves up to 20A of output current with excellent load and line regulation over a wide input supply range. The MP8794 operates at high efficiency over a wide output current load range.

The device adopts an internally compensated constant-on-time (COT) control mode that provides fast transient response and eases loop stabilization.

The operating frequency can be set to 600kHz, 800kHz, or 1000kHz with MODE configuration, allowing the MP8794 frequency to remain constant regardless of the input and output voltages.

The output voltage start-up ramp is controlled by an internal 1ms timer that can be increased by adding a capacitor on REF/TRK. An open-drain power good (PGOOD) signal indicates whether the output is within its nominal voltage range. PGOOD is clamped at about 0.7V with an external pull-up voltage when the input supply fails to power the MP8794.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MP8794 requires a minimal number of readily available, standard external components. It is available in a QFN-21 (3mmx4mm) package.

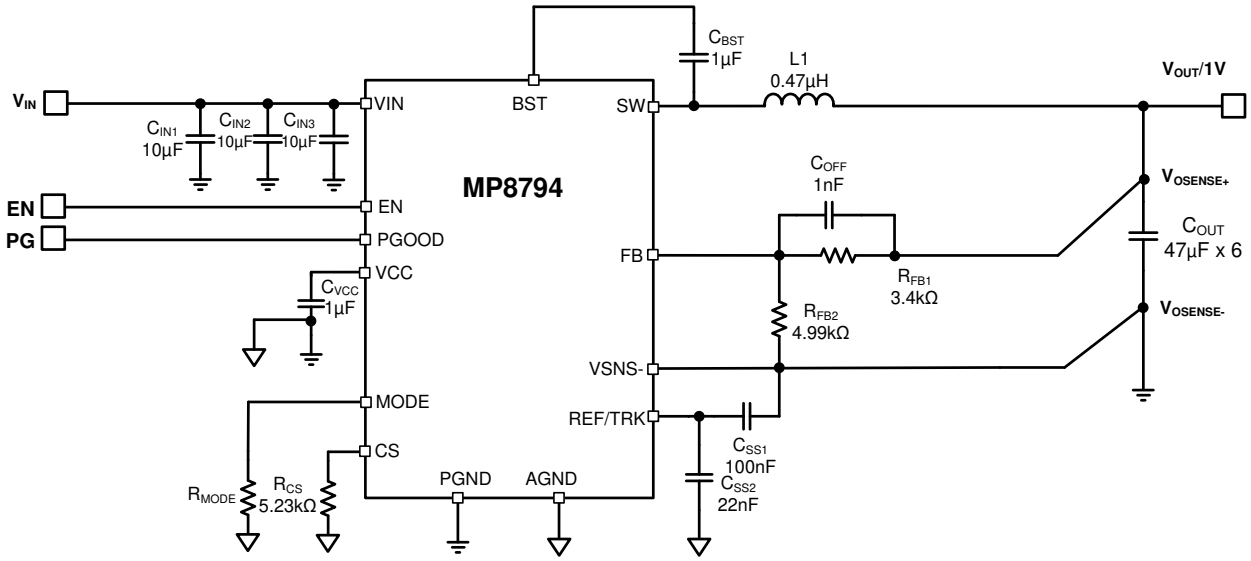
FEATURES

- Wide Input Voltage Range
  - 2.7V to 16V with External 3.3V VCC Bias
  - 4V to 16V with Internal Bias or External 3.3V VCC Bias
- Differential Output Voltage Remote Sense
- Configurable Accurate Current Limit Level
- 20A Output Current
- Low $R_{DS(ON)}$ Integrated Power MOSFETs
- Adaptive COT for Ultra-Fast Transient Response
- Stable with Zero-ESR Output Capacitor
- Output Voltage Discharge
- Excellent Load Regulation
- Output Voltage Tracking
- PGOOD Active Clamped at Low Level during Power Failure
- Programmable Soft-Start Time from 1ms
- Pre-Bias Start-Up
- Selectable Switching Frequency from 600kHz, 800kHz, and 1000kHz
- Non-Latch OCP, OVP, UVP, UVLO, and Thermal Shutdown
- Adjustable Output from 0.6V to 90% of V_{IN}, up to 5.5V Max
- Available in a QFN-21 (3mmx4mm) Package
- The MPL-AY1265 Inductor Series Matches Best Performance

APPLICATIONS

- FPGAs
- Flat-Panel Televisions and Monitors
- Multi-Functional Printers
- Access Points and Routers
- Optical Modules

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP8794GLE	QFN-21 (3mmx4mm)	*See Below*	1

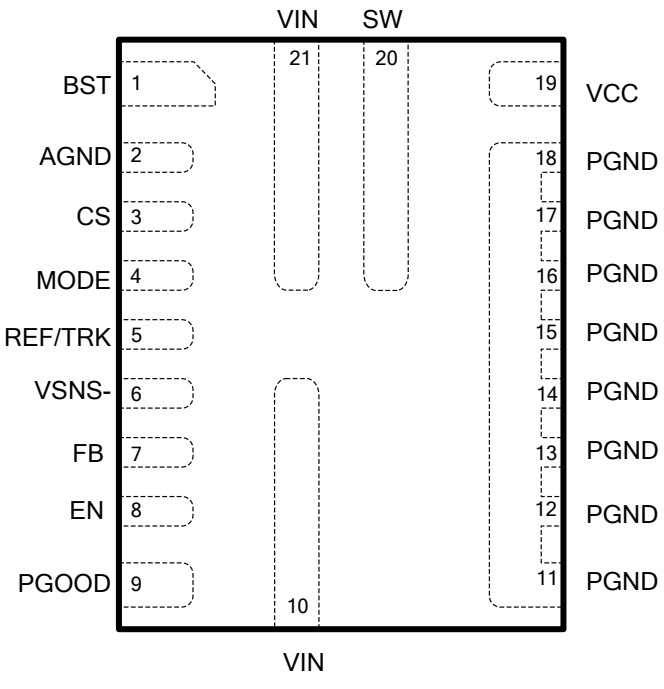
* For Tape & Reel, add suffix –Z (e.g. MP8794GLE–Z).

TOP MARKING

MPYW
8794
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
8794: First four digits of the part number
LLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-21 (3mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver.
2	AGND	**Analog ground.** Select AGND as the control circuit reference point.
3	CS	**Current limit.** Connect a resistor to AGND to set the current limit trip point.
4	MODE	**Operation mode selection.** Program MODE to select the operating switching frequency. See Table 1 on page 14 for additional details.
5	REF/TRK	**External tracking voltage input.** Decouple REF/TRK by placing a ceramic capacitor as close to the pin as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics. The capacitance of the capacitor determines the soft-start time. See Equation 2 on page 14 for additional details.
6	VSNS-	**Differential remote-sense negative input.** Connect VSNS- directly to the negative side of the voltage sense point. Short VSNS- to GND if the remote sense is not used.
7	FB	**Feedback (differential remote-sense positive input).** An external resistor divider from the output to VSNS-, tapped to FB, sets the output voltage. It is recommended to place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.
8	EN	**Enable.** EN is an input signal that turns the regulator on or off. Drive EN high to turn the regulator on; drive EN low to turn it off. For automatic start-up, connect EN to VIN through a pull-up resistor or a resistive voltage divider. Do not float EN.
9	PGOOD	**Power good output.** PGOOD is an open-drain signal. A pull-up resistor connected to a DC voltage is required to indicate a logic high signal if the output voltage is within regulation. There is a delay of about 0.9ms between the time FB becomes greater than or equal to 92.5% of the REF and the time PGOOD pulls high.
10, 21	VIN	**Input voltage.** VIN supplies power to the internal MOSFET and regulator. Input capacitors are required to decouple the input rail. Use wide PCB traces to make the connection.
11–18	PGND	**System ground.** PGND is the reference ground of the regulated output voltage, and requires careful consideration while designing the PCB layout. Use wide PCB traces to make the connection.
19	VCC	**Internal 3V LDO output.** The driver and control circuits are powered by the VCC pin's voltage. Decouple VCC with a minimum 1µF ceramic capacitor, placed as close to the pin as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
20	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to VIN by the high-side switch during the on time of the PWM duty cycle. The inductor current drives SW low during the off time. Use wide PCB traces to make the connection.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
$V_{SW(DC)}$ ..... -0.3V to V_{IN} + 0.3V
V_{SW} (25ns) (2) ..... -3V to +25V
V_{SW} (25ns) ..... -5V to +25V
V_{BST} ..... -0.3V to +22.3V
V_{CC}, EN 4.5V
All other pins ..... -0.3V to +4.3V
Junction temperature ..... 170°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +170°C

ESD Rating

Human body model (HBM) 2000V
Charged device model (CDM) 750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4V to 16V
$V_{IN(DC)}$ - $V_{SW(DC)}$ (4) ..... -0.3V to V_{IN} + 0.3V
$V_{SW(DC)}$ (4) ..... -0.3V to V_{IN} + 0.3V
Output voltage (V_{OUT}) ..... 0.6V to 5.5V
External VCC bias (V_{CC_EXT}) ..... 3.12V to 3.6V
Maximum output current (I_{OUT_MAX}) 20A
Maximum output current limit (I_{OC_MAX}) 24A
Maximum peak inductor current (I_{L_PEAK}) 28A
EN voltage (V_{EN}) 3.6V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance	***θ_{JA}***	***θ_{JC}***	
QFN-21 (3mmx4mm)			
EVL8794-LE-00A (5)	29	4	°C/W
JESD51-7 (6)	50	12	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Measured using a differential oscilloscope probe.
3) The device is not guaranteed to function outside of its operating conditions.
4) The voltage rating can be in the range of -3V to +23V for a period of 25ns or less with a maximum repetition rate of 1000kHz when the input voltage is 16V.
5) Measured on EVL8794-LE-00A, 4-layer PCB, 78mmx81mm.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C [7], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		10	20	μA
Supply current (quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} = 0.62V		650	850	μA
MOSFET						
HS switch on resistance	$HS_{RDS(ON)}$			9		mΩ
LS switch on resistance	$LS_{RDS(ON)}$			3		mΩ
Switch leakage	SW_{LKG_HS}	V_{EN} = 0V, V_{SW} = 0V		0	10	μA
	SW_{LKG_LS}	V_{EN} = 0V, V_{SW} = 12V		0	30	
Current Limit						
Current limit threshold	V_{LIM}		1.15	1.2	1.25	V
I_{CS} to I_{OUT} ratio	I_{CS}/I_{OUT}	I_{OUT} ≥ 2A	9	10	11	μA/A
Low-side negative current limit	I_{LIM_NEG}			-18		A
Negative current limit time out [8]	t_{NCL_Timer}			200		ns
Switching Frequency						
Switching frequency	f_{SW}	MODE = AGND, I_{OUT} = 0A, V_{OUT} = 1V at 25°C	450	600	750	kHz
		MODE = 30.1kΩ to AGND, I_{OUT} = 0A, V_{OUT} = 1V at 25°C	650	800	950	kHz
		MODE = 60.4kΩ to AGND, I_{OUT} = 0A, V_{OUT} = 1V at 25°C	800	1000	1200	kHz
Minimum on time [8]	t_{ON_MIN}	V_{FB} = 500mV			50	ns
Minimum off time [8]	t_{OFF_MIN}	V_{FB} = 500mV			180	ns
Over-Voltage and Under-Voltage Protection (OVP, UVP)						
OVP threshold	V_{OVP}		113%	116%	119%	V_{REF}
UVP threshold	V_{UVP}		77%	80%	83%	V_{REF}
Feedback Voltage and Soft Start						
Feedback voltage	V_{REF}	T_J = -40°C to +125°C	594	600	606	mV
		T_J = 0°C to 70°C	597	600	603	mV
REF/TRK sourcing current	I_{TRACK_Source}	$V_{REF/TRK}$ = 0V		42		μA
REF/TRK sinking current	I_{TRACK_Sink}	$V_{REF/TRK}$ = 1V		12		μA
Soft-start time	$t_{REF/TRK}$	C_{TRACK} = 1nF, T_J = 25°C	0.75	1	1.25	ms
Error Amplifier						
Error amplifier offset	V_{OS}		-3	0	+3	mV
Feedback current	I_{FB}	V_{FB} = REF		50	100	nA
Enable and UVLO						
Enable input rising threshold	VIH_{EN}		1.17	1.22	1.27	V
Enable hysteresis	$V_{EN\text{-}HYS}$			200		mV
Enable input current	I_{EN}	V_{EN} = 2V		0		μA
Soft shutdown discharge FET	R_{ON_DISCH}			80	150	Ω

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C [7], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VIN UVLO						
VIN under-voltage lockout rising threshold	VIN_{Vth_Rise}	V_{CC} = 3.3V	2.1	2.4	2.7	V
VIN under-voltage lockout falling threshold	VIN_{vth_Fall}		1.55	1.85	2.15	
VCC Regulator						
VCC under-voltage lockout rising threshold	VCC_{Vth_Rise}		2.65	2.8	2.95	V
VCC under-voltage lockout falling threshold	VCC_{vth_Fall}		2.35	2.5	2.65	V
VCC regulator	V_{CC}		2.88	3.00	3.12	V
VCC load regulation		I_{CC} = 25mA		0.5		%
Power Good						
Power good high threshold	$PG_{Vth\_Hi\_Rise}$	FB from low to high	89.5%	92.5%	95.5%	V_{REF}
Power good low threshold	$PG_{Vth\_Lo\_Rise}$	FB from low to high	113%	116%	119%	V_{REF}
	$PG_{Vth\_Lo\_Fall}$	FB from high to low	77%	80%	83%	V_{REF}
Power good low-to-high delay	PG_{td}	T_J = 25°C	0.63	0.9	1.17	ms
Power good sink current capability	V_{PG}	I_{PG} = 10mA			0.5	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 3.3V			3	µA
Power good low-level output voltage	V_{OL_100}	V_{IN} = 0V, pull PGOOD up to 3.3V through a 100kΩ resistor at 25°C		650	800	mV
	V_{OL_10}	V_{IN} = 0V, pull PGOOD up to 3.3V through a 10kΩ resistor at 25°C		750	900	mV
Thermal Protection						
Thermal shutdown [8]	T_{SD}			160		°C
Thermal shutdown hysteresis [8]				30		°C

Notes:

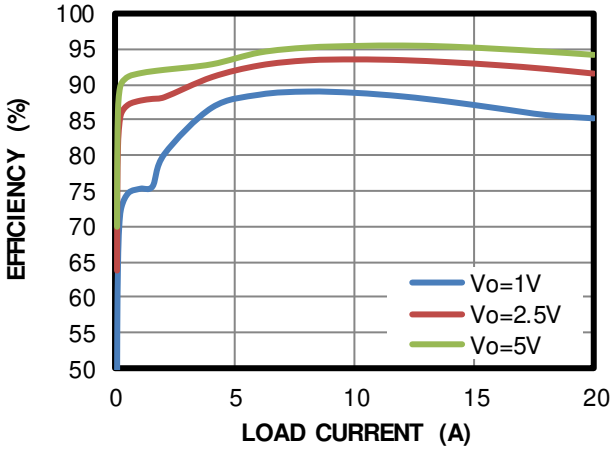
7) Guaranteed by design.
8) Guaranteed by design over temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, V_{OUT} = 1.2V, f_{SW} = 800kHz, unless otherwise noted.

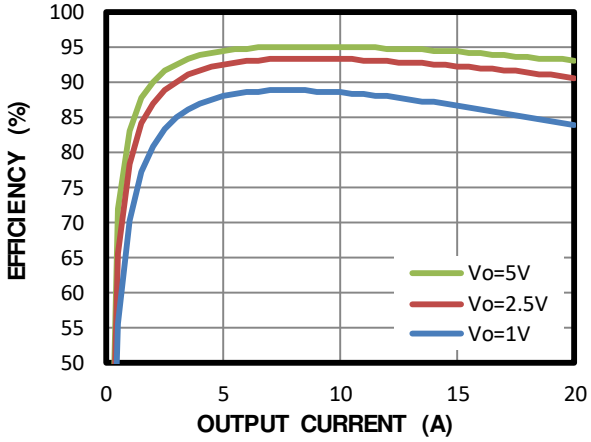
Efficiency

Pulse skip, 0.4µH, 800kHz



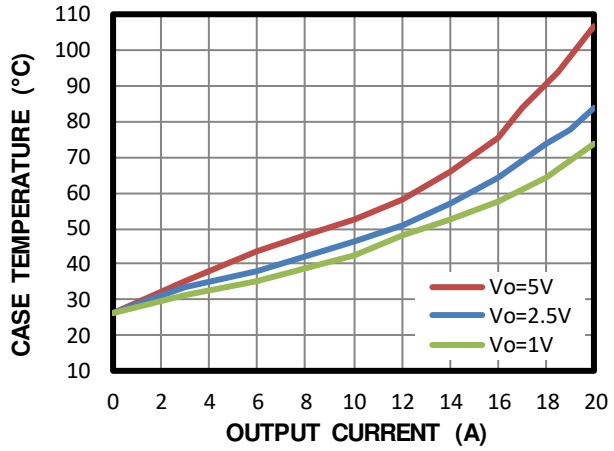
Efficiency

Forced CCM, 0.4µH, 800kHz



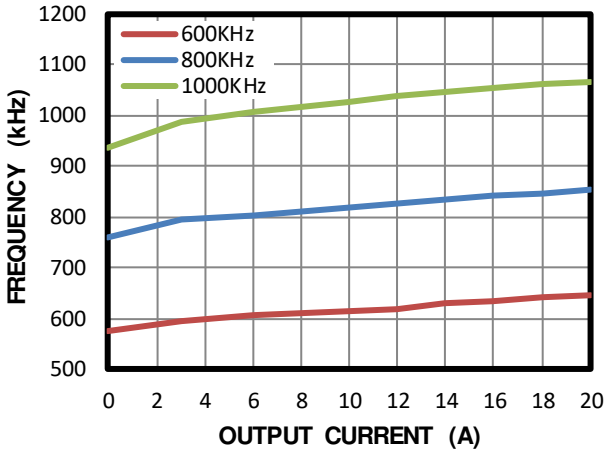
Thermal Results

800kHz, no air flow

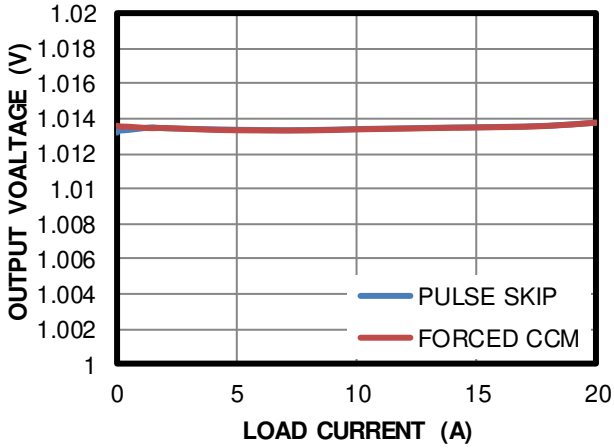


Switching Frequency vs. Output Current

Forced CCM



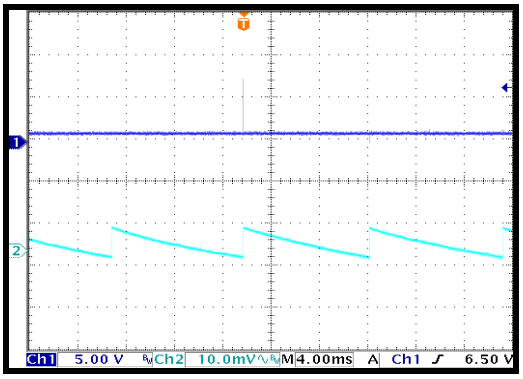
Output Voltage Load Regulation



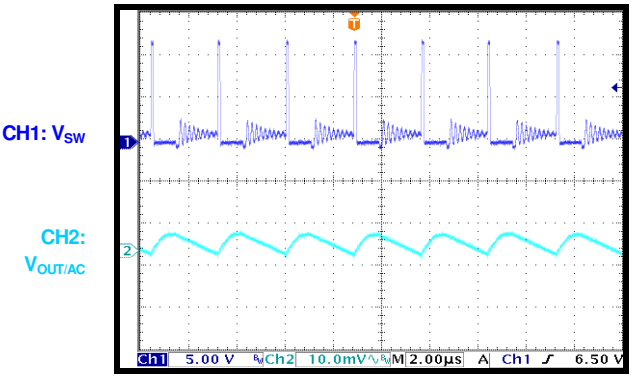
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, V_{OUT} = 1.2V, f_{SW} = 800kHz, unless otherwise noted.

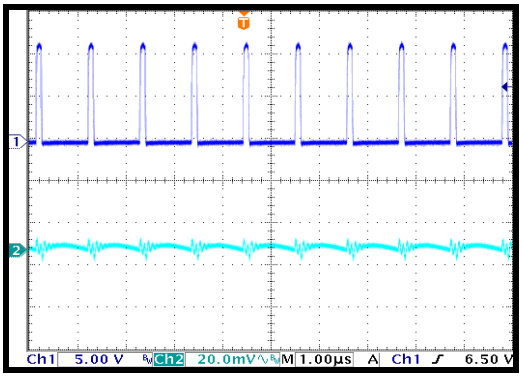
Steady State
I_{OUT} = 0A, pulse skip



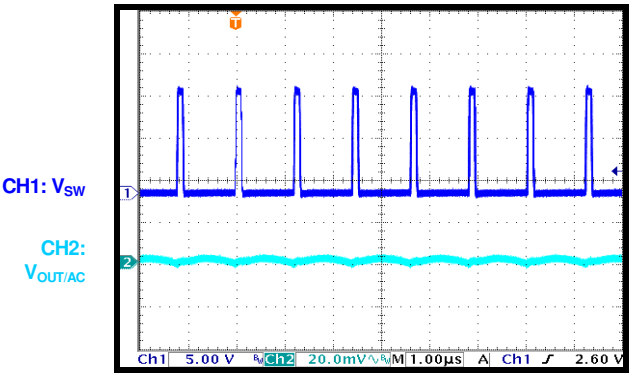
Steady State
I_{OUT} = 0.5A, pulse skip



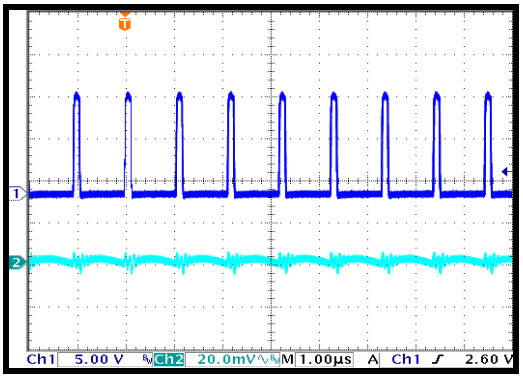
Steady State
I_{OUT} = 20A, pulse skip



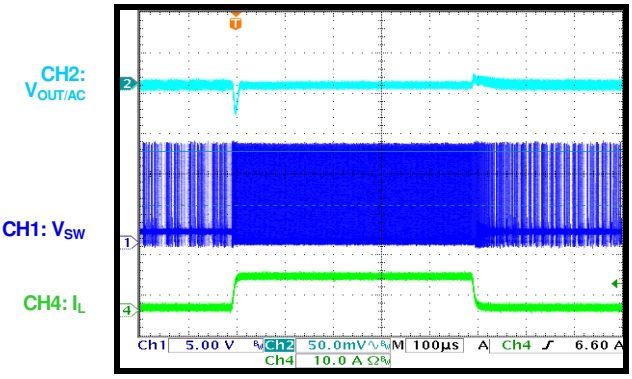
Steady State
I_{OUT} = 0A, forced CCM



Steady State
I_{OUT} = 20A, forced CCM



Load Transient
I_{OUT} = 0A to 8A, pulse skip

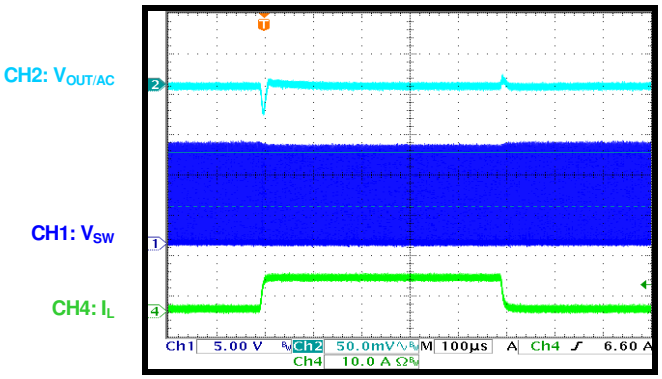


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, V_{OUT} = 1.2V, f_{SW} = 800kHz, unless otherwise noted.

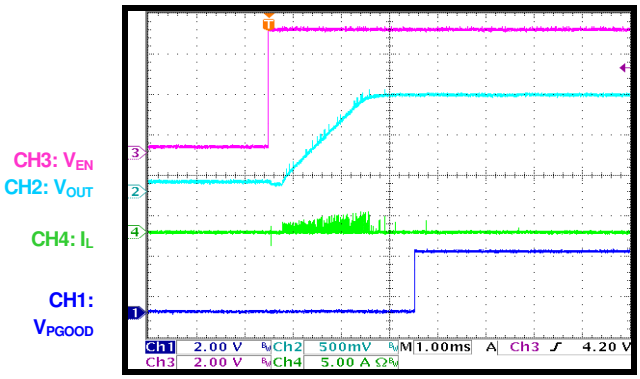
Load Transient

I_{OUT} = 0A to 8A, forced CCM



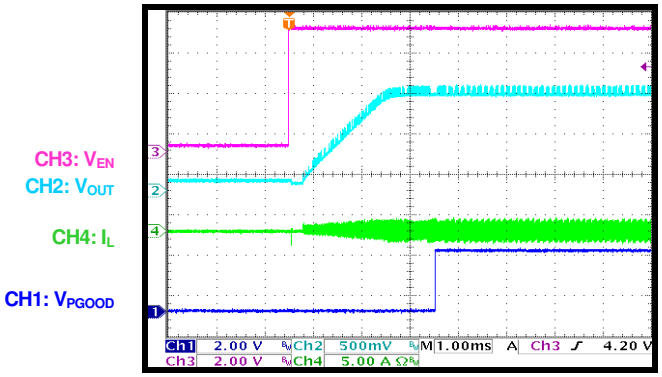
Start-Up through EN

I_{OUT} = 0A, pulse skip



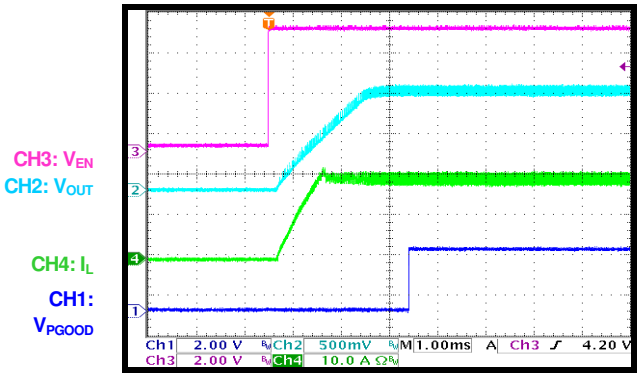
Start-Up through EN

I_{OUT} = 0A, forced CCM



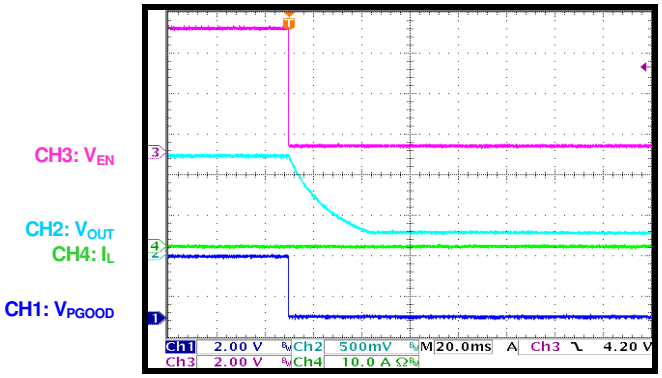
Start-Up through EN

I_{OUT} = 20A



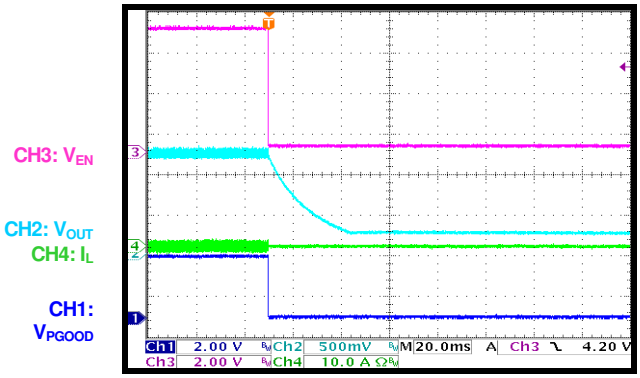
Shutdown through EN

I_{OUT} = 0A, pulse skip



Shutdown through EN

I_{OUT} = 0A, forced CCM

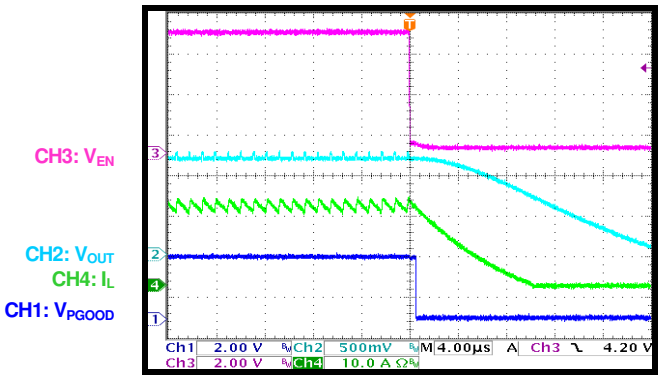


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, V_{OUT} = 1.2V, f_{SW} = 800kHz, unless otherwise noted.

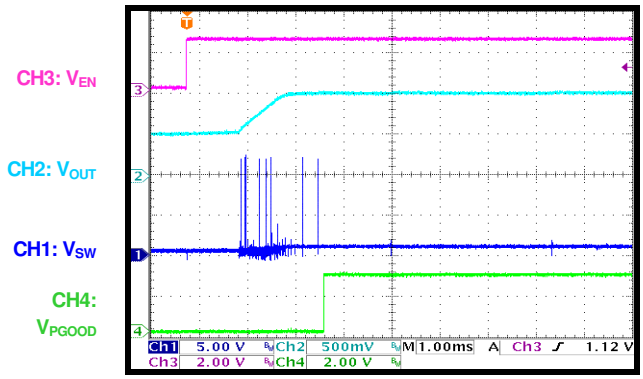
Shutdown through EN

I_{OUT} = 20A



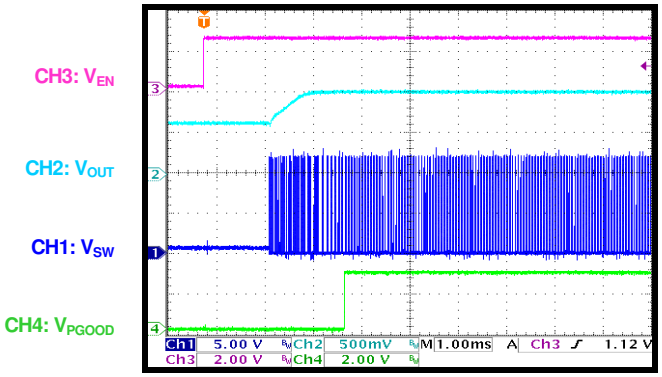
Pre-Bias Start-Up

Pulse skip

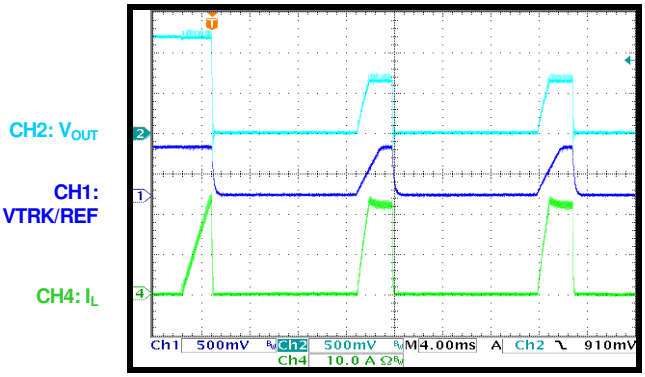


Pre-Bias Start-Up

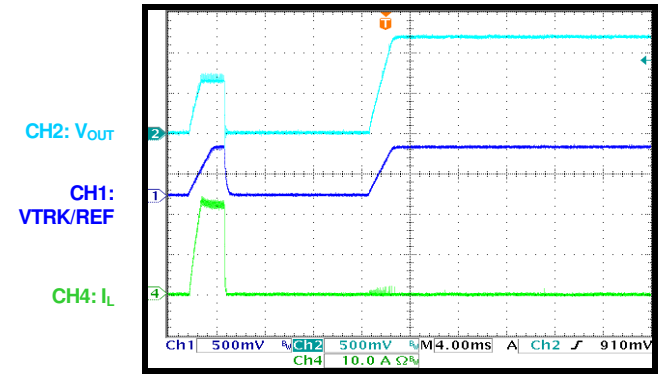
Forced CCM



Over-Current Protection Entry



Over-Current Protection Recovery



FUNCTIONAL BLOCK DIAGRAM

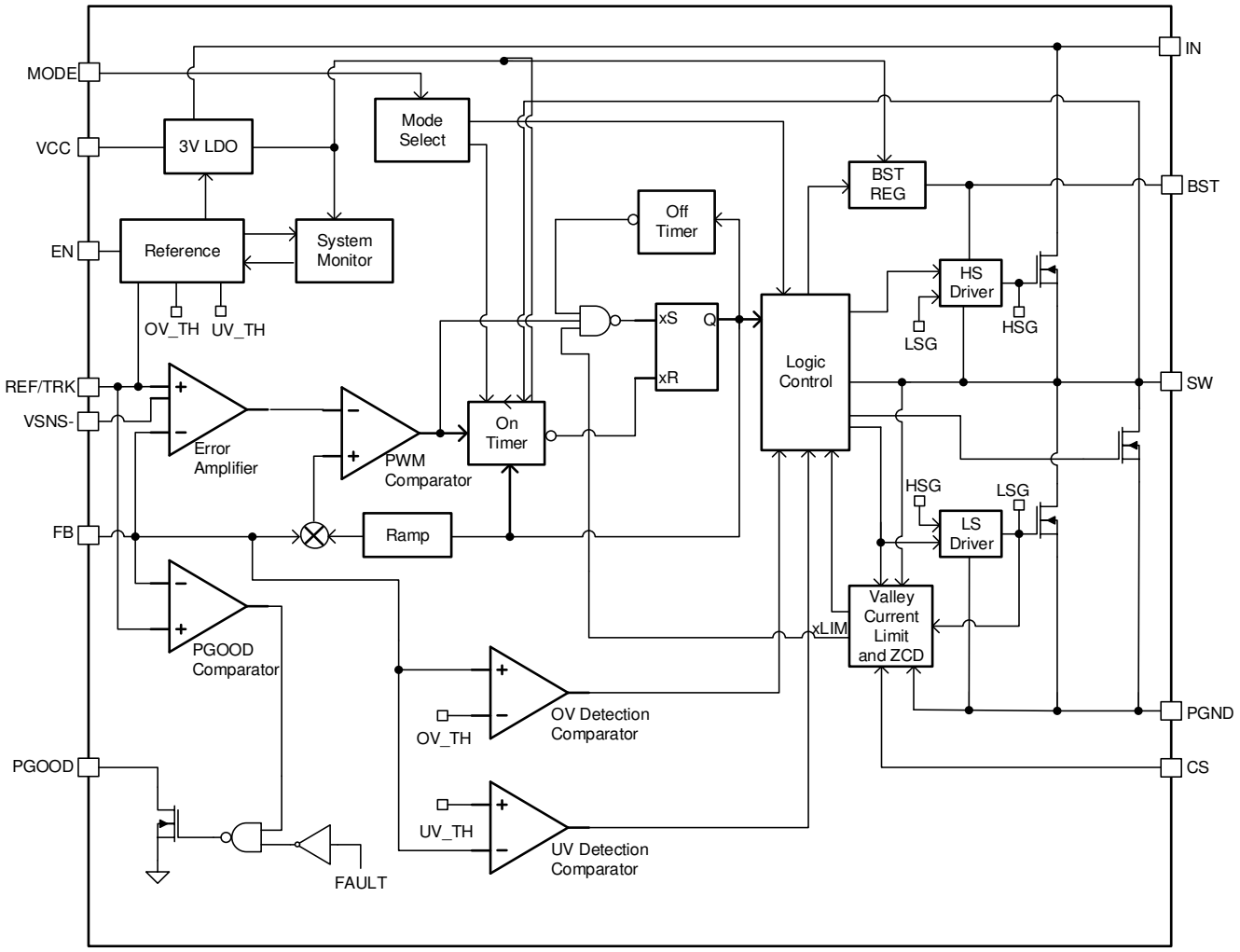


Figure 1: Functional Block Diagram

OPERATION

Constant-On-Time (COT) Control

The MP8794 employs constant-on-time (COT) control to achieve a fast load transient response. Figure 2 shows the details of the control stage of the MP8794.

The operational amplifier (AMP) corrects any voltage errors between the feedback voltage (V_{FB}) and the reference voltage (V_{REF}). The MP8794 can use AMP to provide excellent load regulation over the entire load range in either forced continuous conduction mode (CCM) or pulse skip mode.

The dedicated VSNS- pin provides differential output voltage remote sensing. The remote-sense trace pair should be kept at low impedance for optimal performance.

The MP8794 uses internal ramp compensation to support a low-ESR MLCC output capacitor solution. The adaptive internal ramp is optimized so that the MP8794 is stable across the entire operating input and output voltage ranges with a proper design of the output L/C filter.

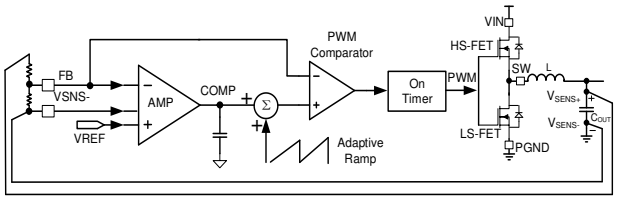


Figure 2: COT Control

Pulse-Width Modulation (PWM) Operation

Figure 3 shows the generation of the pulse-width modulation (PWM) signal. AMP corrects any error between FB and REF, and generates a fairly smooth DC voltage (COMP). The internal ramp is superimposed onto COMP when compared to the FB signal.

When V_{FB} drops below the superimposed COMP, the integrated high-side MOSFET (HS-FET) turns on. The HS-FET remains on for a fixed on time. The fixed on time is determined by the input voltage, output voltage, and selected switching frequency. After the on time elapses, the HS-FET turns off. It turns on again when V_{FB} drops below the superimposed COMP. By repeating this operation, the MP8794 regulates the output voltage.

To minimize conduction loss, the integrated low-side MOSFET (LS-FET) turns on when the HS-FET is off. A dead short occurs between VIN and PGND if both the HS-FET and the LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off period and LS-FET on period, or vice versa.

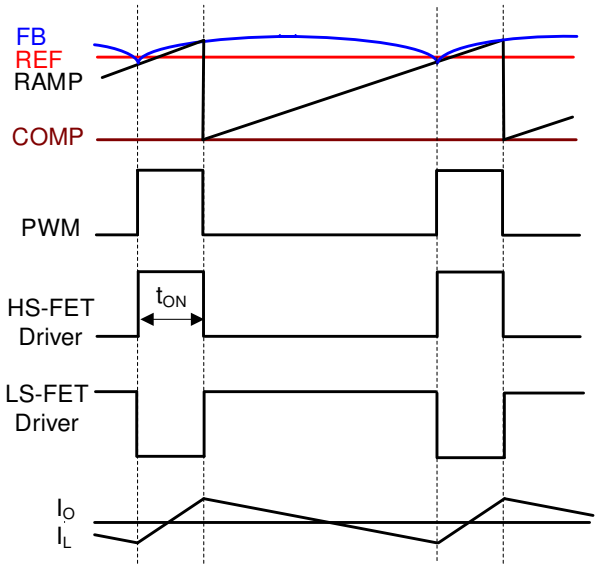


Figure 3: Heavy-Load Operation (PWM)

CCM Operation

Continuous conduction mode (CCM) occurs when the output current is high, and the inductor current is always above 0A (see Figure 3). The MP8794 can be configured to operate in forced CCM operation when the output current is low (see the Mode Selection section on page 14 for details).

In CCM operation, the switching frequency is fairly constant (PWM mode), so the output ripple remains almost constant throughout the entire load range.

Pulse Skip Operation

In light-load conditions, the MP8794 can be configured to work in pulse skip mode to optimize efficiency. When the load decreases, the inductor current also decreases. Once the inductor current reaches zero, the MP8794 transitions from CCM to pulse skip mode if the MP8794 is configured in this way (see the Mode Selection section on page 14 for details).

Figure 4 shows pulse skip mode operation under light-load conditions. When V_{FB} drops below the superimposed COMP, the HS-FET turns on for a fixed interval. When the HS-FET turns off, the LS-FET turns on until the inductor current reaches zero. In pulse skip mode operation, V_{FB} does not reach the superimposed COMP when the inductor current approaches zero. The LS-FET driver swtiches tri-state (Hi-Z) when the inductor current reaches zero.

A current modulator takes over the control of the LS-FET and limits the inductor current to below -1mA. Therefore, the output capacitors discharge slowly to PGND through the LS-FET. In a light-load condition, the HS-FET does not turn on as frequently in pulse skip mode as it does in forced CCM. As a result, the efficiency in pulse skip mode is improved compared to forced CCM operation.

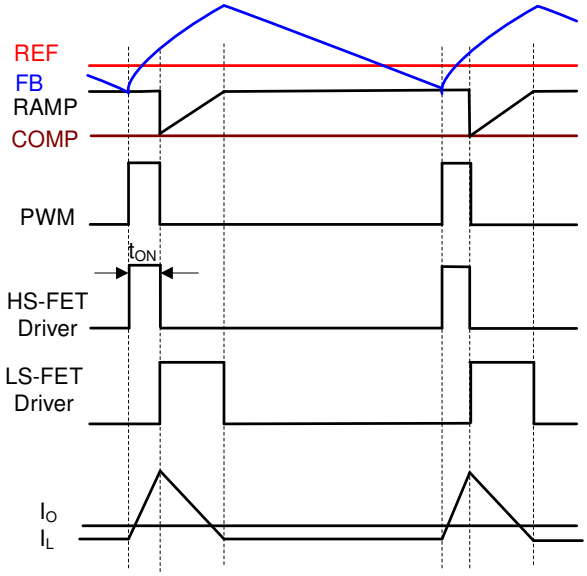


Figure 4: Pulse Skip in Light Load

As the output current increases from light load, the time period during which the current modulator regulates becomes shorter. The HS-FET turns on more frequently, and the switching frequency increases accordingly. The output current reaches critical levels when the current modulator time is zero. The critical level of the output current can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

Where f_{SW} is the switching frequency.

The MP8794 enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

The MP8794 can be configured to operate in forced CCM, even in light-load conditions (see Table 1).

Mode Selection

The MP8794 provides both forced CCM operation and pulse skip mode operation in light-load conditions. The MP8794 has three selectable switching frequency options: 600kHz, 800kHz, and 1000kHz. Selecting the operation mode and switching frequency under light-load conditions is done by choosing the resistance value of the resistor connected between MODE and AGND or VCC (see Table 1).

Table 1: Mode Selection

Mode	Light-Load Mode	Switching Frequency
VCC	Pulse skip	600kHz
243kΩ (±20%) to GND	Pulse skip	800kHz
121kΩ (±20%) to GND	Pulse skip	1000kHz
GND	Forced CCM	600kHz
30.1kΩ (±20%) to GND	Forced CCM	800kHz
60.4kΩ (±20%) to GND	Forced CCM	1000kHz

Soft Start (SS)

The minimum soft-start time is 1ms; it can be increased by adding an SS capacitor between REF/TRK and VSNS-.

The total SS capacitor value can be determined with Equation (2):

$$C_{SS}(nF) = \frac{t_{ss}(ms) \times 36\mu A}{0.6(V)} \quad (2)$$

Output Voltage Tracking and Reference

The MP8794 provides an analog input pin (REF/TRK) to track another power supply or accept an external reference. When an external voltage signal is connected to REF/TRK, it acts as a reference for the MP8794 output voltage.

The feedback voltage (V_{FB}) follows this external voltage signal, and the soft-start settings are ignored. The REF/TRK input signal can range from 0.3V to 1.4V. During initial start-up, the REF/TRK pin must reach at least 600mV to ensure proper operation. After that, it can be set to any value between 0.3V and 1.4V.

Pre-Bias Start-Up

The MP8794 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables switching for both the HS-FET and LS-FET until the voltage on the SS capacitor exceeds the sensed output voltage at FB. If the BST voltage (from BST to SW) is below 2.3V before the REF/TRK voltage reaches the pre-biased FB level, the LS-FET turns on to allow the BST voltage to be charged through VCC. The LS-FET turns on for narrow pulses, so the drop in the pre-biased level is negligible.

Output Voltage Discharge

When the MP8794 is disabled through EN, output voltage discharge mode is enabled. This causes both the HS-FET and LS-FET to latch off. A discharge FET connected between SW and PGND is turned on to discharge the output voltage. The typical switch on resistance of this FET is about 80Ω. Once V_{FB} drops below 10% of V_{REF}, the discharge FET turns off.

Current Sense and Over-Current Protection (OCP)

The MP8794 features an on-die current sense and a configurable positive current limit threshold.

The current limit is active when the MP8794 is enabled. When the LS-FET is on, the SW current (inductor current) is sensed and mirrored to CS with the ratio of G_{CS}. By using a resistor (R_{CS}) from CS to AGND, V_{CS} is proportional to the SW current cycle by cycle. The HS-FET turns on only when V_{CS} drops below the internal over-current protection (OCP) voltage threshold (V_{OCP}) while the LS-FET is on to limit the SW valley current cycle by cycle.

Calculate the current limit threshold setting from R_{CS} with Equation (3):

$$R_{CS}(\Omega) = \frac{V_{OCP}}{G_{CS} \times (I_{LIM} - \frac{(V_{IN} - V_O) \times V_O}{V_{IN}} \times \frac{1}{2 \times L \times f_{SW}})} \quad (3)$$

Where V_{OCP} = 1.2V, G_{CS} = 10μA/A, and I_{LIM} is the desired output current limit (in A).

OCP hiccup becomes active 3ms after the MP8794 is enabled. Once OCP hiccup is active, if the MP8794 detects an over-current condition for 31 consecutive cycles, or if V_{FB} drops below the under-voltage protection (UVP) threshold, the device enters hiccup mode. In hiccup mode, the MP8794 latches off the HS-FET immediately and latches off the LS-FET after zero-current cross detection (ZCD). Meanwhile, the SS capacitor is also discharged.

After about 11ms, the MP8794 attempts to soft start automatically. If the over-current condition still remains after 3ms, the MP8794 repeats this operation cycle until the over-current condition is removed. Then the output voltage smoothly rises back to the regulation level.

Negative Inductor Current Limit

When the LS-FET detects a -18A current, the MP8794 turns off the LS-FET for 200ns to limit the negative current.

Output Sinking Mode (OSM)

The MP8794 employs output sinking mode (OSM) to regulate the output voltage to the targeted value. When V_{FB} exceeds 104% of V_{REF} but is below the OVP threshold, it triggers OSM. During OSM operation, the LSFET remains on until it reaches the -5.5A negative current limit. Upon reaching -5.5A, the LS-FET turns off for 200ns; the HS-FET turns on during this period. After 200ns, the LS-FET turns on again. The MP8794 maintains this operation until V_{FB} drops below 102% of V_{REF}. Once it does, the MP8794 exits OSM after 15 consecutive cycles of forced CCM.

Over-Voltage Protection (OVP)

The MP8794 monitors the output voltage by connecting FB to the tap of the output voltage feedback resistor divider to detect an over-voltage condition. This provides hiccup over-voltage protection (OVP).

If the feedback voltage (V_{FB}) exceeds 116% of the reference voltage (V_{REF}), OVP is triggered. The LS-FET remains on until it triggers the low-side negative current limit (NOCP). Once the LS-FET triggers NOCP, the LS-FET turns off for 200ns; the HS-FET turns on during this period. After 200ns, the LS-FET turns on again. The MP8794 repeats this operation to discharge any over-voltage on the output. The MP8794 exits this mode when V_{FB} drops below 105% of V_{REF}.

Over-Temperature Protection (OTP)

The MP8794 has over-temperature protection (OTP). The IC monitors the junction temperature internally. If the junction temperature exceeds the threshold value (typically 160°C), the MP8794 latches off the HS-FET immediately and latches off the LS-FET once ZC is detected Meanwhile, the SS capacitor is also discharged. Once the junction temperature drops to about 130°C, a soft start is initiated. The OTP function is effective once the MP8794 is enabled.

Output Voltage Setting and Remote Output Voltage Sensing

First, choose a value for R_{FB1}. Then R_{FB2} can be determined with Equation (4):

$$R_{FB2}(k\Omega) = \frac{V_{REF}}{V_O - V_{REF}} \times R_{FB1}(k\Omega) \quad (4)$$

To optimize the load transient response, a feed-forward capacitor (C_{FF}) should be placed in parallel with R_{FB1}. R_{FB1} and C_{FF} add an extra zero frequency to the system, which improves loop response. R_{FB1} and C_{FF} are selected so that the zero frequency formed by R_{FB1} and C_{FF} is located at about 20kHz to 60kHz. Calculate this zero frequency with Equation (5):

$$f_Z = \frac{1}{2\pi \times R_{FB1} \times C_{FF}} \quad (5)$$

Power Good (PGOOD)

The MP8794 has a power good output pin (PGOOD). PGOOD is the open-drain of a MOSFET. Connect PGOOD to VCC or another external voltage source below 3.6V through a pull-up resistor (typically 10kΩ). After applying the input voltage, the MOSFET turns on, so PGOOD is pulled to GND before SS is ready. After the FB voltage reaches 92.5% of V_{REF} and a 0.9ms delay , PGOOD is pulled high.

When V_{FB} drops to 80% of V_{REF} or exceeds 116% of the nominal V_{REF}, PGOOD is latched low. PGOOD can only be pulled high again after a new SS.

If the input supply fails to power the MP8794, PGOOD is clamped low, even though PGOOD is tied to an external DC source through a pull-up resistor. Figure 5 shows the relationship between the PGOOD voltage and the pull-up current.

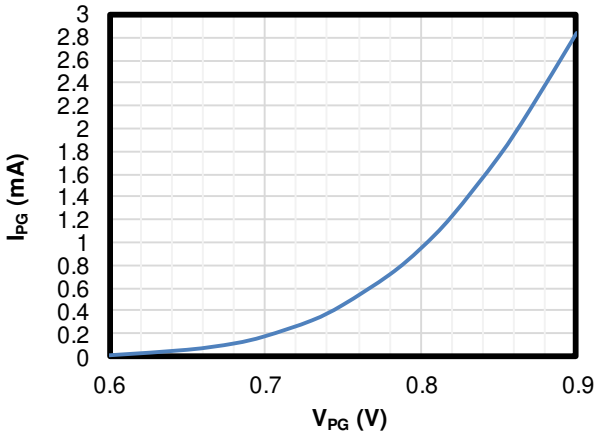


Figure 5: PGOOD Clamped Voltage vs. Pull-Up Current

Enable (EN) Configuration

The MP8794 turns on when EN goes high. The MP8794 turns off when EN goes low. Do not leave EN floating. EN can be driven by an analog or digital control logic signal to enable or disable the MP8794. The MP8794 provides accurate EN thresholds, so a resistor divider from VIN to AGND can be used to program the input voltage at which the MP8794 is enabled. This is highly recommended for applications where there is no dedicated EN control logic signal. This avoids possible UVLO bouncing during start-up and shutdown. The resistor divider values can be determined with Equation (6):

$$V_{IN\_START}(V) = VIH_{EN} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (6)$$

Where VIH_{EN} is typically 1.22V.

R_{UP} and R_{DOWN} should be chosen so that V_{EN} does not exceed 3.6V when V_{IN} reaches its maximum value.

EN can also be connected directly to VIN through a pull-up resistor (R_{UP}). R_{UP} should be chosen so that the maximum current going to EN is 50μA. R_{UP} can be calculated with Equation (7):

$$R_{UP}(k\Omega) = \frac{VIN_{MAX}(V)}{0.05(mA)} \quad (7)$$

APPLICATION INFORMATION

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Use ceramic capacitors for the best performance. During layout design, place the input capacitors as close to VIN as possible.

The capacitance can vary significantly with the temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over a wide temperature range and offer very low ESR.

The capacitors must have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current with Equation (8):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (8)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (9):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (9)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current. The input capacitor value determines the converter input voltage ripple. If there is an input voltage ripple requirement in the system, select an input capacitor that meets the specification.

Estimate the input voltage ripple with Equation (10):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (11):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (11)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use POSCAP or ceramic capacitors.

Estimate the output voltage ripple with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (12)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, estimate the output voltage ripple with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

For simplification, the output ripple can be estimated with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (14)$$

Selecting the Inductor

The inductor supplies a constant current to the output load while being driven by the switching input voltage. A larger-value inductor results in less ripple current and lower output ripple voltage. However, it also has a larger physical size, a higher series resistance, and a lower saturation current. It is usually recommended to select an inductor value that sets the inductor peak-to-peak ripple current between 30% and 40% of the maximum switch current limit. Design for a peak inductor current that is below the maximum switch current limit. Calculate the inductance value with Equation (15):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that does not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (16):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (16)$$

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 lists our power inductor recommendations. Select a part number based on your design requirements.

Table 2: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
MPL-AY1265-R47	0.47µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 6 and follow the guidelines below:

1. Place the input MLCC capacitors as close to VIN and PGND as possible.
2. Place the major MLCC capacitors on the same layer as the MP8794.
3. Maximize the VIN and PGND copper plane to minimize the parasitic impedance.
4. Use as many PGND vias as possible, and place them close to PGND to minimize both parasitic impedance and thermal resistance.
5. Place the VCC decoupling capacitor close to the device.
6. Connect AGND and PGND at the point of the VCC capacitor's ground connection.
7. Place the BST capacitor as close to BST and SW as possible with traces 20 mil or wider to route the path. It is recommended to use a bootstrap capacitor between 0.1µF and 1µF.
8. Place the SS capacitor close to REF/TRK to VSNS-.
9. If they must be placed on the PGOOD pad, place vias at least 10mm away from the positive side of the first input decoupling capacitor and close to the IC.

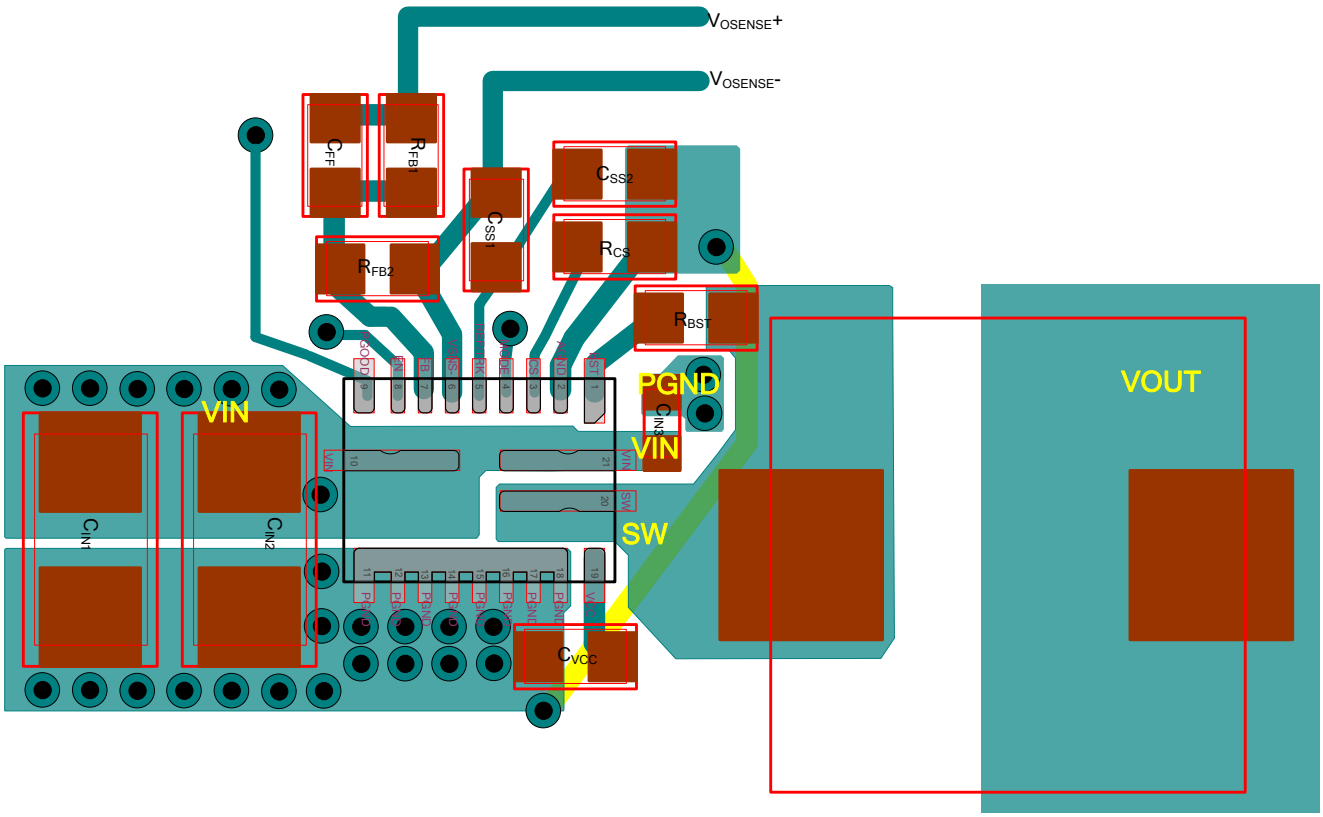
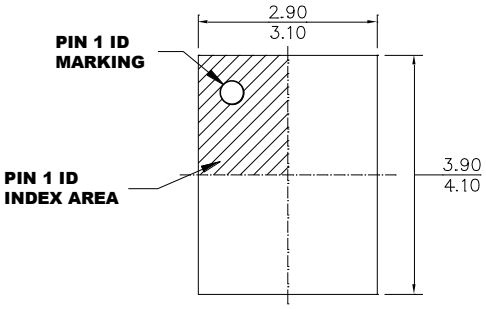


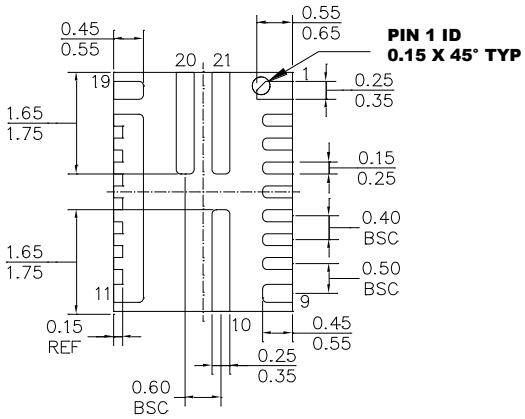
Figure 6: Recommended PCB Layout

PACKAGE INFORMATION

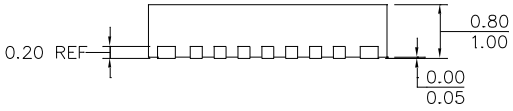
QFN-21 (3mmx4mm)



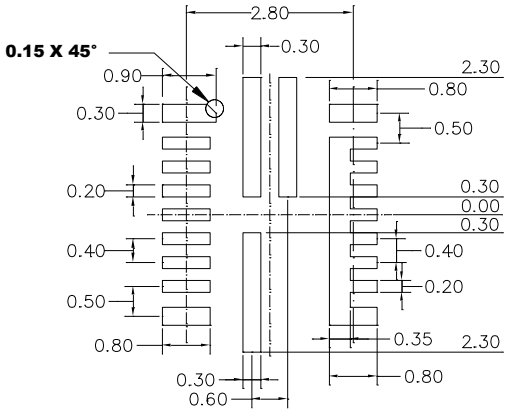
TOP VIEW



BOTTOM VIEW



SIDE VIEW

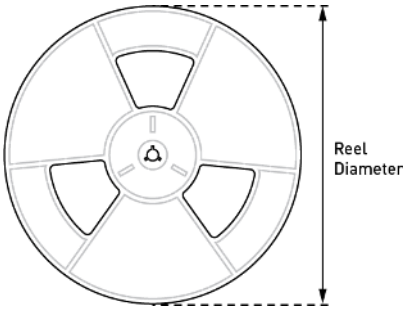


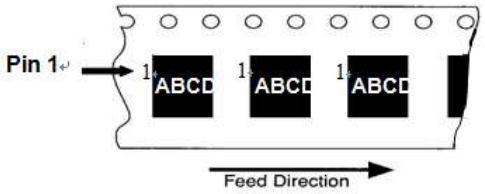
RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERN OF PIN1,9,10,11,19,20 AND 21 HAVE THE SAME WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/Reel	Quantity/Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8794GLE-Z	QFN-21 (3mmx4mm)	5000	nN/A	13in	12mm	8mm