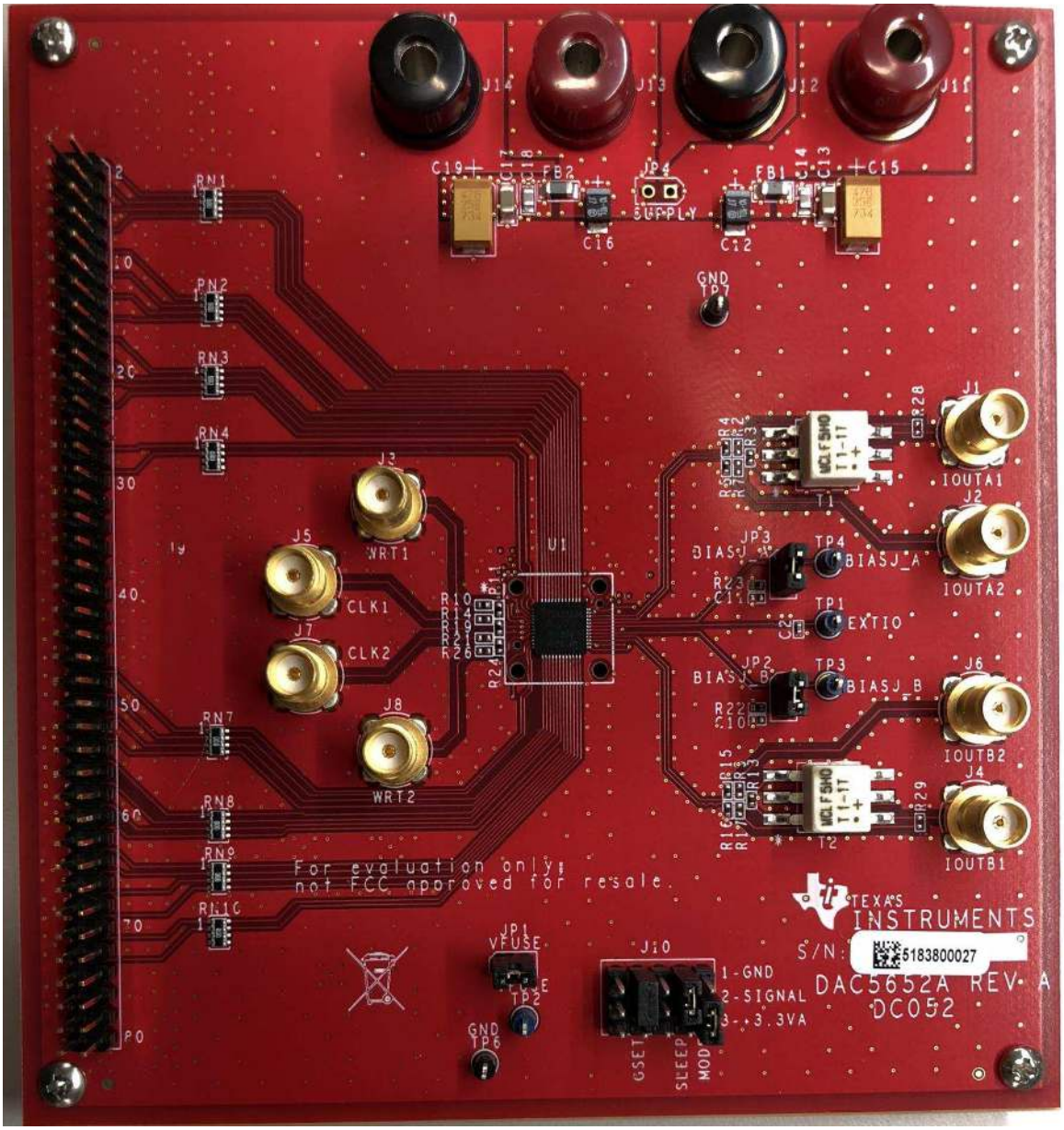
DAC5652AEVM User's Guide

This user's guide describes the characteristics, operation, and use of the DAC5652A evaluation module (EVM). This EVM is designed to evaluate the performance of the DAC5652A dual, 10-bit, 275-MSPS digital-to-analog converter (DAC) in a variety of configurations. Throughout this document, the terms *evaluation board*, *evaluation module*, and *EVM* are synonymous with the *DAC5652AEVM*. This document includes a schematic, printed circuit board (PCB) layouts, and a complete bill of materials (BOM).



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1 Introduction

Digital inputs to the DAC can be provided with CMOS level signals up to 275 MSPS through 80-pin headers. Doing so enables the user to provide high-speed digital data to the DAC5652A.

The analog output from the DAC is available via SMA connectors. Because of its flexible design the analog output of the DAC5652A can be configured to drive a 50-Ω terminated cable using a 4:1 or 1:1 impedance ratio transformer or single-ended referred to GND.

Power connections to the EVM are via banana jack sockets. Separate sockets are provided for the analog and digital supplies.

In addition to the internal band-gap reference provided by the DAC5652A device, options are provided on the EVM to allow external reference to be provided to the DAC.

1.1 Required Hardware and Software

The following hardware and software are required to evaluate the DAC5652A device:

- DAC5652AEVM: Main circuit board containing the DAC to be evaluated
- TSW1400EVM: Hardware that generates digital patterns for the DAC: TSW1400EVM
- HSDC pro software: Software interface that controls the TSW1400EVM. Version 4.80 or higher is recommended: dataconverterpro-sw

1.2 Hardware Description

Figure 1 shows the EVM setup diagram.

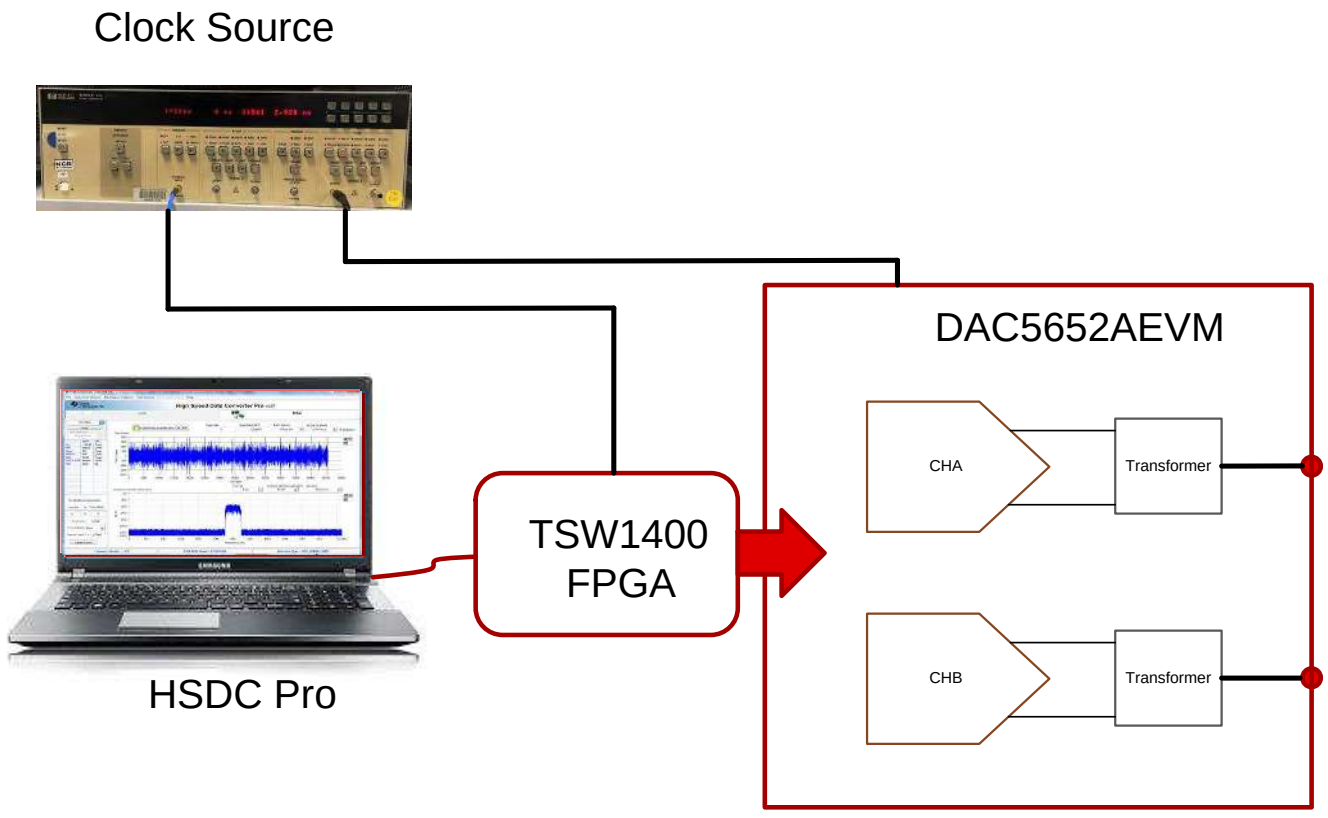

Figure 1. DAC5652AEVM Setup Diagram

1.3 DAC5652AEVM Operation Procedure

The DAC5652AEVM can be set up in a variety of configurations to accommodate a specific mode of operation. Before starting evaluation, the user must decide on the configuration and make the appropriate connections or changes. The demonstration board comes with following factory-set configuration:

Single clock source mode using a clock input at J3. Single clock source driving CLK_1, WRT_1, CLK_2, and WRT_2 from WRT_1 input.

- Transformer-coupled outputs using transformer T1 and T2.
- The converter is set to operate with internal reference.
- Full-scale output current set to 19.2 mA through RBIAS resistor R22 and R23 (GSET jumper on J10 installed between pins 10 and 11 and JP2 and JP3 installed).
- The DAC5652A output is enabled (sleep mode disabled). Sleep jumper on J10 is installed between pins 4 and 5.
- Data input set to dual port mode. Mode jumper on J10 is installed between pins 2 and 3.
- Dual input power supplies required.
- VFUSE function disabled. JP1 installed.

2 Power Requirements

The demonstration board requires only two power supplies. The first, +3.3 VA, is required to be +3.3 VDC at banana jack J11 with the return going to J12. This supply is the analog supply for the DAC5652A. The second, +3.3 VB, is required to be +3.3 VDC at banana jack J13 with the return to J14. This supply is the digital +3.3-V supply for the DAC5652A.

2.1 External Reference Operation

The internal reference can be disabled by simply applying an external reference voltage into the EXTIO pin using test point 1. The use of an external reference may be considered for applications that require higher accuracy and drift performance, or to add the ability of dynamic gain control. The reference input has a high impedance and can easily be driven by various sources.

3 Schematic Diagram

The schematic diagram for the EVM can be down loaded from the product folder at DAC5652AEVM.

3.1 Input Clock

The DAC5652AEVM default operation setting is with a single-ended input clock sent to the DAC5652A. A 3 V_{PP}, 1.5-V offset, 50% duty cycle external square wave is applied to SMA connector J3. This input represents a 50-Ω load to the source. In order to preserve the specified performance of the DAC5652A converter, the clock source features very low jitter. Using a clock with a 50% duty cycle gives optimum dynamic performance. Options are provided to operate the two DACs with separate clocks. Another option allows the user to provide separate write enables when using interleave mode. See Table 1 for proper board configuration.

3.2 Input Data

The DAC5652A EVM can accept +3.3-V CMOS logic level data inputs through the 80-pin headers J9 in Table 1. The user can provide series dampening resistors to minimize digital ringing and switching noise if required. The default values are 0 Ω.

Table 1. Input Connector J9

J9 Pin Number	Description	J9 Pin Number	Description
9	DAC A data bit 9 (MSB)	55	DAC B data bit 9 (MSB)
10	Ground	56	Ground
11	DAC A data bit 8	57	DAC B data bit 8
12	Ground	58	Ground
13	DAC A data bit 7	59	DAC B data bit 7
14	Ground	60	Ground
15	DAC A data bit 6	61	DAC B data bit 6
16	Ground	62	Ground
17	DAC A data bit 5	63	DAC B data bit 5
18	Ground	64	Ground
19	DAC A data bit 4	65	DAC B data bit 4
20	Ground	66	Ground
21	DAC A data bit 3	67	DAC B data bit 3
22	Ground	68	Ground
23	DAC A data bit 2	69	DAC B data bit 2
24	Ground	70	Ground
25	DAC A data bit 1	71	DAC B data bit 1
26	Ground	72	Ground
27	DAC A data bit 0 (LSB)	73	DAC B data bit 0 (LSB)
28	Ground	74	Ground

3.2.1 Output Signal

The DAC5652AEVM can be configured to drive a doubly terminated 50-Ω cable or provide unbuffered differential outputs.

3.2.2 Transformer-Coupled Signal Output

The factory-set configuration of the demonstration board provides the user with a single-ended output signals from channel A and B of the DAC at SMA connector J1 and J4. The DAC5652A is configured to drive a doubly terminated 50-Ω cable using a 4:1 impedance ratio transformer and the center tap of T1 and T2 connected to ground. When using a 1:1 impedance ratio transformer, configure the EVM per Table 2.

Table 2. Transformer Output Configuration

Configuration	Components Installed	Components Not Installed
1:1 Impedance ratio transformer	R3−R5, R13, R15,R16 T1, T2	R1, R8, C1, C9
4:1 Impedance ratio transformer	R4 (100), R5 (100), R15 (100), R16 (100), T1 (4:1), T2 (4:1)	R1, R3, R13, R9, R18, C1, C9

3.2.2.1 Unbuffered Differential Output

To provide unbuffered differential outputs, the EVM must be configured as follows: Remove R3, R13, T1, and T2; Install R10, R12, R15, R18, R25, R29, J6, and J28.

3.2.2.2 Internal Reference Operation

The full-scale output current is set by applying an external resistor (R_{SET}) between the BIASJ pins of the DAC5652A and ground. The full-scale output current can be adjusted from 20 mA down to 2 mA by varying R_{SET} or changing the externally applied reference voltage. The full-scale output current, I_{OUTFS}, is defined as: $I_{OUTFS} = 32 \times (V_{EXTIO} / R_{SET})$, where V_{EXTIO} is the voltage at pin EXTIO. This voltage is 1.2 V (typical) when using the internally provided band-gap reference voltage source. On the DAC5652AEVM, R23 is used to set the output current of channel A and R22 is used to set channel B.

4 Device Modes and Settings

4.1 Sleep Mode

The DAC5652AEVM provides a means of placing the DAC5652A into a power-down mode. This mode is activated by placing jumper J10 between pins 5 and 6.

4.2 Gain Set

The full-scale output current on the DAC5652A can be set two ways: both channels independently or simultaneously. For independent gain control, set GSET to a logic low. This mode is activated by placing jumper J10 between pins 7 and 8. For simultaneous mode, set GSET to a logic high. This mode is activated by placing jumper J10 between pins 8 and 9.

5 Input Data Mode

The DAC5652AEVM provides a means of placing the DAC5652A into a dual-port data input mode or interleaved mode. With MODE set to a logic high (JP10 set to 2 and 3), the device operates in dual-port mode. With MODE set to a logic low (JP10 set to 1 and 2), the device operates in interleave mode.

6 Quick-Start Procedure

1. Connect EVM to TSW1400 board through the CMOS connectors
2. Apply 3.3-V power to J11 and J13; connect ground to J12, J14
3. Setup the clock signals through the HP8133A
   - Inject 100 MHz to the external input
   - Set channel 1 and 2 with
     - 3.3-V amplitude
     - 1.65-V offset
     - Divide by 1
     - 0-ps delay
   - Connect channel 1 output to CMOS clock input (J7) of the TSW1400
   - Connect channel 2 output to J3 on the DAC5652AEVM
4. Connect DAC output J1 to the spectrum analyzer
5. Setup the TSW1400. Launch the HSDCpro software and connect the TSW1400EVM to the PC.
   - Click the DAC tab. Set sample rate to 100 MSPS (that is, match the clock rate)
   - Select the CMOS .ini file using the dropdown button on upper left corner of the GUI
   - Select Offset Bin
   - On the lower left corner of the HSDCpro GUI under I/Q Mutlitone Generator enter 1 for number of tones and tone center as 10M.

- Set the number of samples to 65536 and select real for tone selection
- Click the Create Tones button
- Click Send to send the tone to the DAC

6. Verify the output signal at J1 and J2
7. Adjust the channel 1 output delay on the HP8133A if needed to eliminate timing errors

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