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FAIRCHILD

SEMICONDUCTOR*

74LVX573 Low Voltage Octal Latch with 3-STATE Outputs

General Description

The LVX573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (\overline{OE}) inputs. The LVX573 is functionally identical to the LVX373 but with inputs and outputs on opposite sides of the package. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

June 1993

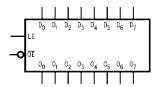
Revised April 2005

Ordering Code:

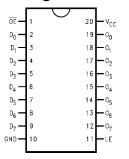
Order Number	Package Number	Package Description						
74LVX573M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide						
74LVX573SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide						
74LVX573MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide						
Devices also available	Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.							

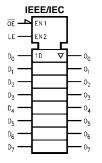
Pb-Free package per JEDEC J-STD-020B.

Logic Symbols



Connection Diagram





Pin Descriptions

Pin Names	Description
D ₀ -D ₇	Data Inputs
LE	Latch Enable Input
OE	3-STATE Output Enable Input
O ₀ -O ₇	3-STATE Latch Outputs

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Functional Description

The LVX573 contains eight D-type latches. When the enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are enabled. When \overline{OE} is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

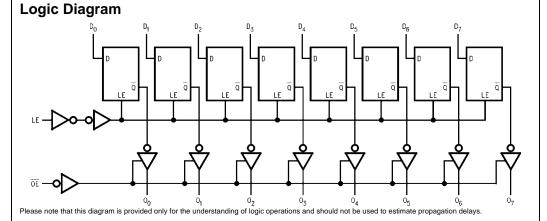
	Inputs						
OE	LE	D	O _n				
L	Н	н	Н				
L	н	L	L				
L	L	х	O ₀				
Н	Х	Х	Z				

H = HIGH Voltage

L = LOW Voltage Z = High Impedance

X = Immaterial

 $O_0 =$ Previous O_0 before HIGH-to-LOW transition of Latch Enable



Absolute Maximum Ratings(Note 1)

Supply Voltage (V _{CC})	-0.5V to +7.0V
DC Input Diode Current (I _{IK})	
$V_{I} = -0.5V$	–20 mA
DC Input Voltage (VI)	-0.5V to 7V
DC Output Diode Current (I _{OK})	
$V_O = -0.5V$	–20 mA
$V_{O} = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V _O)	–0.5V to V _{CC} + 0.5V
DC Output Source	
or Sink Current (I _O)	±25 mA
DC V _{CC} or Ground Current	
(I _{CC} or I _{GND})	±75 mA
Storage Temperature (T _{STG})	-65°C to +150°C
Power Dissipation	180 mW

Recommended Operating Conditions (Note 2)

Supply Voltage (V _{CC})	2.0V to 3.6V
Input Voltage (V _I)	0V to 5.5V
Output Voltage (V _O)	0V to V _{CC}
Operating Temperature (T _A)	-40°C to +85°C
Input Rise and Fall Time ($\Delta t / \Delta V$)	0 ns/V to 100 ns/V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Vcc		T _A = +25°C	;	$T_A = -40^{\circ}$	C to +85°C	Units	Conditions	
0,11201		- 00	Min	Тур	Max	Min	Max	onno	Conditions	
VIH	HIGH Level	2.0	1.5			1.5				
	Input Voltage	3.0	2.0			2.0		V		
		3.6	2.4			2.4				
VIL	LOW Level	2.0			0.5		0.5			
	Input Voltage	3.0			0.8		0.8	V		
		3.6			0.8		0.8			
V _{OH}	HIGH Level	2.0	1.9	2.0		1.9			$V_{IN} = V_{IH} \text{ or } V_{IL} I_{OH} =$	-50 μA
	Output Voltage	3.0	2.9	3.0		2.9		V	I _{OH} =	–50 μA
		3.0	2.58			2.48			I _{OH} =	–4 mA
V _{OL}	LOW Level	2.0		0.0	0.1		0.1		$V_{IN} = V_{IH} \text{ or } V_{IL} I_{OL} =$	50 μA
	Output Voltage	3.0		0.0	0.1		0.1	V	I _{OL} =	50 μA
		3.0			0.36		0.44		I _{OL} =	4 mA
I _{OZ}	3-STATE Output	3.6			±0.25		±2.5	μA	$V_{IN} = V_{IH} \text{ or } V_{IL}$	
	Off-State Current								$V_{OUT} = V_{CC} \text{ or } GND$	
I _{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V _{IN} = 5.5V or GND	
Icc	Quiescent Supply Current	3.6			4.0		40.0	μA	$V_{IN} = V_{CC}$ or GND	

Noise Characteristics (Note 3)

Symbol	Parameter	V _{cc}	T _A =	25°C	Units	C _L (pF)	
	i didilotor	(V)	Тур	Limit			
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.5	0.8	V	50	
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.5	-0.8	V	50	
VIHD	Minimum HIGH Level Dynamic Input Voltage	3.3		2.0	V	50	
V _{ILD}	Maximum LOW Level Dynamic Input Voltage	3.3		0.8	V	50	

Note 3: (Input $t_r = t_f = 3ns$)

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AC Electrical Characteristics

Symbol	Parameter	V _{CC}		$T_A = +25^{\circ}C$;	$T_A = -40^{\circ}$	C to +85°C	Units	Conditions
Symbol	Falanielei	(V)	Min	Тур	Max	Min	Max		
t _{PLH}	Propagation	2.7		7.6	14.5	1.0	17.5		C _L = 15 pF
t _{PHL}	Delay Time			10.1	18.0	1.0	21.0	ns	C _L = 50 pF
	D _n to O _n	$\textbf{3.3}\pm\textbf{0.3}$		5.9	9.3	1.0	11.0	115	$C_L = 15 \text{ pF}$
				8.4	12.8	1.0	14.5		C _L = 50 pF
t _{PLH}	Propagation	2.7		8.2	15.6	1.0	18.5		C _L = 15 pF
t _{PHL}	Delay Time			10.7	19.1	1.0	22.0	ns	C _L = 50 pF
	LE to O _n	$\textbf{3.3}\pm\textbf{0.3}$		6.4	10.1	1.0	12.0	115	C _L = 15 pF
				8.9	13.6	1.0	15.5		C _L = 50 pF
t _{PZL}	3-STATE Output	2.7		7.8	15.0	1.0	18.5		$C_L = 15 \text{ pF}, R_L = 1 \text{ k}\Omega$
t _{PZH}	Enable Time			10.3	18.5	1.0	22.0	ns	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$
		$\textbf{3.3}\pm\textbf{0.3}$		6.1	9.7	1.0	12.0	115	$C_L = 15 \text{ pF}, R_L = 1 \text{ k}\Omega$
				8.6	13.2	1.0	15.5		$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$
t _{PLZ}	3-STATE Output	2.7		12.1	19.1	1.0	22.0	ns	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$
t _{PHZ}	Disable Time	$\textbf{3.3}\pm\textbf{0.3}$		10.1	13.6	1.0	15.5	113	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$
t _W	LE Pulse	2.7	6.5			7.5		ns	
	Width	$\textbf{3.3}\pm\textbf{0.3}$	5.0			5.0		113	
t _S	Setup Time	2.7	5.0			5.0		ns	
	D _n to LE	$\textbf{3.3}\pm\textbf{0.3}$	3.5			3.5		115	
t _H	Hold Time	2.7	1.5			1.5		ns	
	D _n to LE	$\textbf{3.3}\pm\textbf{0.3}$	1.5			1.5		113	
t _{OSHL}	Output to Output	2.7			1.5		1.5	ns	C _L = 50 pF
t _{OSLH}	Skew (Note 4)	2.3			1.5		1.5	113	

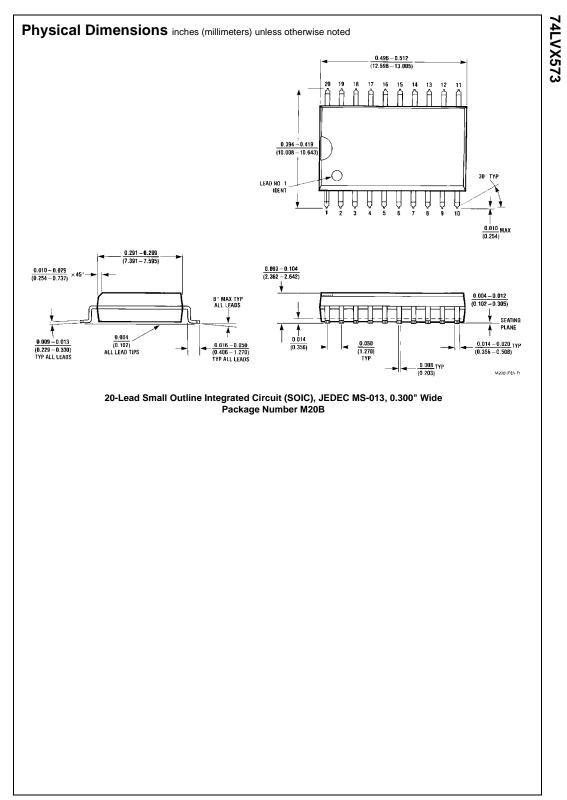
Note 4: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.

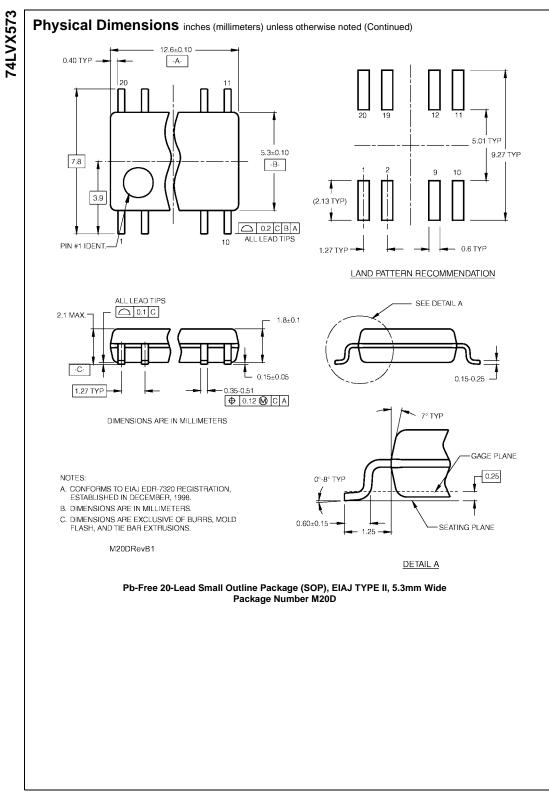
Capacitance

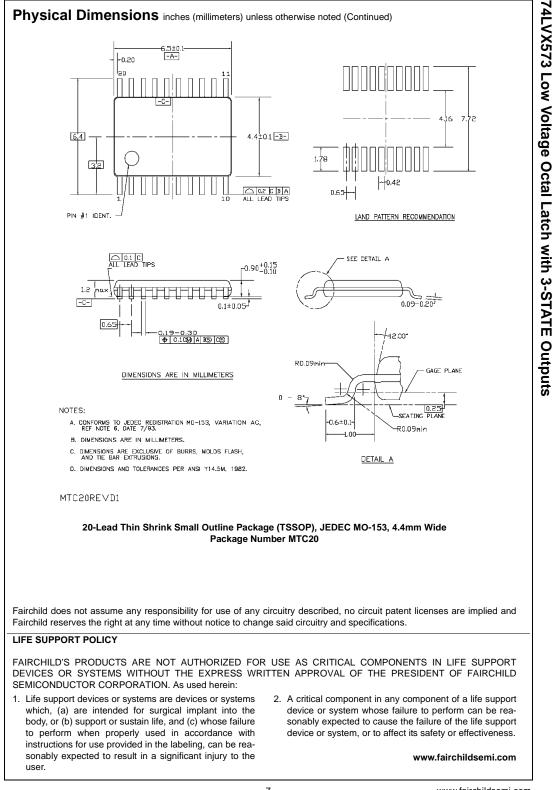
Symbol	Parameter		T _A = +25°C		$T_A = -40^{\circ}$	Units	
	i di dificici	Min	Тур	Max	Min	Max	onita
CIN	Input Capacitance		4	10		10	pF
C _{OUT}	Output Capacitance		6				pF
CPD	Power Dissipation		27				pF
	Capacitance (Note 5)						

Note 5: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per latch)}}$







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